Application Report
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Low-Emission Designs With ISOW7841 Integrated Signal and Power Isolator

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ABSTRACT

The ISOW7841 integrated signal and power isolation device simplifies system design and reduces board area. The use of low-inductance micro-transformers in the ISOW7841 device necessitates the use of high-frequency switching, resulting in higher radiated emissions compared to discrete solutions. The ISOW7841 device uses on-chip circuit techniques to reduce emissions compared to competing solutions. Techniques such as lower supply operation, the use of interlayer stitching capacitance, filters, and common-mode chokes can further reduce radiated emissions at the system level.

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1 Introduction

Texas Instruments' ISOW7841 device is a high-performance 5000-V_{RMS} reinforced quad-channel digital isolator with an integrated high-efficiency, low-emissions DC/DC converter. Figure 1 shows a pinout and simplified block diagram of the ISOW7841 device.

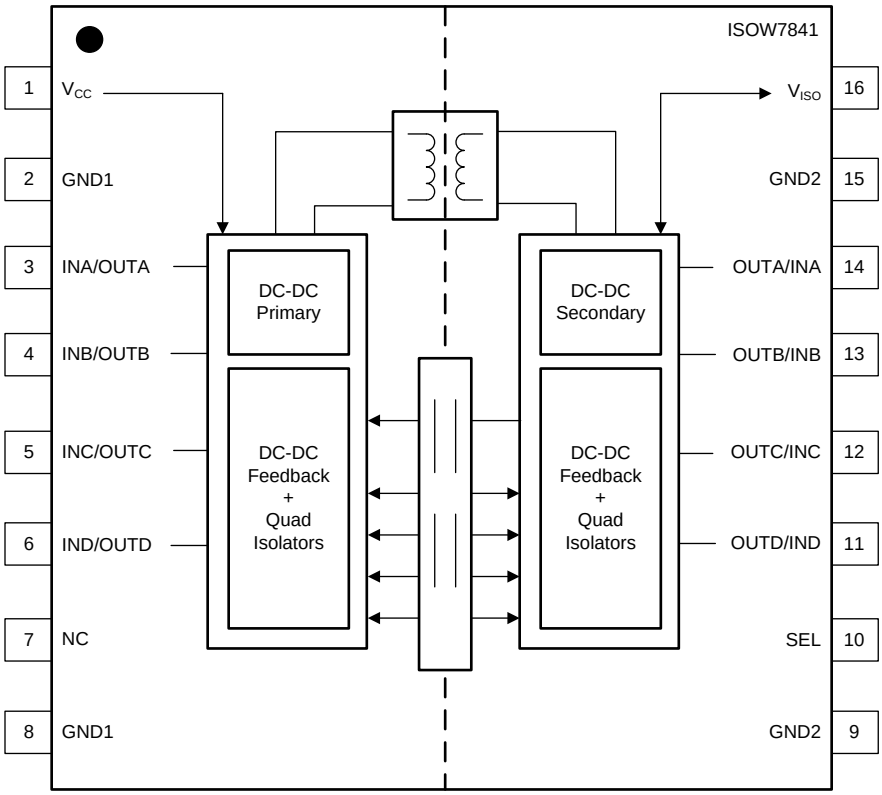


Figure 1. ISOW7841 Single-Chip Power and Data Isolation

Traditionally, discrete transformers in addition to driver integrated circuits (ICs) have been used to generate isolated power. The ISOW7841 device uses chip-scale transformers to integrate the isolated power converter in a small outline SOIC-16 package. These chip-scale transformers are very small in size, use only a few turns (to reduce series resistance), and use an air core. Consequently, the DC/DC converter driving these transformers must operate at a few tens of megahertz. Because the primary and secondary windings of the transformers are very close to each other inside the package, a parasitic capacitance forms between the two coils of the transformer. The fast transients in the DC/DC converter couple through this parasitic capacitance creating a common-mode current between side 1 and side 2 of the isolated system (see Figure 2). Because the two sides are completely isolated, the current forms a large return loop through board-level parasitic capacitances. This large current loop can cause radiated emissions in isolated systems. Another way to understand the emissions mechanism is that the two isolated parts of the board form a dipole antenna transmitter.

In discrete implementations with on-board transformers, radiated emissions are lower because of the use of high-inductance magnetic-core transformers and much lower switching frequencies.

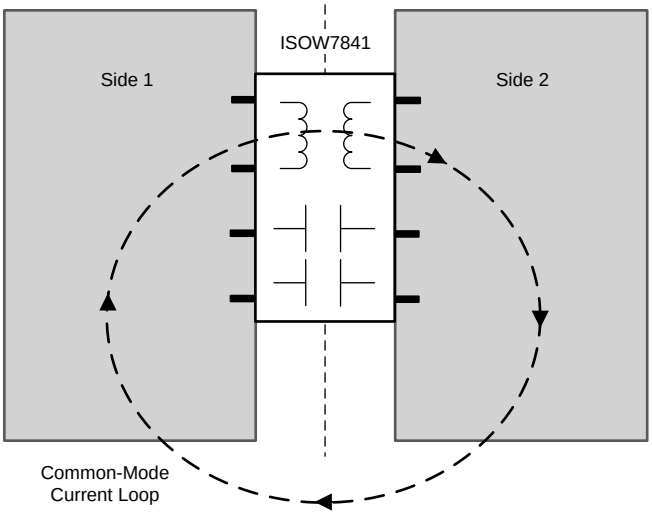


Figure 2. Common-Mode Currents Across the Isolation Barrier form a Large Return Loop

The ISOW7841 device uses several techniques, including symmetric design and layout, and clock dithering to reduce electromagnetic emissions which competing solutions do not use. Figure 3 compares the performance of the ISOW7841 device with an equivalent competitor device under identical conditions. The ISOW7841 device passes the CISPR22B standard, and is more than 15 dB lower in emissions in absolute terms.

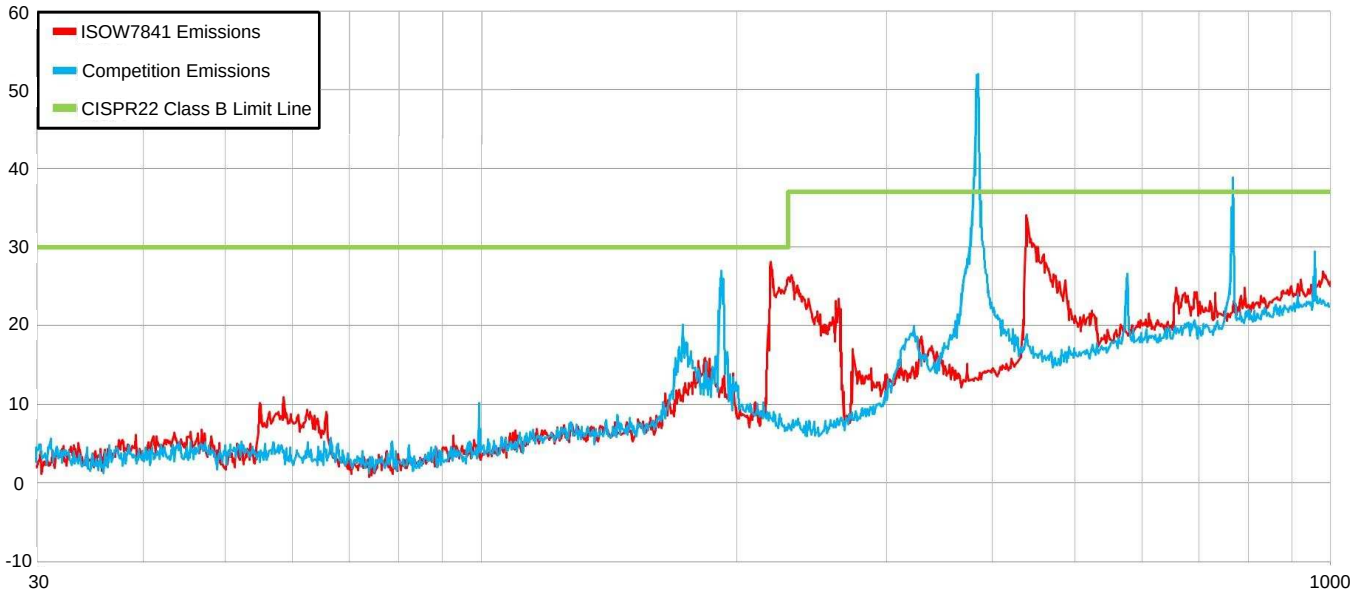


Figure 3. Radiated Emissions of the ISOW7841 vs a Competitive Device at 5-V Input and 80-mA Load

While the ISOW7841 device achieves low emissions even with a standard evaluation module (EVM), board design and layout techniques can be used to further reduce emissions in isolated systems. This application note discusses some of these methods. This document also discuss precautions during EMI testing to avoid spurious effects and how to measure the true performance of the system under test.

2 Use 3.3-V Input Supply Where Possible

The ISOW7841 supports both 3.3-V and 5-V input supply operation. Compared to 5-V operation, at 3.3-V operation the slew rates of the internal DC/DC converter are lower because of the lower voltage drive available to the power transistors. Lower slew rates reduce the common-mode current across the isolation barrier, leading to lower radiated emissions. As shown in Figure 4, the emissions with a 3.3-V input supply are much lower than with a 5-V supply. Where possible, TI recommends operating the ISOW7841 device with a 3.3-V input supply.

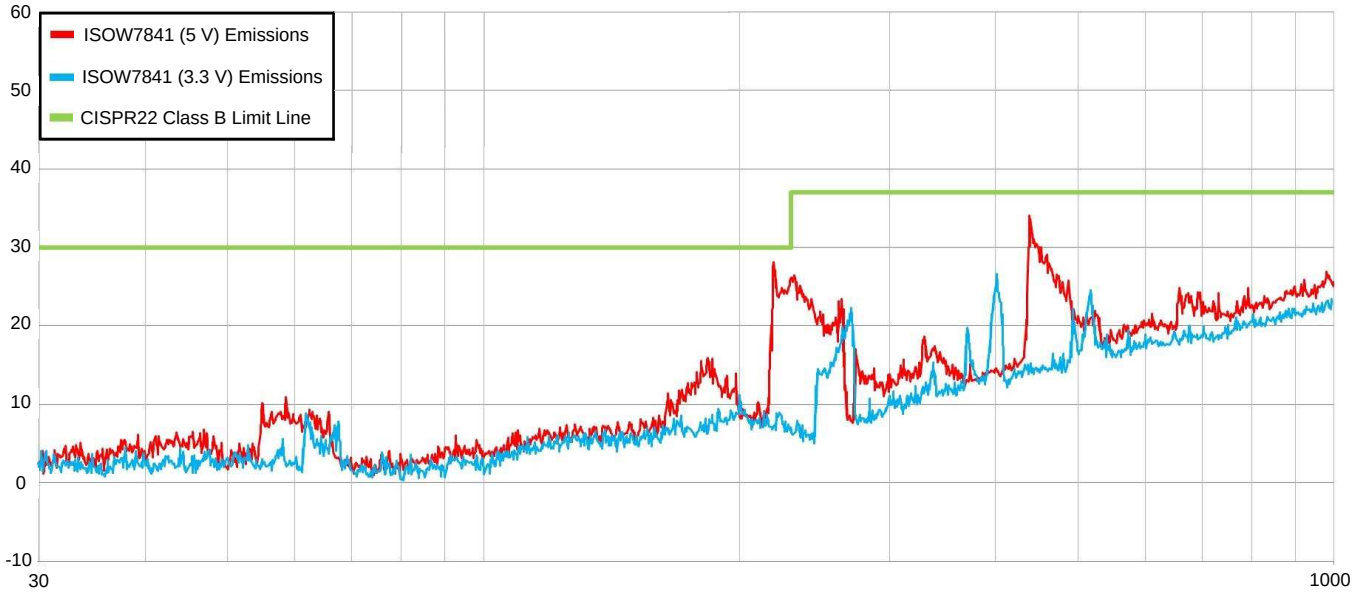


Figure 4. Radiated Emissions of ISOW7841 at 5-V Input vs at 3.3-V Input

3 Input and Output Decoupling Capacitors, Input Ballast Resistor, Ferrite Beads

The ISOW7841 device uses high-frequency switching to compensate for low transformer inductance, and also duty-cycles the power-converter to provide the required output DC load while maintaining regulation. Whenever the converter is on, a high current draw from the input supply, V_{CC}, occurs. This current has low-frequency content (roughly proportional to the closed-loop regulation bandwidth) and high-frequency content at the switching frequency and harmonics of the DC/DC converter.

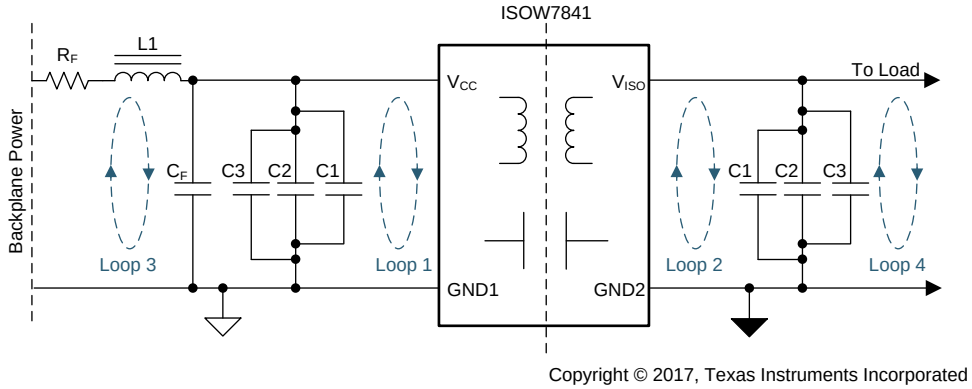


Figure 5. Supply Decoupling Capacitors and Input Ballasting Resistor

An input capacitor bank of different capacitors (C1 = 100 nF, C2 = 1 µF, C3 = 10 µF) at the input of the IC filters out a lot of the high-frequency content and prevents it from propagating to the backplane supply routing. Placing these capacitors as close to the IC (see Figure 5) as possible is critical to limit the area of loop 1. Place the smallest-value capacitor closest to the IC. A similar bank of capacitors placed on the output side filters out switching current on the secondary side of the DC-DC converter. Minimizing the area of loop 2 is important.

Despite the decoupling capacitors, the backplane supply routing can still draw some high-frequency and low-frequency current (a peak current of 100 s of milliamperes lasting several microseconds) depending on the output impedance of the supply network. If the input supply routing is long, a ballasting resistor (R_F) and an additional larger capacitor (C_F, 100 µF) can prevent current into the input supply routing (loop 3) leading to lower radiated emissions.

Figure 6 shows the image of the ISOW7841 evaluation module (EVM) and the placement of decoupling capacitors. In this layout, stitching vias along the board edge that connect all ground planes creates a Faraday shield. This shield prevents any radiation from noisy inner traces or planes.

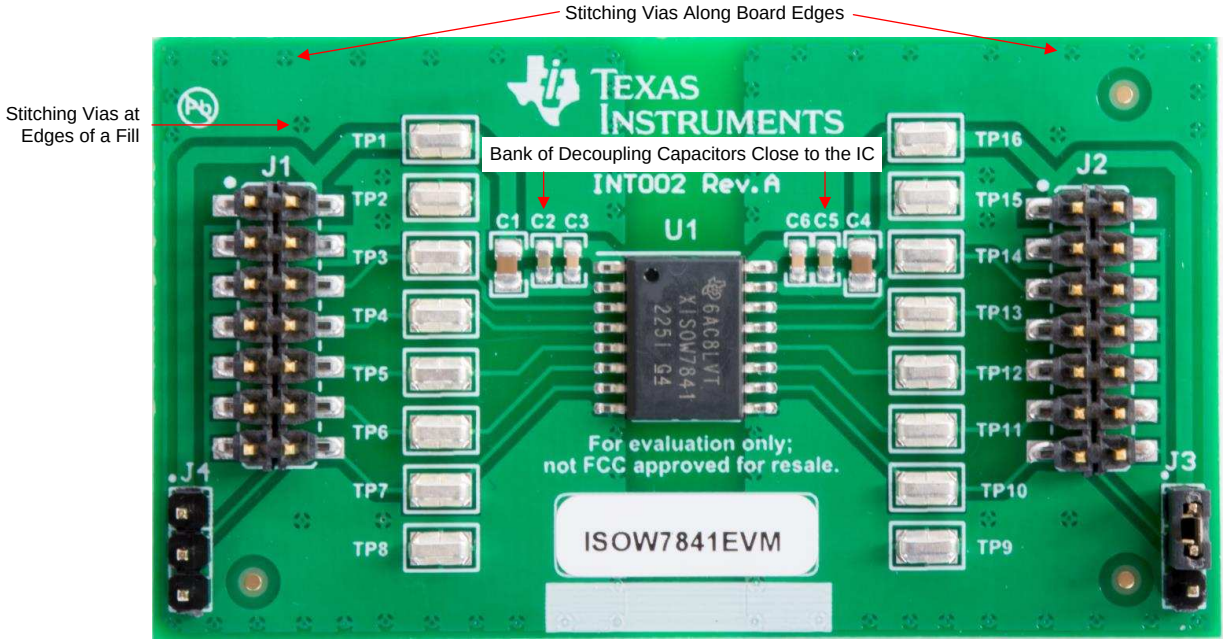


Figure 6. ISOW7841 Evaluation Module

4 Interlayer Side 1-to-Side 2 Capacitor

As previously discussed, the common-mode current from side 1 to side 2 and a large return loop are the main causes of emissions in isolated systems. One way of minimizing the current loop is to include a high-voltage capacitor from side 1 to side 2 and place it as close to the IC as possible as shown in Figure 7.

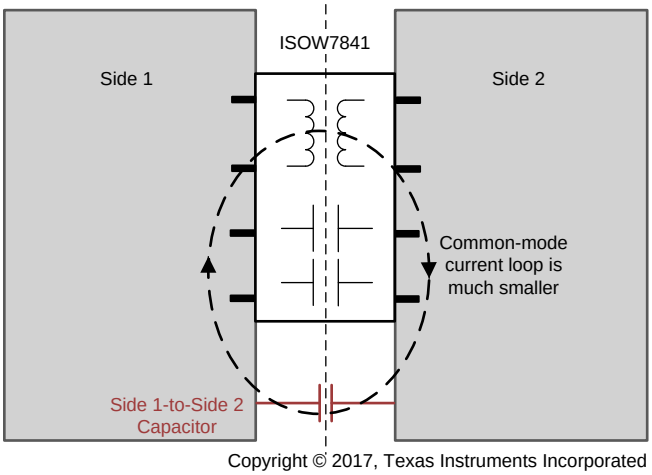


Figure 7. Side 1-to-Side 2 High-Voltage Capacitor Reduces the Common-Mode Current-Loop Area

The capacitors suitable for such use include high-voltage Y2 capacitors (surface-mount device [SMD] or leaded with appropriate creepage, or clearance levels) commonly used in power supplies. Using Y2 capacitors on the printed circuit board (PCB) introduces lead inductances on both sides of the capacitor, in addition to the parasitic inductance of the capacitor, making the capacitor ineffective at frequencies higher than 200 MHz. One way to create a low-inductance capacitance is by overlapping internal PCB layers.

Consider a four-layer PCB with the top layer for the signal, layer 2 for ground, layer 3 for V_{CC}, and the bottom layer for the signal. Because of system isolation, PCB layers are separated into two groups: side 1 layers (forming signal1, GND1, and V_{CC1}) and side 2 layers (forming signal2, GND2, and V_{CC2}). Extending the internal reference layers (GND and V_{CC}) on either side of the isolation barrier (as shown in Figure 8) creates an overlap of internal layers. This overlap area, formed by the extension of the GND1 and V_{CC2} layers with FR4 material between them acting as a dielectric, creates a stitching capacitance between GND1 and V_{CC2}. For fast transient common-mode currents, both GND and V_{CC} points are considered to be the same references (similar to AC analysis). Therefore, interlayer stitching capacitance forms between the reference points of side 1 and side 2. Figure 9 shows a 3-D representation of the interlayer stitching capacitance created in a four-layer PCB.

Use Equation 1 to calculate the equivalent capacitance formed between the sides.

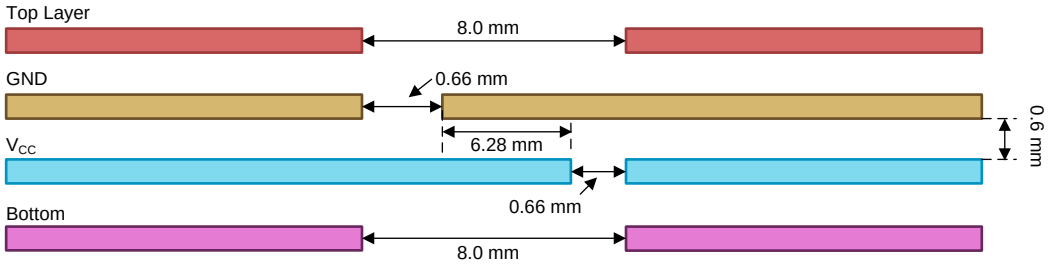
$$C_i = \epsilon \frac{A}{d} \tag{1}$$

where

- $\varepsilon = \varepsilon_o \varepsilon_r$
- C_i is the interlayer stitching capacitance.
- ε_o is the absolute permittivity of air (8.854 pF/m).
- ε_r is the relative permittivity of the dielectric (4.2 for FR4)
- A is the overlapping area.
- d is the distance between the GND and V_{CC} layers.

From Equation 1, solving for the interlayer stitching capacitance (C_i) for the PCB in Figure 9 would produce an approximate value of 30 pF.

Cross section:



Capacitance:

	K	Eo (F/m)	D (mm)	L (mm)	W (mm)	C (pF)
PCB	4.2	8.85E-12	0.6	77.3	6.28	30.09

Figure 8. Solving for C_i for the PCB in Figure 9 Using Equation 1

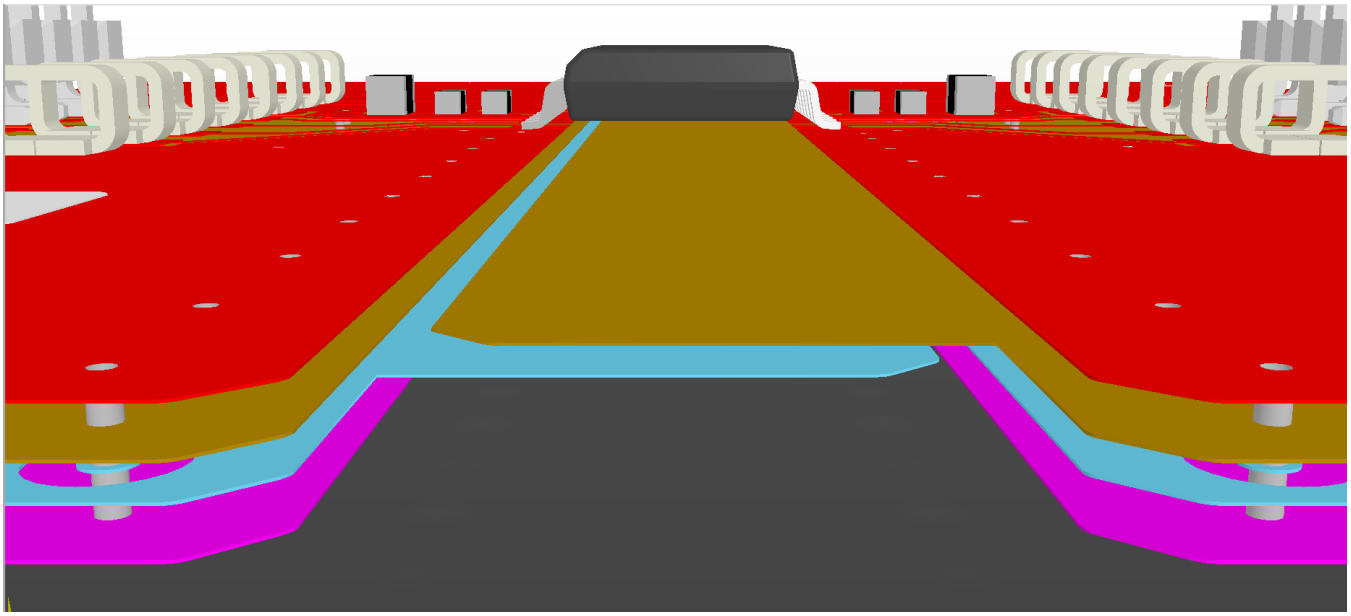


Figure 9. 3-D Diagram of PCB Layers With Interlayer Stitching Capacitance

Implementing a stitching capacitance across the isolation barrier with appropriate spacing is required to meet the overall isolation performance of the system. End-equipment electrical safety standards and working-voltage conditions determine these spacing requirements. Most system standards with functional or basic isolation do not have a minimum spacing requirement between the side 1 and side 2 layers on the same plane or on different planes. For such systems, using the lowest spacing between the overlapping area is best to achieve the highest capacitance value. Also consider the working voltage expected across the barrier and the dielectric strength of the insulation material.

Standards for safety systems and systems with reinforced isolation may require a minimum spacing between the side 1 and side 2 layers on both the same plane and on different planes. Allowing 0.4-mm spacing for systems less than 300 V_{RMS} and 0.6-mm spacing for 300-V_{RMS} to 600-V_{RMS} systems meets most standard requirements. Aside from these spacing requirements, standards organizations stipulate requirements on temporary overvoltages and surge voltages. For example, the International Electrotechnical Commission (IEC) 61010-1 mandates a 5 s withstand test of 3510 V_{RMS} and a surge or impulse test of 6400 V_{PK} for reinforced isolation from 300 V_{RMS} to 600 V_{RMS} mains voltage. The interlayer spacing must be designed to withstand these voltages, considering the dielectric strength of the insulation. For example, FR4 has a dielectric strength of 20 kV/mm.

Figure 10 shows the reduction in radiated emissions from the ISOW7841 device with the use of an interlayer stitching capacitance. With only a 30-pF capacitor between the two sides, an improvement of 10 dB to 20 dB is achieved. Higher stitching values can provide progressively higher attenuation in emissions.

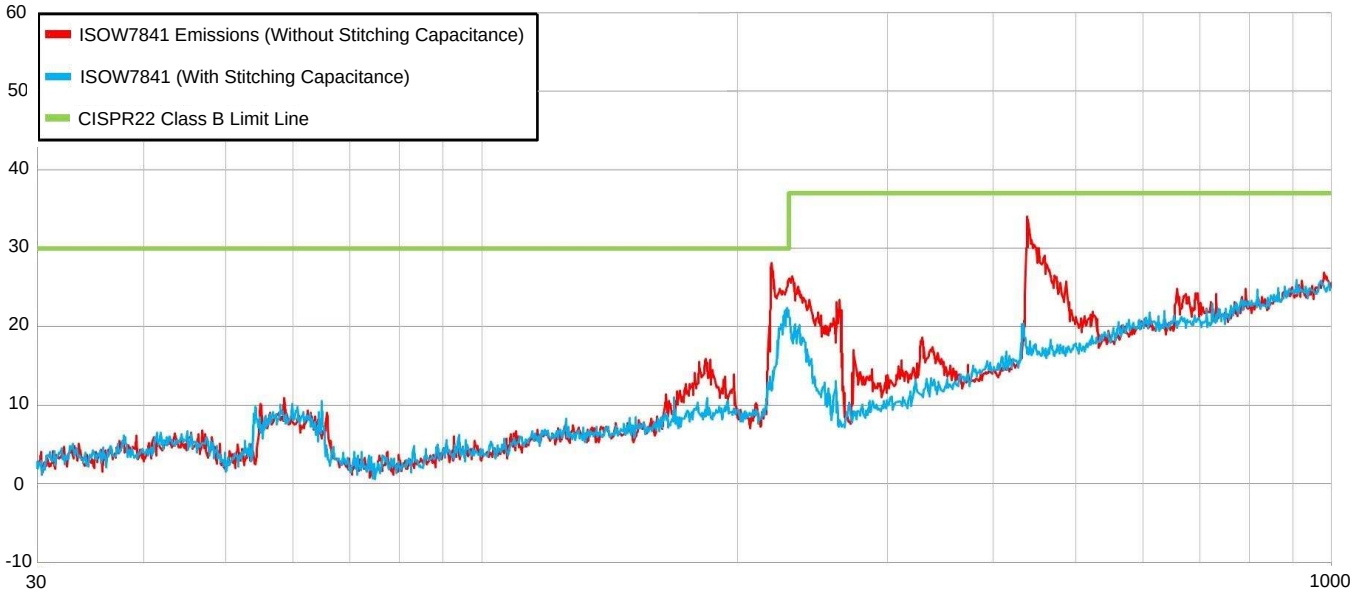


Figure 10. ISOW7841 Emissions With and Without a 30-pF Stitching Capacitance at a 5-V Input and 80-mA Load Current

Apart from maintaining the spacing across the barrier, extra care must be given at the edges of the PCB. At the edges, the planes can be exposed to air. Because opposite voltages come close to the edge of the board, these opposing voltages could lead to electric field stress and then air breakdown along the edge. Sharp edges and corners can also contribute to the air breaking down further because they increase the intensity of the electric field in the vicinity of the sharp edge, leading to a breakdown path for high-voltage impulse tests. To avoid such scenarios, pull in the inner layers at the edge of the PCB, and modify sharp edges into triangle-cut shapes, which will spread the charge density. Figure 11 shows an example of such an implementation. Rounding the corners and planes can also further enhance the solution.

Figure 11. Triangle Corners Implemented to Enhance High-Voltage Performance

While the inner layers of the PCB completely surrounded by dielectric allow relatively lower spacing (as previously discussed), the top and bottom signal layers must maintain much higher spacing. This spacing is based on the expected temporary overvoltage, impulse voltages, and environmental conditions such as altitude and pollution degree.

5 Direct and Capacitive Connection to Protection Earth

The controller or *cold* side of most isolated systems is connected to a system chassis that is then connected to protection earth (PE). This strong earth connection ties the controller-side ground to a stable point and reduces the conversion of common-mode noise to electromagnetic radiation in the system. Therefore, wherever possible, the control side of isolated systems should be strongly connected to protection earth.

The isolated ground of interfaces, such as analog and digital I/O modules and isolated RS485/CAN, can be AC connected to PE with the use of high-voltage safety capacitors. This capacitive connection is used to provide a return path to PE for ESD, surge, and EFT strikes on the bus and I/O cables. This connection also serves the purpose of reducing the common-mode noise on the isolated ground which reduces emissions through the interface and I/O cables.

Figure 12 shows an example of an isolated RS-485 system using the ISOW7841 device. The microcontroller ground is directly connected and the isolated ground is capacitively connected to PE, minimizing electromagnetic radiation from the input supply cables as well as from the RS-458 bus.

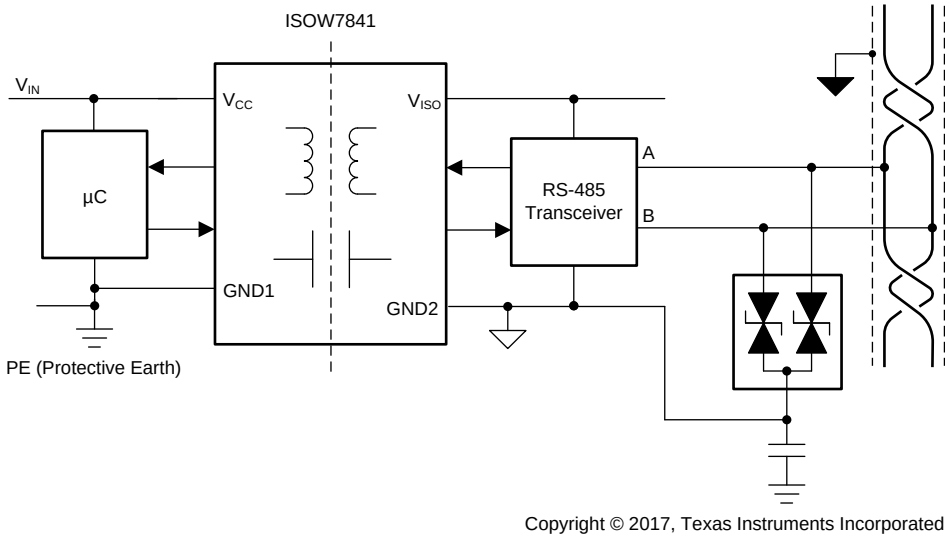
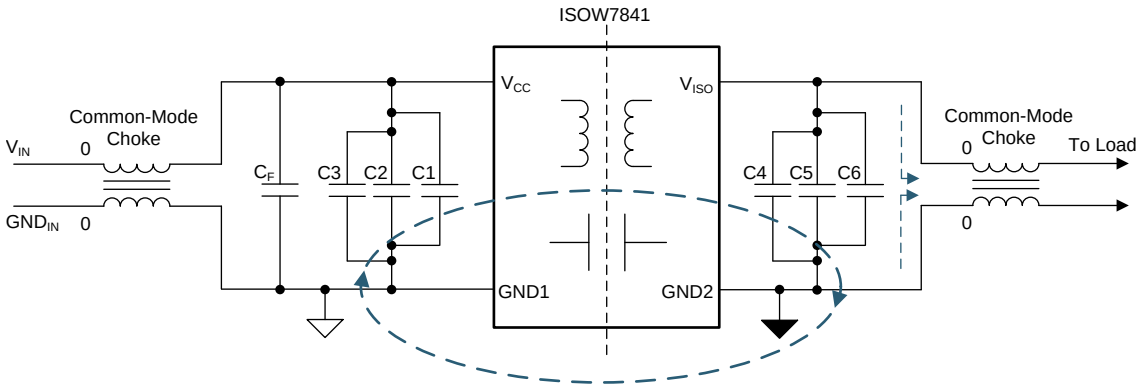


Figure 12. Direct and Capacitive Connection to PE in an Isolated RS-485 Application Using ISOW7841

6 Using Common-Mode Chokes

Long cables or wires connected to the system containing the ISOW7841 device can potentially pick up high-frequency switching noise from the convertor and act as transmitter antennas; longer cables result in higher radiation levels. The solution is to keep the common-mode current loop as small as possible and to keep the cables as short as possible. In case the system cannot avoid the presence of long cables and cannot provide a good connection between the ground and power earth or chassis, common-mode chokes (see Figure 13) can be used for attenuating the common-mode noise. For the ISOW7841 designs, a choke helps reduce the common-mode current as well as the return-path loop area, indirectly reducing radiated emissions. Common-mode chokes can be inserted on the input and output power supplies or on any long cables connected to the system.



(1) Any I/O cables should have common-mode choke with respect to GND.

Figure 13. Common-Mode Chokes on Input and Output Power Supply and I/O Lines Reduce Emissions

7 Precautions During EMI Measurements

When performing emissions measurements, make sure that only the emissions from the equipment under test (EUT) or device under test (DUT) are being measured and not emissions from other parts of the setup. While the following practices do not lower radiated emissions, they are critical to determining the true performance of the ISOW7841 device in the system under test.

The primary reason for radiation is the formation of antennas on the board. Long cables used to power up the system or probes used to measure any parameter can act like antennas and cause a higher emissions reading. The solution is simple: the setup used for emissions should closely mimic the final system conditions in which it will be operating. Properly shield all supporting equipment other than the system being tested with a Faraday shield.A box lined with a conductive metal, such as copper or aluminum, can serve as a Faraday shield. Keep cables connected to and originating from the system as short as possible, and keep the module to which the cables are connected within the Faraday shield. Any direct or capacitive connections of the board or metal shields to PE that are eventually planned for use in the final system must be present during EMI testing as well.

Figure 14 shows the setup used to measure the ISOW7841 emissions. The board containing the ISOW7841 device is exposed for measuring the radiated emissions. The cables connected to the board to power up the IC are as short as possible and in a tight twisted-pair configuration. The rest of the equipment—a 12-V battery and low-dropout regulator (LDO) in this case—are inside the black box and lined with aluminum foil to shield the components inside from the measurements. The cables connecting the LDO to the board are as short as possible and in a tight twisted-pair configuration. The cables extend out through a small hole at the top of the box. This hole is as small as possible to avoid compromising the effect of the Faraday shield.

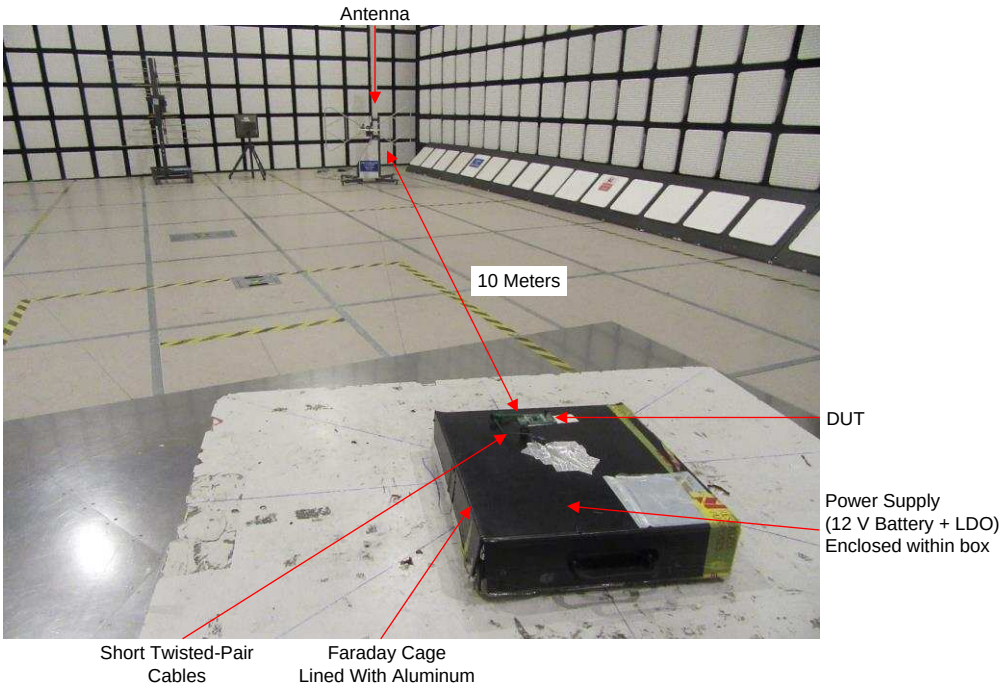


Figure 14. ISOW7841 Emissions Measurement Setup (CISPR 22)

If the supply connections are long wires coming from a power supply placed far away from the DUT, then common-mode chokes are recommended near the DUT so that the emissions are not unnecessarily enhanced by the long wires. By using common-mode chokes, emissions of the actual setup are measured and the effect of the long cables is nullified.

Any extra components required on the board, such as load resistors, must be soldered directly to the board rather than connecting them to the board using long wires.

8 Quasi-Peak versus Peak Detection

According to the CISPR 22 standard, the radiated emissions specification is specified as a quasi-peak limit, although the peak-detector measurement can typically be used to get a quick result.

The ISOW7841 device uses clock dithering to change the switching frequencies across a small band instead of concentrating all of the power at one single peak. Techniques such as this lower the peak scan levels and also show significantly better results when subjected to quasi-peak scans. At lower load operations, the power of radiated emissions is less because the DC/DC converter is on for a much shorter time compared to the full load condition. This lower power is reflected as a significant improvement in the quasi-peak results.

Texas Instruments recommends taking a peak-detector measurement first to find out the frequencies for the worst-case measurements. Then take a quasi-peak measurement at those frequencies to estimate the true margin from the CISPR 22B quasi-peak limit line.

Figure 15 shows the CISPR 22B measurement results with the ISOW7841 device. Up to 8.8-dB improvements occur with quasi-peak (QP) measurement compared to a peak-detector measurement.

	Frequency (MHz)	Polarization	Peak (dBuV/m)	QP (dBuV/m)	Improvement (dB)
ISOW7841 5 V to 3.3 V at 5 mA	240	H	18	11.8	6.2
	240	V	20	13	7
	465	V	32	24.5	7.5
	465	H	29	21	8
	676	H	39	30.2	8.8
	676	V	41	32.5	8.6
ISOW7841 5 V to 3.3 V at 80 mA	240	V	20	13.3	6.7
	240	H	19	13	6
	465	H	30	23.6	6.4
	465	V	32	26.3	5.7
	676	H	38	31.6	6.4
	676	V	40	34.5	5.5

Figure 15. Quasi Peak vs Peak Measurements With ISOW7841

9 Conclusion

The ISOW7841 integrated data and power isolator simplifies system designs and reduces board area. Through chip-design techniques, the ISOW7841 device reduces electromagnetic emissions by more than 15 dB when compared to competition solutions. However, techniques such as lower supply operation and the use of interlayer stitching capacitance, filters, and common-mode chokes can further reduce radiated emissions at the system level. Care should be taken during emissions measurement to measure the true performance of the system under test. Quasi-peak measurements result in lower readings than peak measurements, and should be used to assess the exact margin to the CISPR22B standard.

Read our blogs

- Optimize the emissions performance in your isolated system
- Small doesn't mean you compromise performance
- Cool down your industrial system design with integrated data and power isolation

10 References

- Read the How to isolate signal and power for an RS-485 system tech note for an example of isolated power and interface
- Read about advantages of using an integrated data and power isolation in the Fully integrated signal and power isolation – applications and benefits white paper.
- Texas Instruments, ISOW7841 High-Efficiency, Low-Emissions, Reinforced Digital Isolator With Integrated Power product folder
- Texas Instruments, 8-ch Isolated High Voltage Analog Input Module with ISOW7841 Reference Design
- Texas Instruments, Isolated RS-232 With Integrated Signal and Power Reference Design
- Texas Instruments, Size and Cost Optimized Binary Module Reference Design Using Digital Isolator with Integrated Power Reference Design

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2017) to A Revision	Page
• Changed the IEC specification number in the *Interlayer Side 1-to-Side 2 Capacitor* section	7

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