

Understanding LDO Performance in the TCAN4550-Q1

Richard Hubbard

ABSTRACT

To understand if a low-dropout (LDO) voltage regulator supports the system requirements, several factors have to be considered. Integrated LDOs present opportunities to reduce board space while at the same time presenting challenges for the system design. Package, ambient temperature input and output voltages must be considered when designing the system. In some devices, the LDO also supplies current to internal circuitry that limits the amount available externally. These contribute to the junction temperature of the semiconductor which determines the performance of the LDO. This application note considers the performance of the LDO that is integrated in the TCAN4550-Q1 in relationship to these factors.

Contents

1	Introduction	1
2	Device Overview	2
3	Device Description	2
4	Summary	6

List of Figures

1	Junction Temperature vs Ambient Temperature	3
2	Junction Temperature vs V _{sup} vs Ambient Temperature	3
3	I_{SUP} Current vs V _{SUP} vs Ambient Temperature with 60 Ω Load	4
4	I_{SUP} Current vs V _{SUP} vs Ambient Temperature with 50 Ω Load	4
5	LDO Output Voltage vs V _{SUP} vs Ambient Temperature	5
6	LDO Output Voltage vs V _{SUP} vs Ambient Temperature	5

List of Tables

1 TCAN4550-Q1 Performance 6

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

What is a low-dropout (LDO) voltage regulator? In the simplest terms, it is a component that takes a higher input direct current (DC) voltage and reduces this DC voltage to a level that the circuit requires. An example of this would be a 3.3 V regulator that is powered off of a 5 V system. There are many parameters that could be considered when evaluating an LDO. Examples are, but not limited too; input voltage, output voltage and current requirements, both internally and externally. LDOs are offered as a standalone device or integrated into a device that has more functionality. The TCAN4550-Q1 has an integrated 5 V LDO supplying current externally and to the integrated Control Area Network with Flexible Data Rate (CAN FD) transceiver and is the basis for this application note.

2 Device Overview

The TCAN4550-Q1 is a CAN FD controller and transceiver system basis chip (SBC) with an integrated 5 V LDO supplying current externally and to the integrated CAN transceiver supporting 12 V battery automotive systems. The LDO provides 5 V \pm 5% output externally and internally. The TCAN4550-Q1 device can source up to 125 mA of current. 70 mA of current is available externally because the CAN transceiver can need up to 50 mA during normal operation provided the design and certain constraints are understood. These factors include package, supply voltage and ambient temperature.

3 Device Description

The TCAN4550-Q1 has integrated a CAN FD controller along with a CAN FD transceiver. The device is powered from the battery supply (V_{SUP}) and integrates a 5 V LDO to provide 5 V tor the CAN FD transceiver. The LDO is capable of supplying 125 mA of current. The LDO also provides 5 V and required current, typically 50 mA, to the integrated CAN transceiver leaving 70 mA is available to the V_{CCOUT} pin. This type of configuration is typically called a self-power transceiver. The CAN transceiver can consume more current than the typical value provided under heavier loads or bus fault conditions. See the data sheet for the maximum values. This means what is left can be used by an external device.

The supply voltage, V_{SUP}, and ambient temperature, T_A, is considered first. As the output voltage, V_{CCOUT}, is fixed. A change in V_{SUP} can impact the overall LDO performance and thermal considerations. The equation ($V_{SUP} - V_{CCOUT}$) x I_{CCOUT} is used to arrive at the power consumption of the device. As an example, if $V_{SUP} = 28$ V, $V_{CCOUT} = 5$ V and $I_{CCOUT} = 125$ mA, then the power consumption of the device is 2.88 W. This is realized as heat which impacts the junction temperature, T_J, of the silicon. This power number is part of the evaluation to determine the impact to overall performance. Temperature is the next consideration as higher the ambient temperature means higher junction temperature. The theoretical junction temperature can be calculated by taking the calculated power and multiplying it with the package thermal resistance and adding the ambient temperature. Selecting the correct thermal resistance is application dependant. Factors to be considered are air flow, board, enclosure and system level thermal designs, see Semiconductor and IC Package Thermal Metrics for a more detailed description. For typical TCAN4550-Q1 applications, R_{BJA} is the parameter of focus. In the example above, the junction temperature is calculated using R_{eJA} = 35.25°C/W. R_{eJA} is the thermal resistance between the package and the ambient air surrounding the package, measured in change in degrees celsius per watt of power dissipation. For the TCAN4550-Q1 package the R_{BJA} value is 35.2°C/W which allows supporting higher currents with higher V_{SUP} or T_A .

$$(P \times R_{BJA}) + T_A = T_J \rightarrow (2.88 \text{ W} \times 35.2^{\circ}\text{C/W}) + 85^{\circ}\text{C} = 186.4^{\circ}\text{C}$$
(1)

This is above the maximum junction temperature of 150°C and results in a thermal shut down event as the T_J is above 160°C. Another thermal resistance parameter to consider is $R_{\theta JB}$ which is the thermal resistance between the silicon junction and the board. Using $R_{\theta JB} = 12.8°$ C/W provides a junction temperature of 121.9°C as an example of how proper thermal considerations can improve the performance of the LDO by using an optimized thermal design for the system. $R_{\theta JA}$ and $R_{\theta JB}$ are package and board design dependent and shown here for a high-k board. If best thermal practices are followed with airflow and heat sinks for the board; using $R_{\theta JB}$ provides higher performance but is beyond the scope of this application note. Packages, such as the RGY used by the TCAN4550-Q1, with thermal pads tend to have better $R_{\theta JB}$ performance than packages without.

When considering packages, the thermal characteristics are important to consider. Considering the list of thermal information in a data sheet one can see up to four thermal resistance parameters. These are important to understand as they contribute to the equation used to determine the silicon junction temperature which predicts when the device may reach the thermal shut down limit. For the TCAN4550-Q1 devices, the thermal resistance $R_{\theta JA}$ is considered. In automotive applications, the expectations is that the ambient temperature saturates the system; thus the $R_{\theta JA}$ is used to understand how the device performs.

The TCAN4550-Q1 is designed with a maximum junction temperature of 150° C and has a built in thermal shut down feature at 160° C. The junction temperature is the temperature the CMOS transistor junction should not exceed to meet long term reliability. The thermal shut down feature exists to protect the device in case an external fault causes the junction temperature to rise enough to damage the device. The three following charts show the theoretical junction temperature based upon V_{SUP}, ambient temperature and amount of current being sourced externally and internally. The graphs have two lines that represent the



www.ti.com

maximum junction temperature, dark green, and the rising temperature thermal shut down point, dark red. When the device is consistently operating in the temperature region between the maximum T_J and thermal shut down the life of the device may shorten. The application design should keep the junction temperature below the green line, maximum T_J . Figure 1 to Figure 2 show the theoretical performance with the 5 V output based upon a 125 mA and 100 mA external and internal load.



 $V_{cc} = 5 V at 125 mA Load$





 $V_{CC} = 5 V$ at 100 mA Load





Device Description

www.ti.com

The actual performance of the LDO aligns with the expected theoretical values when using the lab evaluation module and thermal stream that heats or cools the air around the device. Figure 3 and Figure 4 provide the data based upon 70 mA load at 5 V with CAN bus held dominant with a 60 Ω and 50 Ω load. Figure 5 and Figure 6 shows the V_{CCOUT} value under these same conditions.

Figure 3 shows the behavior of the 5 V LDO in relationship to I_{SUP}, V_{SUP}, LDO load of 70 mA, CAN bus dominant, CAN bus load of 60 Ω and ambient temperature. The I_{SUP} current is based upon a 70 mA load on V_{CCOUT} and the CAN bus held dominant which together comes out to about 120 mA. As can be seen, an ambient temperature of 125°C can cause a thermal shut down event when V_{SUP} reaches 20 V and V_{CCOUT} is providing 70 mA to a load. The load on the CAN bus is 60 Ω . When the CAN bus load is 50 Ω a V_{SUP} of 19 V can trigger the same decrease.

The reason the curve shows I_{SUP} dropping off is due to the internal junction temperature T_J exceeding the thermal shut down temperature. At this point, the LDO and CAN transceiver are turned off. Even though the figure shows the current leveling off to approximately 74.5 mA; in reality it drops to the μ A area. This is happening in milliseconds and cools down prior the $t_{UV/TSD}$ timer expiring, which would put the device into sleep mode. As the junction temperature drops below thermal shut down point of 150°C the device enters standby mode. As the 70 mA load was still connected, I_{SUP} shows this current plus the normal standby current which is approximately 4.5 mA. As this is happening quickly, the figures do not show the drop to microamps but shows I_{SUP} leveling out to 74.5 mA. If the TSD event is prolonged, the current drops to microamps and V_{CCOUT} drops to 0 V once the decoupling capacitor discharges. When there is 50 Ω bus load this can also happen at 105°C when V_{SUP} is at 29 V as seen in Figure 4



Figure 3. I_{\text{SUP}} Current vs V_{\text{SUP}} vs Ambient Temperature with 60 Ω Load



www.ti.com









 I_{VCCOUT} Load = 70 mA

CANH and CANL Load = 60 Ω









4 Summary

6

The LDO in the TCAN4550-Q1 can supply 5 V at 125 mA. As the LDO supplies the CAN transceiver, not all of the 125 mA can be utilized by an external load. When considering LDO sourcing requirements, expected system behavior needs to be considered when a CAN bus fault takes place, requiring more current to the CAN transceiver. If the expected behavior is no interruption to the load, then supporting a reduced I_{CCOUT} load is warranted. A reasonable trade off would be a 50 mA load on V_{CCOUT} with normal CAN bus operating conditions. For the best performance, special care must be taken to design a board and system that meets the thermal needs. For devices that have thermal pads, the thermal pad must be soldered to a good solid ground plan. Based upon the data, Table 1 provides typical performance for specific data points.

Device	V _{CCOUT} (V)	I _{CCOUT} (mA)	V _{SUP} (V)	T _A (°C)
TCAN4550-Q1	5	70	14	105

TEXAS

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2022, Texas Instruments Incorporated