Application Report
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Optimizing Gate Driver Layout for LiDAR Applications

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ABSTRACT

Lidar is an evolving light radar technology that is making advanced, innovative laser applications possible. The gate driver and FET play a major role in maximizing laser performance. New FET technologies make laser pulsing solutions faster, smaller, and therefore make Lidar more practical for every day applications. The gate driver and GaN FET can be 5 to 10 times faster than a buffer and MOSFET which can result in much higher resolution for Lidar. There are three typical components to the laser pulse circuit:

- A high-speed **Gate Driver**
- A compact, low gate charge **FET**
- A High-Power **IR LED**

Many unplanned issues can come up when designing for the peak current or power of the laser. In order to have a high performance laser driver, there needs to be an optimal PCB layout. Optimized laser driver PCB layout can be achieved with the right component placement and routing techniques. The gate drive circuit must have excellent PCB layout to achieve fast rise and fall times on the gate and drain of the FET and low switch-node jitter for high Lidar resolution. A Lidar system, shown in Figure 1, highlights how the laser driver interacts with the Lidar system. The *LMG1020* and *LMG1025-Q1* gate drivers both have the ability to improve laser driver performance. This helps achieve nanosecond laser pulses at high peak power for sufficient Lidar distance and resolution.

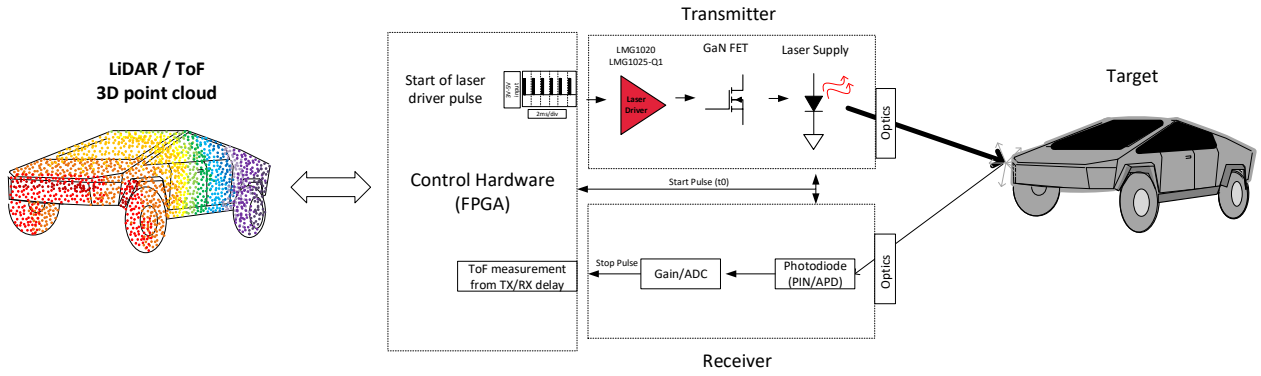

Figure 1. Automotive Lidar / Time of Flight (ToF) System Block Diagram

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1 Importance of peak laser current measurement

Typically, a DC voltage is pulsed by the GaN FET to the switch-node where the laser diode sees the full VBUS voltage minus the forward voltage drop of the laser. A high performance laser driver circuit supplies high Ipeak current to the laser shown in Figure 2. To achieve the highest peak laser light power, the highest peak laser current should occur. When measuring the laser output, just relying on the peak current is not enough. The laser optical power needs to be read with a sufficient gain and noise immune photodetector. Only then will the laser output measurement become accurate. Measuring the output of each laser pulse is useful for peak current-limiting the laser for eye safety. This can be achieved by measuring the average optical power reading and the half power bandwidth of the optical pulse width to obtain the peak optical power of each pulse. A current sense resistor can then be accurately implemented after optical to electrical power calibration. A current sense resistor adds to the power loop inductance and can throw off the peak readings shown in Figure 4.

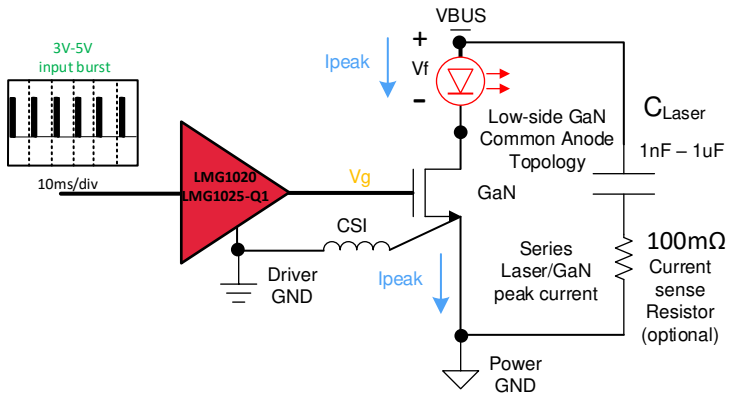

Figure 2. Typical Low-Side Laser Drive Circuit

2 How to drive common cathode laser

A high power, stacked laser diode should not be used for long range Autonomous Vehicle Lidar due to high beam divergence and therefore low long distance resolution. Instead, multiple lasers are connected in parallel and have their metal lead-frames connected to the anode or to the cathode. The metal is connected to ground to help with thermals. This makes two power laser driver topologies or grounding configurations: common anode and common cathode. The configuration is called common anode because if multiple laser diodes are added in parallel their anodes would need to be touching or common. Likewise, the other laser topology would be common cathode, shown in Figure 3, and would require a high-side

driver to switch a high-side GaN FET. Since the laser is connected to ground with the common cathode configuration, there can be a large ground plane to help with temperature rise. To maintain a long laser life time, lasers typically dissipate 50 % of the pulse energy as heat and 50 % as optical power. Lasers can be reliable through out their life-time so long as temperatures and driver oscillations are minimized. An optimized layout also helps with laser circuit oscillations that contribute to higher temperatures.

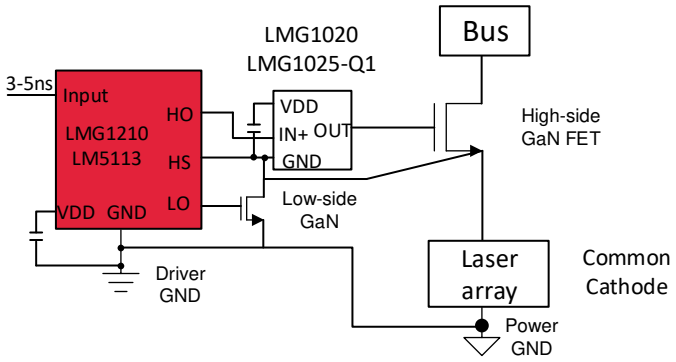

Figure 3. common cathode Configuration Using High and Low-Side Drivers

For the common cathode configuration, the LMG1210 or LM5113 half-bridge gate drivers can be used as the level shifter and LMG1020 or LMG1025-Q1 can be used as the buffered high-side driver where the VDD pin is riding on the switch-node. This circuit is useful for 4 - 5 ns pulses due to the minimum input pulse width capability of the high-side driver. The low-side portion of the driver is also used to quickly switch another FET to replenish the bootstrap cap or in this case the LMG1020 or LMG1025-Q1 VDD cap.

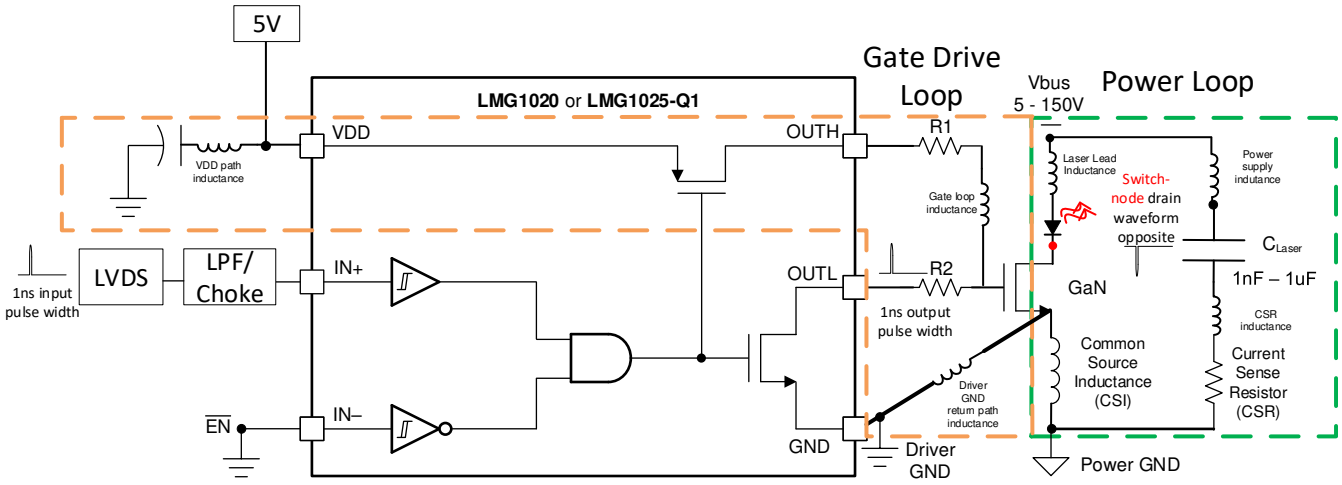

Figure 4. common anode Laser Driver Gate Loop and Power Loop

3 How to control peak laser current

Lidar requires high frequency burst mode or high PRF (Pulse Repetition Frequency) pulsing to keep average laser current low for thermals, efficiency, and eye safety. The shorter the laser pulse the steeper the current slope needs be to achieve the same peak laser current or same Lidar distance. This is why PCB inductance needs to be minimized as much as possible, so that its peak current slope will not flatted by more power or gate loop inductance. Due to the high voltage and resonant circuit the switch-node waveform can have a very high slew rate. A high dv/dt on the switch-node is due to a high di/dt as well. To achieve the highest Ipeak, for the same laser pulse width, the gate pulse should have the fastest rise and fall time as shown in Figure 5. That way, Ipeak begins sooner and reaches a higher peak value for the same pulse width measurement.

Although a higher Ipeak is needed for higher laser power, its also important to keep the power under a certain limit for safety. At high power, light can bounce off a surface in any direction and it does not have to be visible to cause harm to the human eye. There are four potential ways to limit peak laser power and quickly kill signal and power to the laser in order to maximize eye safety:

- Use a peak laser power calibrated current sense resistor
- Use less bus capacitance or lower bus voltage to achieve less peak laser current
- Limit the gate driver rise time and pulse width to a fixed value
- Design a PCB purposefully limited by inductance and dampened by resistance

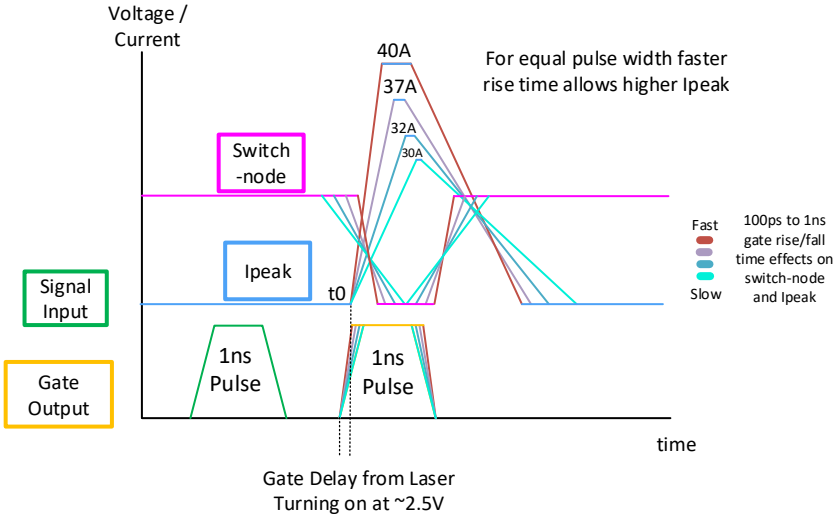

Figure 5. Gate Drive Rise and Fall Effects

4 How to optimize layout with the LMG1020 gate driver

When doing GaN layout, it's important to remember the gate current needed to charge the gate uses the same return path that is used to discharge the gate. Since trace inductance is proportional to the entire current loop, if the loop area is reduced so is the inductance. To help explain the PCB layout Figure 6 shows a schematic view of the important loops in the *TI Designs: TIDA-01573 Nanosecond Laser Driver Reference Design for LiDAR* . For more layout details on the TIDA-01573, see the Design Considerations section 2.2 from *TI Designs: TIDA-01573 Nanosecond Laser Driver Reference Design for LiDAR* .

The following considerations help achieve an optimized layout, higher laser power and less ringing for better EMI and thermals:

- Component placement of the GaN FET and gate driver
- PCB layout effects for a 1 ns pulse
- Kelvin connection ground plane
- Trace length / width and routing (including laser leads)
- VDD / VBUS optimal capacitor placement
- Parallel gate/return paths to minimize oscillations
- PCB layout effects on Pulse Width Distortion (PWD)

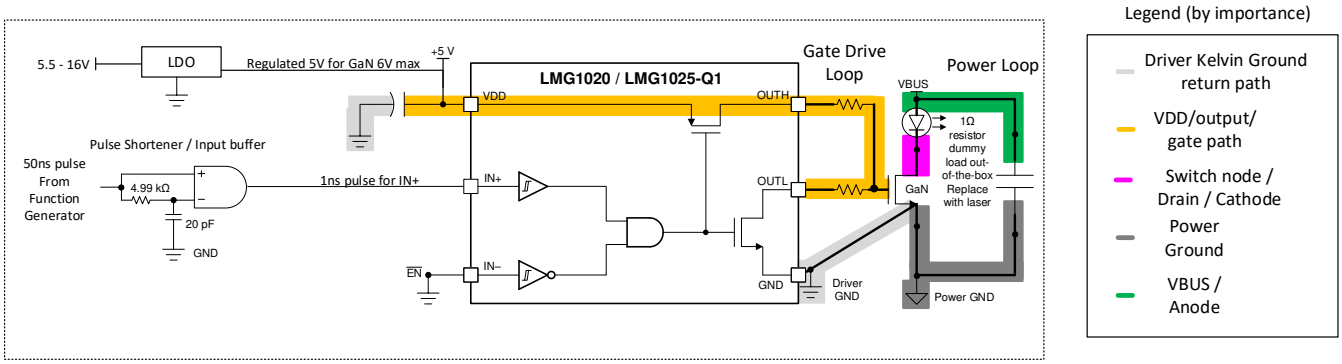

Figure 6. LMG1020EVM-006 Essential Gate Loops Colored System Block Diagram

4.1 Driver and GaN component placement and routing

The key to an optimized layout is to place the components, while keeping in mind gate and power loops, in such a way that allows the shortest and widest connection possible. A short trace length is more important than a wide trace width since they are directly proportional. On a wire of equal area, there is more trace inductance for a long wire vs a skinny wire. Doubling the trace width does not half the trace inductance. For the lowest inductance connection, put the gate driver, GaN FET, and laser on the top layer in the smallest area and connect the return paths on the adjacent layer 5 mil deep with in-pad microvias to take advantage of vertical current extraction. 90 degree trace connection should be avoided and replaced with two 45 degree angles or a smooth transition for the magnetic fields to follow. Varying magnetic fields causes varying electric fields which can cause EMI.

Understanding the high current gate and power loops on the schematic and PCB can help achieve better layout. The driver, GaN, and laser placement combination can affect the laser performance. In Figure 7, the EPC2019 and EPC2016 are used to show how a low inductance package GaN FET and LMG102x driver can be placed to drive the laser most efficiently. FET selection is important to achieving a good gate loop. With the EPC2019, the driver and VDD cap are placed in-line and equal length with each other to achieve parallel gate loop paths. This is optimal for the lowest loop inductance, noise as well as fast rise times. With the EPC2016, the power loop and gate loops are separated by 90 degrees. However the drain to source current direction, due to the pinout of the GaN FET, is aligned with the FET. This loop alignment results in a decrease in power loop inductance.

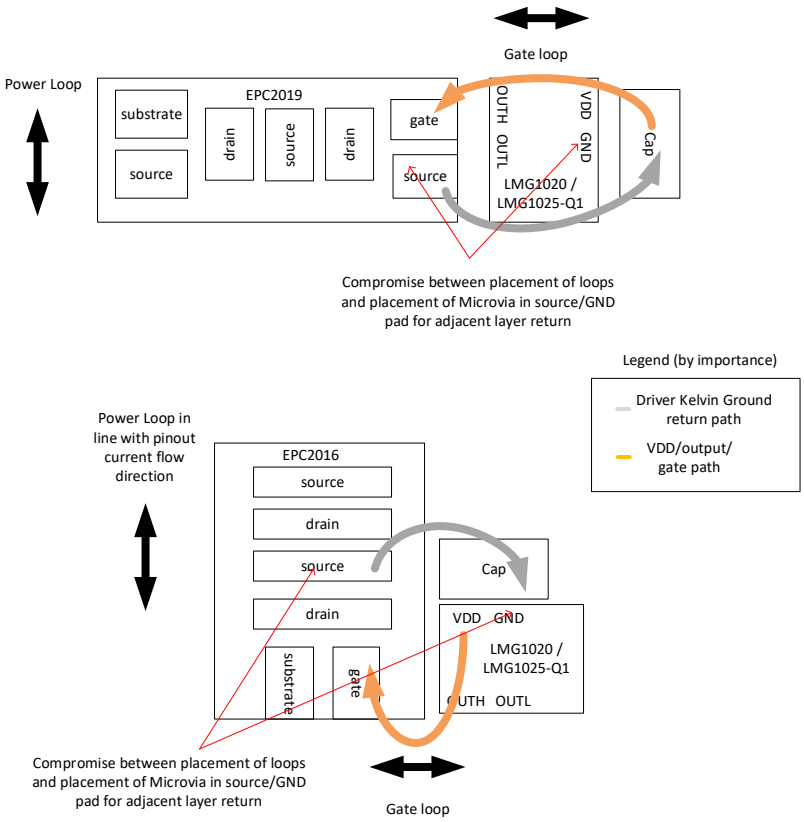

Figure 7. EPC GaN and Gate Driver Placement

4.2 Effects of PCB layout on 1 ns pulse

When comparing LMG1020 and LMG1025-Q1, the device package is the most differentiating feature. Although the package pin inductance adds a few 100 pH of inductance between WCSP and QFN, the rise and fall times are similar. The package difference only effects solution size, not laser driver performance. When comparing the EVM's, the overall results are very similar but have a difference in the peak gate voltage and VDD dip. These differences exist because of the difference in loop inductance due to the package sizes as well as substrate to source connection due to pinouts. The clamping diode affects the gate loop of the LMG1025-Q1 EVM and not the LMG1020 EVM because of the different FET used. The LMG1025-Q1 EVM uses the EPC2212, in which the pinout has the substrate pin where the gate return pin should be. This can prevent a low inductance substrate and source return connection. Due to these clamping diode affects, there is a higher trace inductance from the substrate connection on the LMG1025-Q1 EVM, shown in Figure 8. This substrate connection couples oscillations from the power loop to the gate loop, and lowers the driver GND as well as the VDD drive voltage shown in Figure 8. A clamping diode can be used but must not impede the power or gate loop performance. Placement on the bottom side of the board may be a trade off for performance of the gate loop and clamping action.

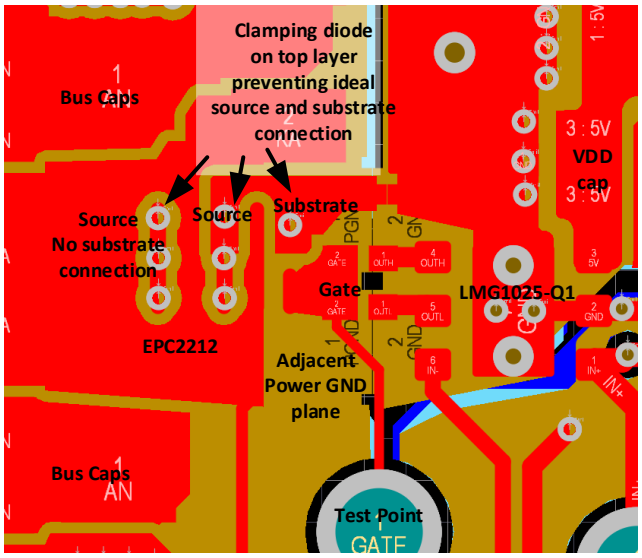

Figure 8. LMG1025-Q1EVM Substrate Connection

Figure 9 shows LMG1020 and LMG1025-Q1 EVM performance comparison with equal 1 ns pulses at 70 V. The purpose of this comparison is to show that with two similar but different driver and FET layouts, both LMG1020 and LMG1025-Q1 can achieve 1 ns high voltage laser pulses. Such a high voltage can be achieved with a capacitively resonant circuit only when the laser pulses are 1 - 2 ns, to keep average current and thermals low. The rise and fall time is typically measured from 1V to 4V exactly. Due to ground lifting, as shown in the max gate voltage in Figure 9, measurement is therefore taken from a percentage of the max. 20 - 80 % rise and fall time and 50 - 50% for pulse width.

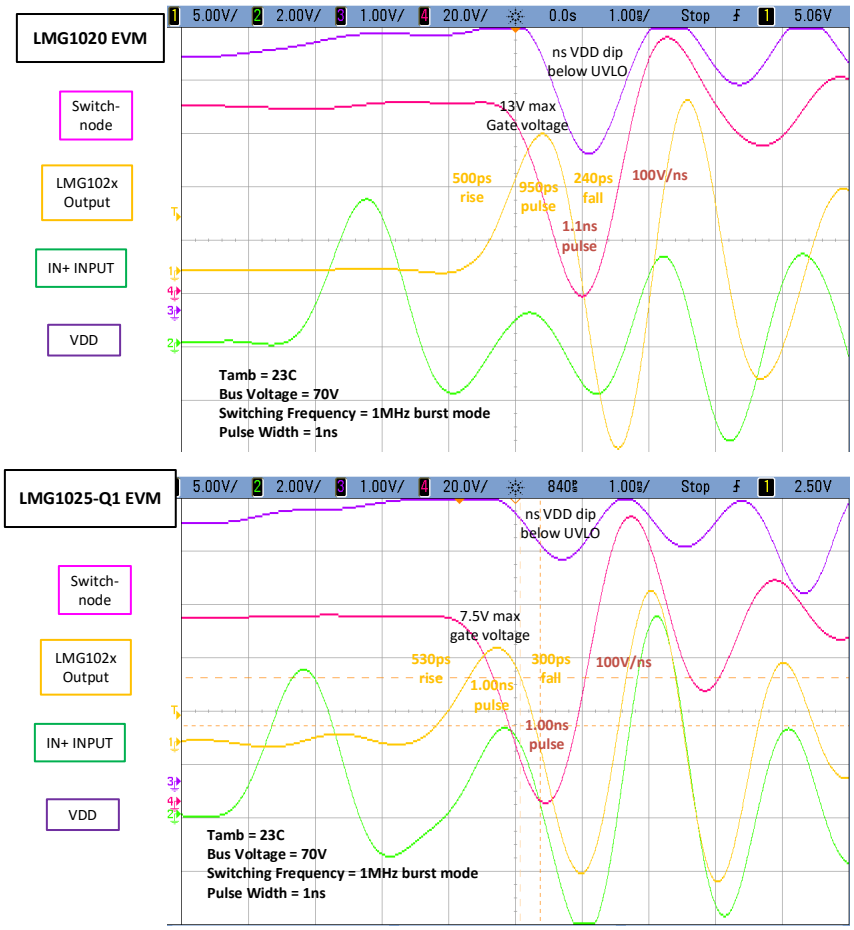

Figure 9. LMG1020 and LMG1025-Q1 EVM 1 ns Performance Comparison

To optimally switch the laser at peak efficiency it needs to be switched with an nanosecond pulse width or impulse. This high slew rate on the GaN drain excites parasitic loop inductance and gets coupled to the laser as well as the gate loop. The effects of the PCB coupling and gate drive performance are more apparent for higher voltage pulses. It is possible for the ringing on the gate to manifest into a double pulsing of the laser accidentally, or the gate voltage oscillation increases during switch-node rise time shown in Figure 11 and Figure 9. The larger gate pulse during the second oscillation could cause a double laser pulse, increase rise and fall times, and corrupt the input signal.

4.3 Ground plane: achieving a kelvin gate connection with microvias

The most overlooked connection is the kelvin connection from power ground back to driver ground. Figure 12 clearly shows power ground and driver ground separated to help achieve a good kelvin connection and remove power loop noise coupling as much as possible. There is not much dark gray or light gray around the gate loop on the top layer because microvias are placed in-pad to reduce unnecessary Common Source Inductance (CSI) or long gate return path length. The way to achieve an optimal kelvin connection is for the power ground plane to connect to the driver pins at one point as close to the component pins as possible, shown in Figure 10.

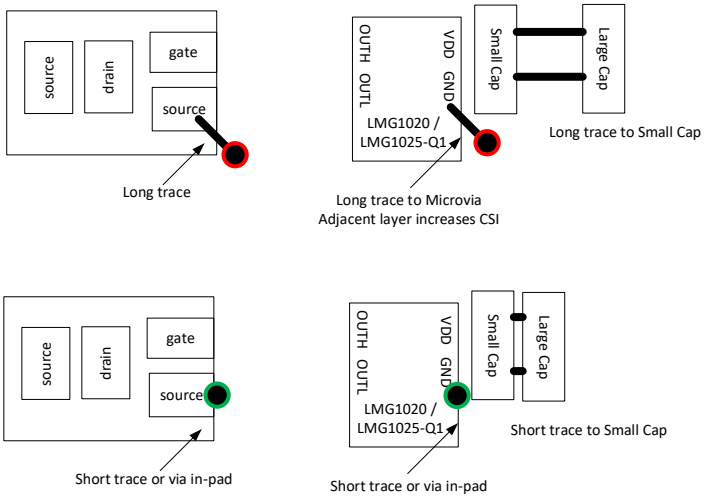

Figure 10. Correct Microvia in-pad return connection in green

If the vias are not placed close to the driver pin and FET pin, CSI can cause the gate voltage to fall as the switch node experiences high dv/di/dt, as shown in Figure 11. If the gate voltage falls close to UVLO when the gate is first turned on, the drivers high peak source current pulls down the VDD cap voltage. The GaN is not driven to saturation, which causes the following issues:

- Thermals - add thermal vias, more copper, layers, and trace width
- Oscillations - achieve smaller layout loop area
- EMI - add gate resistor and remove potential antennas

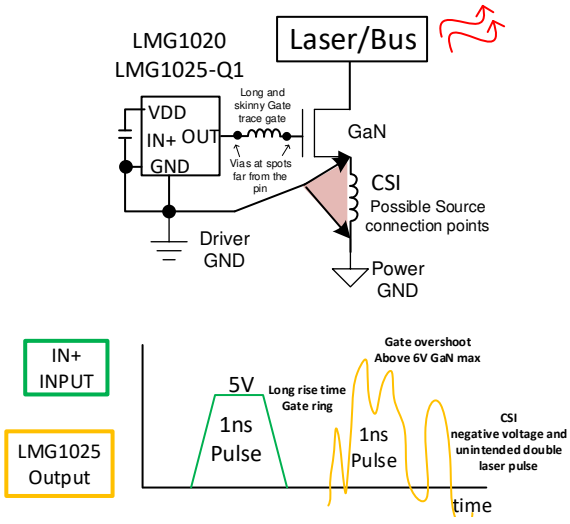

Figure 11. Long Gate Trace and CSI Affects

High oscillations can also be an issue for long input traces which act like antennas and pick up lower frequency noise. An input buffer, and low-pass filter close to the driver input pin is often necessary to keep edges clean and sharp from controller to driver input. And if the common source inductance (CSI) is not mitigated by a good source or kelvin ground connection the driver ground can be affected and corrupt the input signal pulses. To mitigate the power loop from affecting the gate loop, a LVDS interface and low-pass filters can be used, shown in Figure 4.

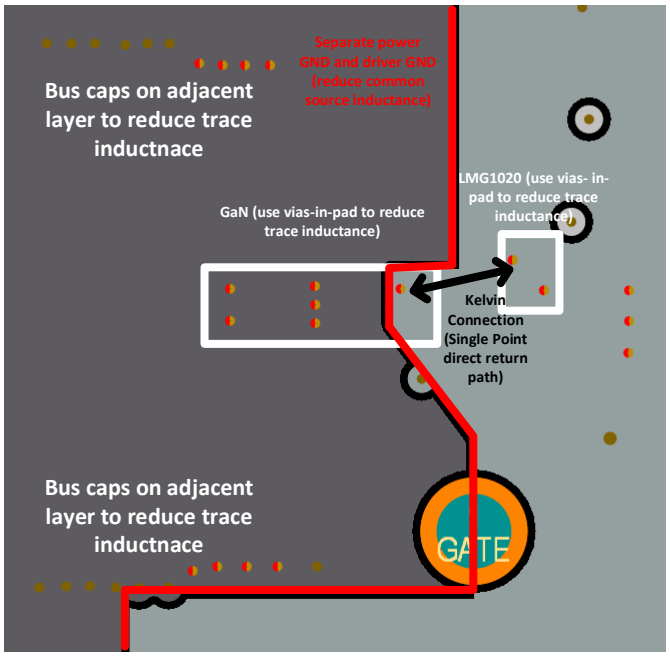

Figure 12. LMG1020EVM-006 Adjacent Layer Layout

4.4 How laser lead length can effect laser turn off time

The switch-node of the GaN can see long fall times even with a fast gate fall time. A long laser turn off time can be due to overshoot from the high Ipeak current still flowing through the FET during turn off. As a rule of thumb, every inch of slender wire is about 20 nH of trace inductance. To reduce this inductance, reduce the trace length rather than increase the width. Long laser leads contribute greatly to power loop inductance and can especially be seen when turning the laser off. This can prevent nanosecond light pulses and give a less precise light beam. Figure 13 shows the affects of a resistive dummy load on LMG1025-Q1 EVM with 2 inch leads vs 1 inch leads shows how the laser pulse width can be reduced with the right laser package leads.

- 2" each leads give 5 ns pulses
- 1" each leads give 3 ns pulses
- No leads give 1 ns pulses

Since light travels 1 ft in 1 ns, and each inch of laser leads gives an extra 2 ns pulse width, then the laser leads can contribute 2 ft or more to the resolution error than the laser driver itself.

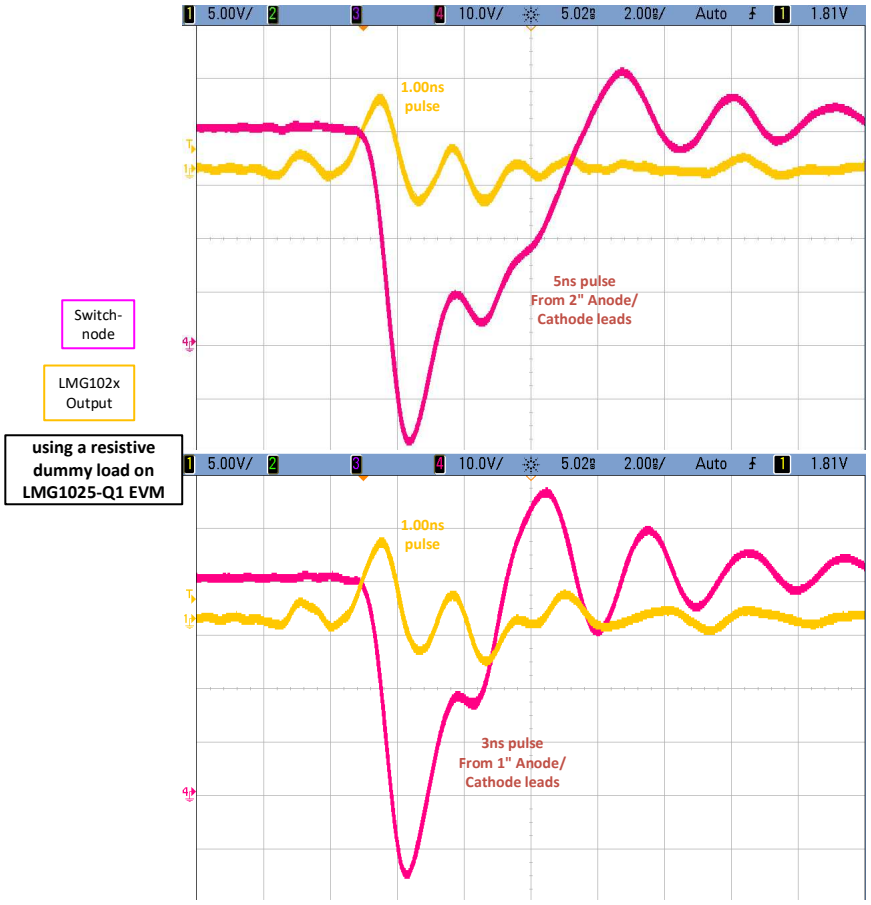

Figure 13. Laser lead affects with 1 ns 40V pulse

4.5 How to Prevent Oscillations on VDD

The laser driver ground plane is noisy, since high current is being switched on and off very quickly. A VDD cap placed close to the pins helps filter out and block much of the power ground noise that leaks into the driver ground affecting VDD. Since high peak currents are used, the shortest and widest connections are needed for VDD. Perhaps the most important part of the gate loop is the VDD capacitor to driver inductance. Place the VDD cap 50 - 100 mil from the driver output pin, shown in Figure 14. A wide body or feed through cap has the lowest lead inductance, however a regular X7R can also be used for low cost. 100 - 500 nF can be placed closest to the pins for peak sourcing current, and a parallel 1 - 2 uF can be used to hold VDD steady. With more nH of power loop inductance there could be more nH of gate loop inductance from CSI. 1 nH of gate loop CSI could mean a 5 V of ground lifting for a 5 A current peak, which could work against the VDD drive voltage during turn off, increasing the gate fall time. The higher switch-node dv/dt the lower VDD dip and in some cases VDD can ring below UVLO although in many cases, not long enough to trigger it, shown in Figure 9.

To prevent UVLO chattering, make sure the distance between both VDD caps to the driver pins are as close as possible, shown in Figure 10. High oscillations producing high negative voltage on the pin should also be considered, although negative oscillations of 1 - 2 ns are not long enough to turn on internal parasitic diodes and are not a major concern. Undershoot as well as overshoot can be an issue if the excursion above the max or min spec is longer than a few nanoseconds. VDD, gate and drain undershoot and overshoot should be kept under max and min spec and can be avoided with good PCB layout.

4.6 How to layout parallel FETs or Lasers

In many laser solutions, multiple lasers are fired at the same time or consecutively. With nanosecond pulses of multiple FETs and lasers, one GaN or laser can turn on before the other which creates an out of sync light pulse, lost data point or damage to the GaN. More channels brings more routing complexity and greater chance for EMI. Connections should be close to equal trace length to limit part-to-part or gate-to-gate delay variation, as well as have symmetry for magnetic and electric field canceling if possible. Canceling magnetic fields from parallel gate and return paths also removes parasitic trace inductance and can be easily accomplished with a ground plane.

To streamline layout design, for a very high-frequency parallel or multi-channel laser driver, the connection, and placement can be duplicated. In parallel laser systems, the gate length is often too long which can create oscillations. For each laser channel, the length from the driver output to the GaN gate, and GaN to the laser, as well as the laser PCB pad to the laser pins, must be very short and similar width and length.

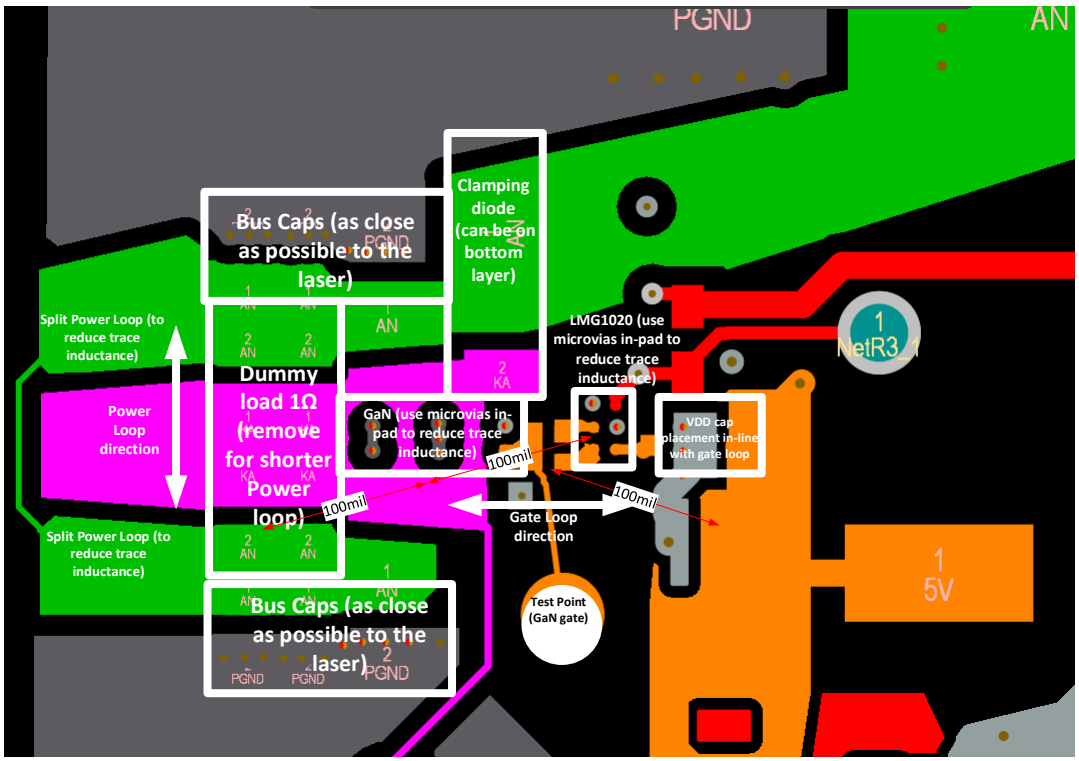

Figure 14. LMG1020EVM-006 Top Layer Layout

Gate resistors can be used to limit overshoot from long gate traces but they will also slow down the maximum operating frequency. They will also contribute to longer rise and fall times due to a larger gate loop. The turn-on gate resistor can be easily used with LMG102x's split output to avoid overshoot. The maximum GaN gate voltage is 6 V, so a gate resistor dampens oscillations and excessive switch node dv/dt to help with overshoot, undershoot and EMI. If a gate resistor is used, start at a low resistance value and work up to a nice balance between fast rise time and less ringing. A 4-layer board can be used to help separate noise from coupling back to the input from the gate driver and power loops. More layers helps with low-inductance loops and high-frequency performance and can be added when paralleling more FETs or more lasers.

4.7 Effects of PCB layout on PWD

Propagation delay needs to be short and consistent to achieve short pulse width and minimum delay before t0 or at the start of the pulse. For reducing this pulse width variation or jitter the GaN to laser connection, as well as the laser leads to the PCB, should be very low inductance. A split power loop with adjacent layer bus cap return path can also help with faster laser turn off times. The pulse width needs to be consistent to achieve more resolution for more accurate ToF calculation. To better understand the max pulse width variation over temperature and time, a different measurement is used featuring the persistence of the scope shown in Figure 15. The largest pulse width variation is also known as the Pulse Width Distortion (PWD) or positive pulse distortion, as referred to in the datasheet. PWD is from input to output of the gate driver where jitter can be due to loop inductance effects on the switch-node. Jitter measurements must be taken with a 1 GHz, or finer resolution scope with minimal interaction between possible antennas such as cables and connection points. The input signal should have very fast rise and fall time to avoid threshold variation. To achieve this, another LMG1020 or LMG1025-Q1 can be used to drive the inputs. There is 200 ps PWD from the function generator to the driver output. There is also 300 ps of switch-node jitter from high voltage operation, and power and gate loop inductance.

Lidar requires exact timing since it's a race with the speed of light to start and stop the pulse as accurately as possible. For high performance Lidar, distance resolution can be in centimeters, as shown in nanosecond ToF values in Equation 1.

$$\text{Distance\_one-way} = (\text{Speed of Light} / 2) * \text{Time of Flight} \quad (1)$$

The max PWD, from the *LMG1025-Q1* output, with a 105 C ambient temperature is 220 ps. Therefore, with a mean pulse width value of 1.00 ns, the PWD could make the mean pulse width 890 ps min to 1.11 ns max. Since 1 ns means 30 cm or 1 ft of light traveled, shown in Equation 1 then 220 ps of jitter means 6.6 cm of more resolution can be gained with less input to output laser driver jitter.

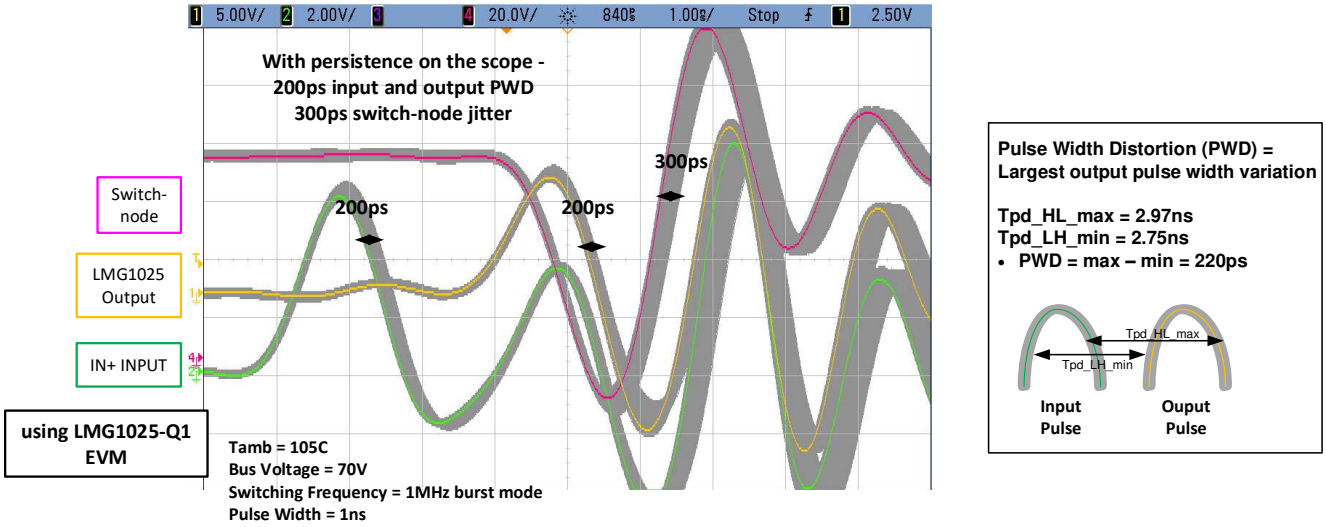

Figure 15. LMG1025-Q1 EVM Jitter and PWD Analysis

5 Summary

The objective of the optimal laser driver is to create a resonant circuit layout limited only by trace inductance and bus capacitance in order to switch extremely fast. The laser driver circuit should have:

- Minimal gate loop and power loop interaction
- GaN / driver placement, and short trace lengths
- Short Laser leads for shorter pulse widths
- Minimal jitter / PWD for laser pulse width variation

The placement and routing for the laser driver and GaN FET is very important to achieve fast edges without ringing while using GaN. For the lowest inductance connection, put the gate driver, GaN FET and laser on the top layer in the smallest area. Then connect the return paths on the adjacent layer with in-pad microvias. The more nH of power loop inductance the more affect it will have on the gate loop due to CSI. So it is important that the laser leads are short. A GaN FET and high-performance GaN driver can deliver high-performance Lidar laser transmitters. LMG1020 and LMG1025-Q1 both have the ability to improve the performance of a laser circuit enabling faster, further and more precise Lidar for cutting edge applications.

6 Related Documentation

- Texas Instruments, *TI Designs:TIDA-01573 Nanosecond Laser Driver Reference Design for LiDAR*
- Texas Instruments, *LMG1020 Datasheet*
- Texas Instruments, *Using the LMG1020EVM-006 Nano-second LiDAR EVM*
- Texas Instruments, *LMG1025-Q1 Datasheet*
- Texas Instruments, *Using the LMG1025-Q1EVM Nano-second LiDAR EVM*

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