Application Note

Multiplexers and Signal Switches Glossary

ABSTRACT

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1 About This Multiplexers and Signal Switches Glossary

This glossary provides a brief overview and introduction to the terminology, features, and parameters for TI'smultiplexers and signal switches for analog signal chain applications. The entire signal switches and multiplexers portfolio can be found at *www.ti.com/switches*.

For components used to manage power rails and for applications that require a switch current of greater than 500mA, TI offers a power switch and power multiplexer portfolio which can each be found at *www.ti.com/powerswitch*.

2 Introduction to Multiplexers and Signal Switches

Signal switch — An integrated circuit (IC) used for connecting and disconnecting an electrical circuit. For more information, see the *Switches and muxes: What are switches & multiplexers?* training video from *TI Precision Labs*.

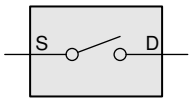


Figure 2-1. Ideal 1:1 SPST Switch

Multiplexer (Mux) — An integrated circuit that connects a selected signal path to a single line.

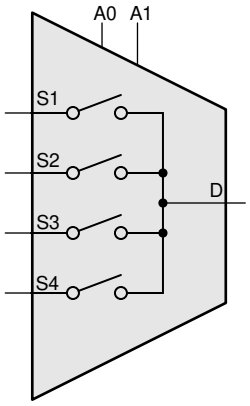


Figure 2-2. Ideal 4:1 Mux

Analog switches and multiplexers — These devices are used for switching and multiplexing analog and digital signals up to 500 mA in applications such as:

- Precision Data Acquisition
- GPIO Expansion
- Diagnostics
- System communication
- Bus Isolation
- System Protection
- Power Sequencing
- General-Purpose Signal Switching

Protocol-specific switches and multiplexers — These devices are defined to support specific protocol applications such as USB, HDMI, LAN, MIPI, audio, memory and so forth.

Precision — These devices minimize offset error and signal distortion in a high-accuracy measurement system.

Protection — These devices isolate I/O signal paths and protect the system using powered-off, overvoltage and undershoot protection.

Low voltage — These devices support I/O signals ≤ ±25 V

Mid voltage — These devices support I/O signals > ±25 V

Configuration — Defines the number of signals that can be selected. Table 2-1 shows the typical configurations.

Channel — Defines the number of configurations (circuits) in a single device. Table 2-1 shows the 1- and 2- channel configurations, but the number of channels may exceed 2.

Table 2-1. Configurations and Channels

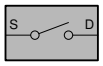
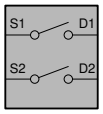
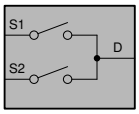
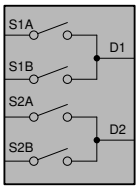
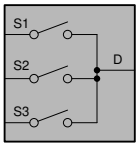
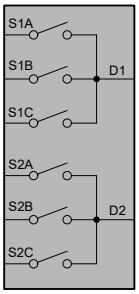
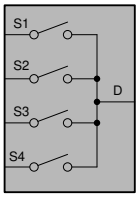
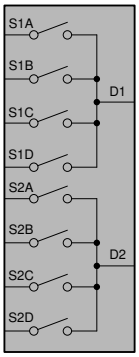
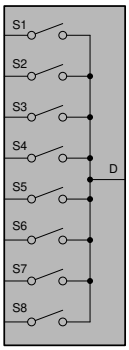
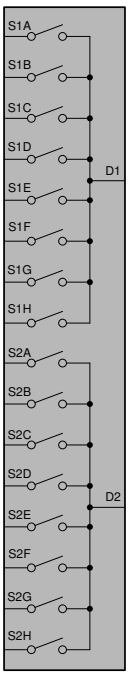
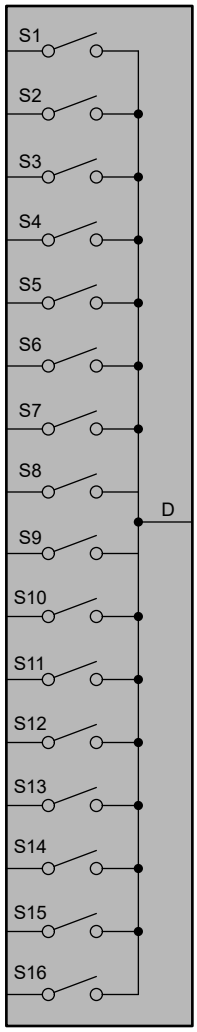
		1-Channel	2-Channel
Configuration	1:1		
	2:1		
	3:1		
	4:1		
Configuration	8:1		

Table 2-1. Configurations and Channels (continued)

		1-Channel	2-Channel
Configuration	16:1		N/A

3 Operation of Multiplexers and Signal Switches

Absolute maximum ratings — These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Stresses beyond those listed under the *Absolute Maximum Rating* may cause permanent damage to the device.

Recommended operating conditions — The operating conditions for which the device has been characterized.

Single power supply — Device with only positive power supply pins with reference to ground. The voltage applied is labeled as V_{DD}, V_{CC}, V_+ and so forth.
Dual power supply — Device with positive and negative supply pins with reference to ground. Voltage applied at the positive pin is labeled as V_{DD}, V_{CC}, V_+, and so forth, and at the negative pin is labeled as V_{SS}, V_{EE}, V_-, and so forth.

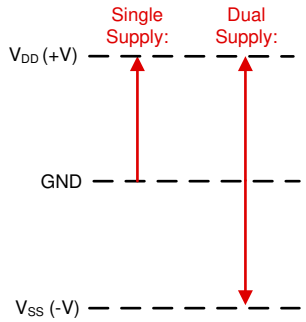


Figure 3-1. Single and Dual Supply

Switch control signal levels (V_{IH}, V_{IL}) — Voltage levels required on the control pins (EN, SEL, IN, and so forth) required for the switch to change the internal signal path.

- **V_{IH}** – The minimum voltage for the input control signal to achieve a logic "1"*high* value
- **V_{IL}** – The maximum voltage for the input control signal to remain a logic "0"*low* value

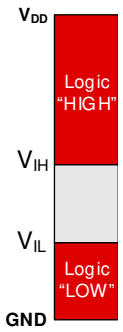


Figure 3-2. Switch Control Signal Levels

Rail-to-rail — A common term meaning that a device will support $V_{I/O}$ voltage range between the most positive and most negative power supply *rails*.

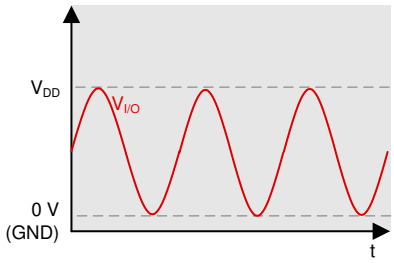


Figure 3-3. Rail-to-Rail

Input/Output voltage beyond supply – The switch can support voltage range beyond the supply rail to $V_{I/O(MAX)}$as indicated by the recommended operating conditions.

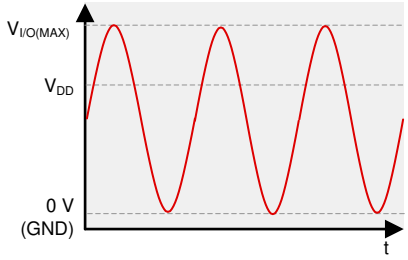


Figure 3-4. I/O Voltage Beyond Supply

Bidirectional signal path – The switch conducts equally well from source (S) to drain (D) or from drain (D) to source (S). Each channel has very similar characteristics in both directions and supports both analog and digital signals. TI analog switches and multiplexers are typically bidirectional. See the *Switches and muxes: Are switches & multiplexers bidirectional?* training video from *TI Precision Labs*.

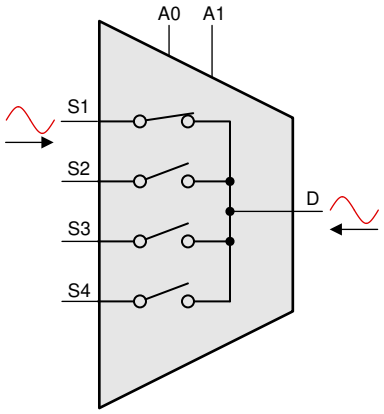


Figure 3-5. Bidirectional Signal Path

4 Additional Features

1.8-V Control Logic – Switches with this feature have a built-in voltage translator to prevent voltage mismatch between the supply rail and the control logic. V_{IH} and V_{IL} levels are compatible with the 1.8-V logic levels at any voltage supply. See the *Simplifying Design With 1.8 V logic MUXes and Switches Tech Note* for more information.

Fail-Safe Logic – Ensures the switch stays off and the voltage on the logic pin (V_{SEL}) does not back-power V_{DD} when V_{SEL} is greater than V_{DD}. See the *Switches and muxes: What is fail-safe logic?* training video from *TI Precision Labs*.

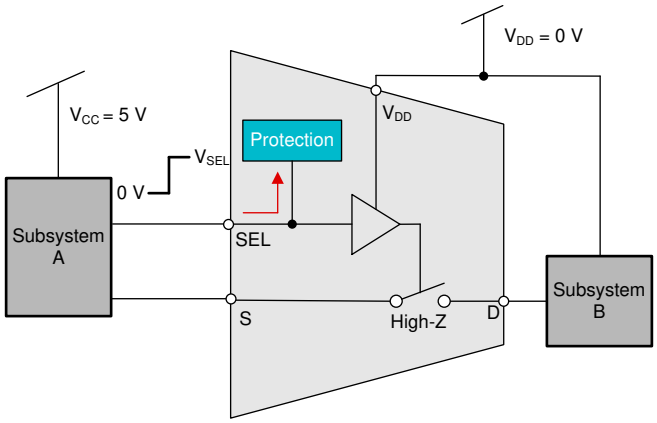


Figure 4-1. Fail-Safe Logic

Injection Current Control — Devices with Injection Current Control shunt injected current on disabled (high-Z) signal pathways to ground. This mitigates error on the active signal pathway as the injected current is going into the ground rail and not the power rail. See the *Switches and muxes: Prevent crosstalk with injection current control* training video from *TI Precision Labs*.

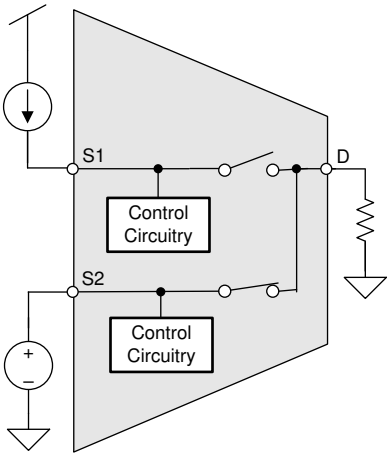


Figure 4-2. Injection Current Control

Integrated Pulldown Resistor on Logic Pin – Internal weak pulldown resistors to GND to ensure the logic pins are not floating.

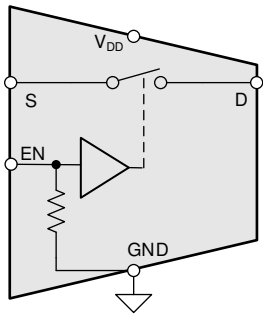


Figure 4-3. Integrated Pulldown Resistor on Logic Pin

Latch-Up Immunity – Devices that are latch-up immune can use various methods to achieve latch up immunity such as being built in a Silicon On Insulator (SOI) process, employing the use of guard rings, or a mix between different methods. When these measures are taken Electrical Overstress, Electrically Fast Transients, and Injected Currents will not cause latch up in these devices. See the *Switches and muxes: What is latch-up immunity?* training video from *TI Precision Labs*.

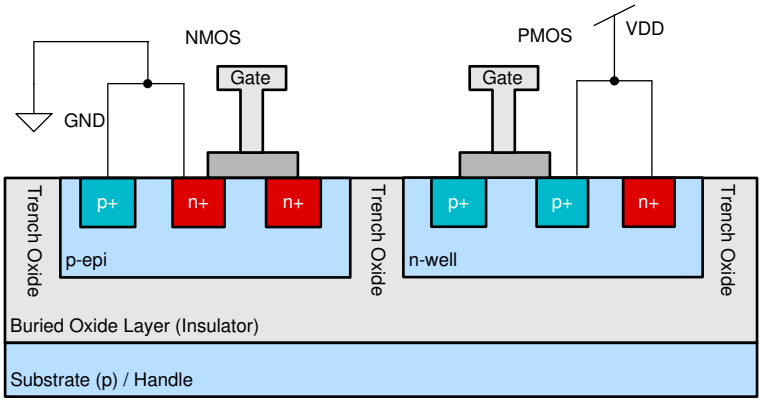


Figure 4-4. Latch-Up Immunity With SOI Process

Overvoltage Protection – When the input voltage $V_{I/O}$ exceeds the defined threshold voltage, V_{TH} or V_T, the switch enters the high impedance state, isolates signal path, and protects downstream components. Depending on device the threshold can determined in 1 of 3 ways.

- Fixed Threshold
- Threshold = Supply
- Threshold = Configurable

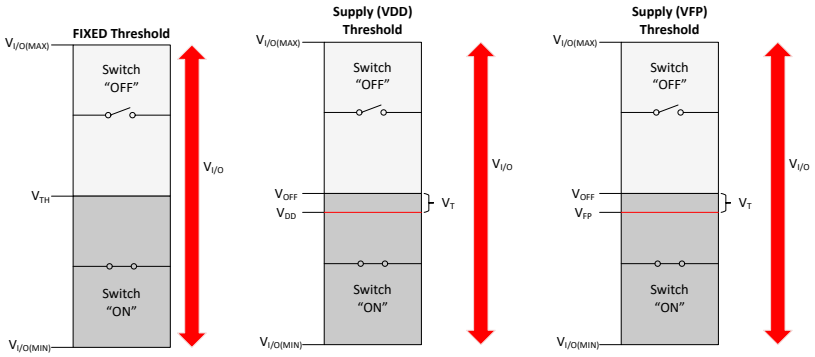


Figure 4-5. Overvoltage Protection

Undervoltage Protection – When the input voltage $V_{I/O}$ falls below the defined threshold voltage, V_{TH}, the switch enters the high impedance state, isolates signal path, and protects downstream components. Depending on device the threshold can determined in 1 of 2 ways.

- Threshold = Supply
- Threshold = Configurable

This feature typically exists alongside Overvoltage Protection

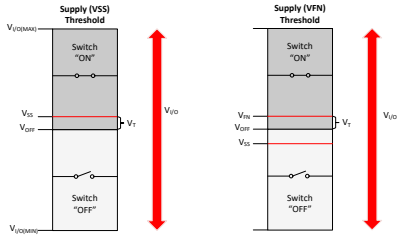


Figure 4-6. Undervoltage Protection

Fault Flag Indicators – On some devices there is a fault flag pin that will change states (typically from high to low) when a fault is present on the device and will return to its default state when the fault is cleared.

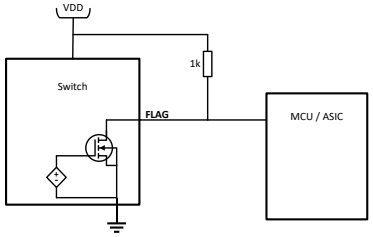


Figure 4-7. Fault Flag Indicators

Drain Response Output – On some protection switches/multiplexers the output response of a device during a fault condition can be set to either clamp to supply or open circuit the output.

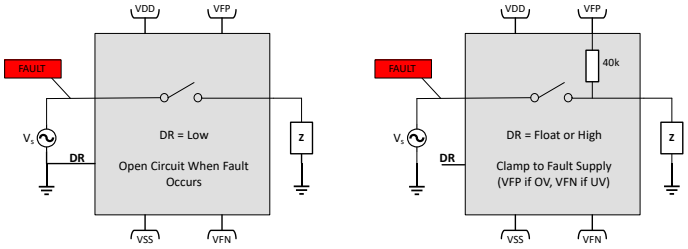


Figure 4-8. Drain Response Output

Powered-Off Protection – Protects switch and isolates signal path when signals are present at the I/O pins and VDD = 0 V. See the *Switches and muxes: Simplify power sequencing with powered-off protection* training video from *TI Precision Labs*and the *Eliminate Power Sequencing With Powered-off Protection Signal Switches Tech Note* for more information.

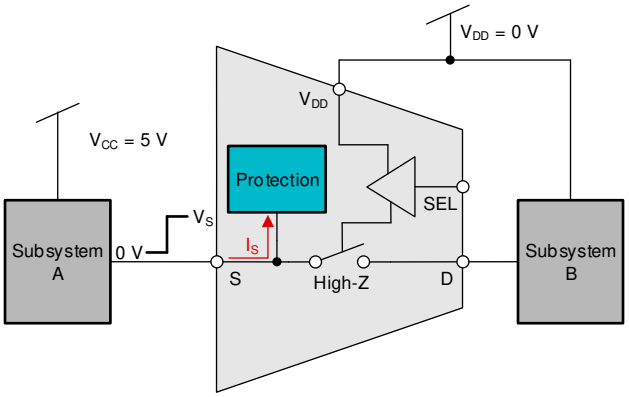


Figure 4-9. Powered-Off Protection

5 DC Characteristics

For more parameter information, see the device data sheet.

On-Resistance (R_{ON}) — The resistance of the switch pathway when the switch pathway is closed (low impedance). The resistance varies with temperature, supply voltage, and input voltage with respect to ground.

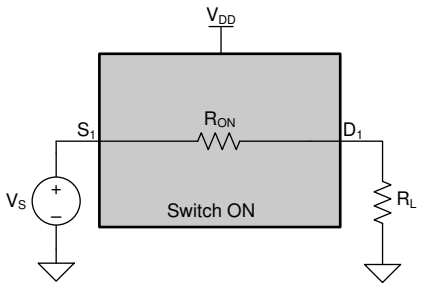


Figure 5-1. On-Resistance

On-Resistance Flatness ($R_{ON\ FLAT}$) — Difference between the maximum and minimum value of Ron in a channel over the V_D or V_S voltage range (w.r.t. ground).

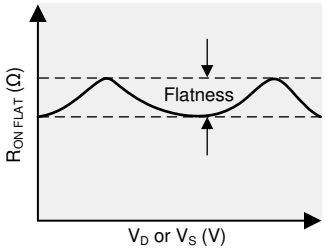


Figure 5-2. On-Resistance Flatness

On-Resistance Match Between Two Channels (ΔR_{ON}) – Difference between On-Resistance of two different switch pathways at the same input voltage

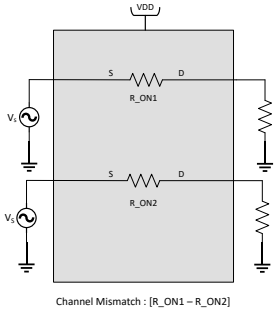


Figure 5-3. ΔR_{ON}

OFF leakage current ($I_{D(OFF)}$, $I_{S(OFF)}$) — Leakage current measured at the input port, with the corresponding channel output in the OFF state under worst-case input and output conditions.

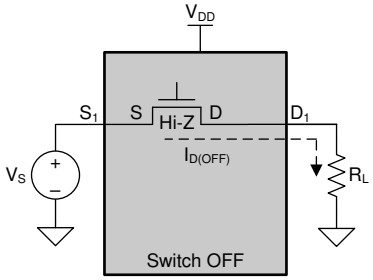


Figure 5-4. OFF Leakage Current

Powered-off I/O pin leakage current (I_{POFF}) — The leakage current flowing into or out of the source pin when the device is powered off (V_{DD} = 0V).

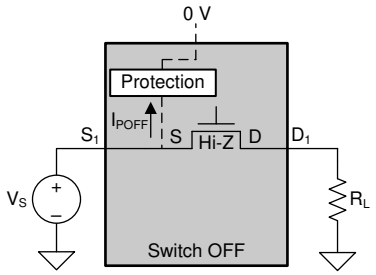


Figure 5-5. Powered-Off I/O Pin Leakage Current

ON leakage current ($I_{D(ON)}$, $I_{S(ON)}$) — Leakage current measured at the input port in the ON state, with the corresponding output port in the ON state and the output being open.

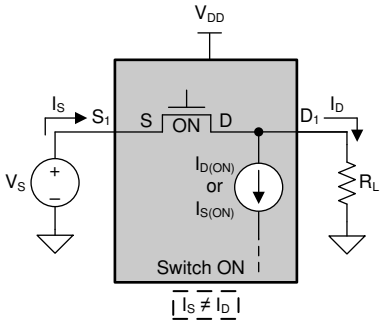


Figure 5-6. ON Leakage Current

Control input leakage (I_{SEL} or I_{EN}) — Leakage measured at the switch control pins.

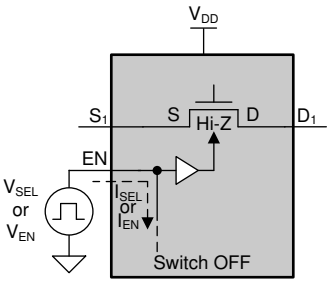


Figure 5-7. Control Input Leakage

Supply Current (IDD or ISS) – The supply current is the amount of current that is sourced from/sunk into the supply pins. IDD refers to current into the VDD pin and ISS refers to current into the VSS pin.

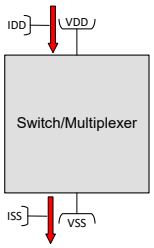


Figure 5-8. Supply Current

6 Dynamic Characteristics

For detailed information of dynamic characteristics, see the *Multiplexers: Bandwidth, Channel-to-Channel Crosstalk, Off-Isolation and THD+Noise* training video from *TI Precision Labs*.

For more parameter information, see the device data sheet.

Off capacitance source and drain (C_{OFF}) — The capacitive loading when a switch path is in the high-impedance state.

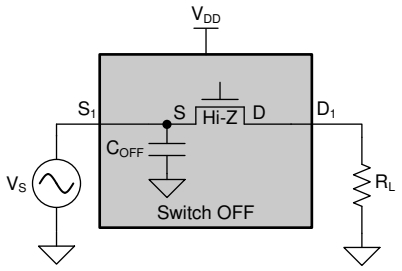


Figure 6-1. Source and Drain Off Capacitance

On capacitance source and drain (C_{ON}) — The capacitive loading when a switch path is in the low-impedance state.

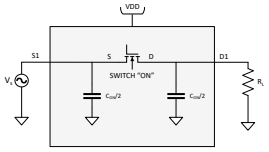


Figure 6-2. Source and Drain On Capacitance

Charge injection (Q_C) — Charge injection is a measurement of unwanted signal coupling from the control (EN) input to the analog output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.

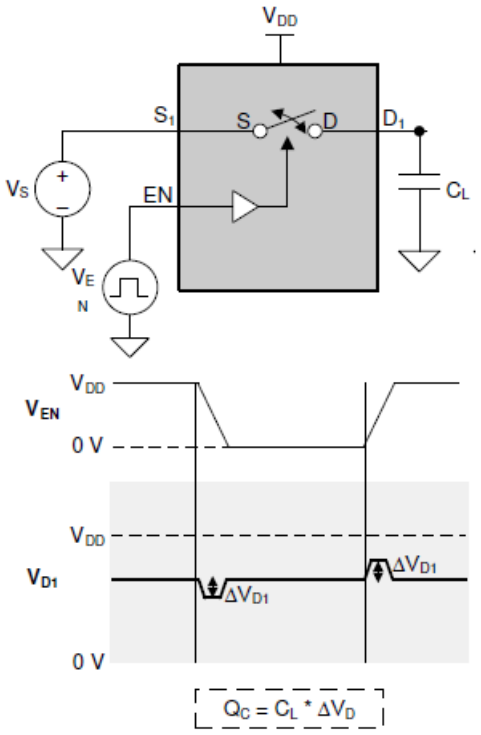


Figure 6-3. Charge Injection

Off-isolation (O_{ISO}) — A measurement OFF-state switch impedance. This is the ratio of V_{D1} to V_{S1} measured in dB at a specific frequency, with the corresponding channel in the OFF state.

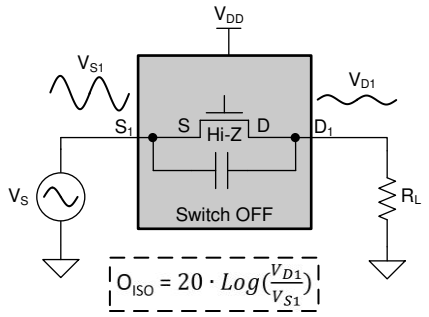


Figure 6-4. Off-Isolation

Channel-to-channel crosstalk (X_{TALK}) — A measurement of unwanted signal coupling from an ON channel to an OFF channel. This is the ratio of V_{S2} to V_{S1} measured in dB at a specific frequency.

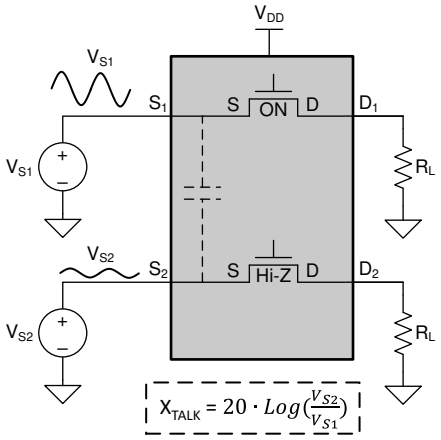


Figure 6-5. Channel-to-Channel Crosstalk

Bandwidth (BW) — The frequency range of signals that can pass through the switch with no more than 3 dB of attenuation from the DC gain (0 Hz).

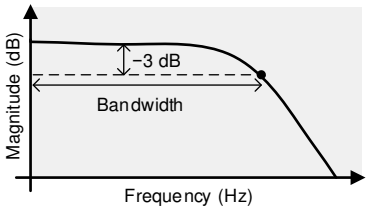


Figure 6-6. Bandwidth

Insertion Loss - The loss through the switch with predefined load across frequency. Since the switch is more than just a resistor when closed there is frequency dependent loss associated with the switch - this is defined by Insertion Loss

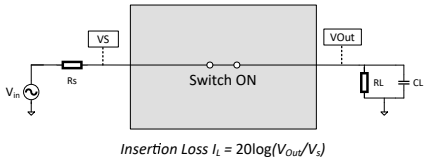


Figure 6-7. Insertion Loss

Total Harmonic Distortion + Noise (THD+N) -
Also called Sine Wave Distortion – this parameter looks at the harmonic content introduced by the switch and is defined by summing all non-fundamental harmonics RMS amplitudes + the noise floor and dividing it by the RMS amplitude of the fundamental frequency. This parameter is commonly expressed as a percentage.

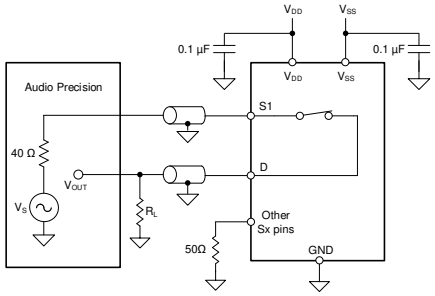


Figure 6-8. THD + N

7 Timing Characteristics

For detailed information, see the *Switches and muxes: What are timing characteristics?* training video from *TI Precision Labs*.

For more parameter information, see the device data sheet.

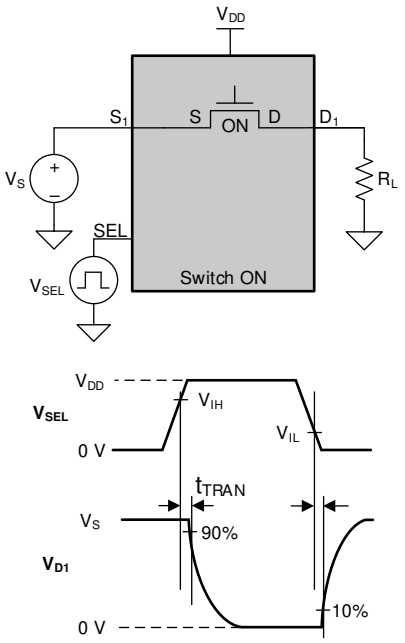


Figure 7-1. Transition Time

Transition time (t_{TRAN}) — The time taken by the switch output to rise or fall within a given percentage of the final value after the address signal has risen or fallen past the logic threshold.

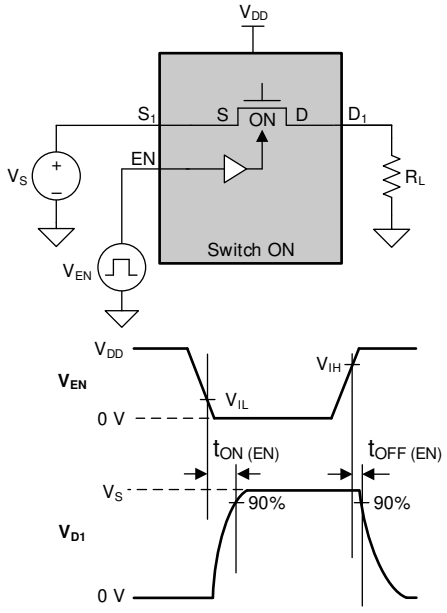


Figure 7-2. Device Turn on Time From Enable Pin

Device turn on time from enable pin ($t_{ON(EN)}$ and $t_{OFF(EN)}$) — The time taken by the switch output to rise or fall within a given percentage of the final value after the enable has risen or fallen past the logic threshold.

Break-before-make time ($t_{OPEN\ (BBM)}$) — Ensures that in a multiplexer, two multiplexer paths are never electrically connected when the signal path is changed by the select input.

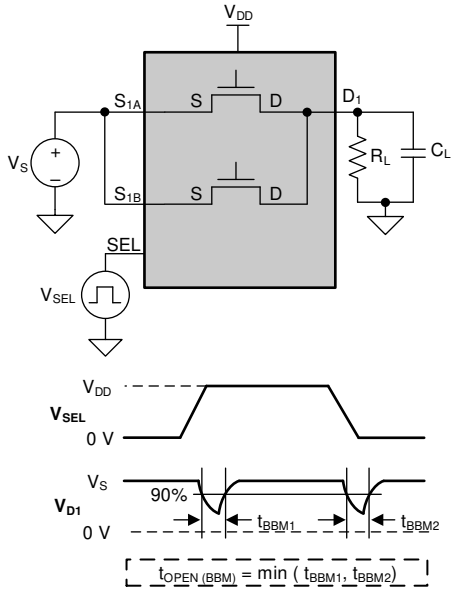


Figure 7-3. Break-Before-Make Time

Make-before-break time ($t_{CLOSED\ (MBB)}$) — Ensures that in a multiplexer, two multiplexer paths are never electrically disconnected when the signal path is changed by the select input.

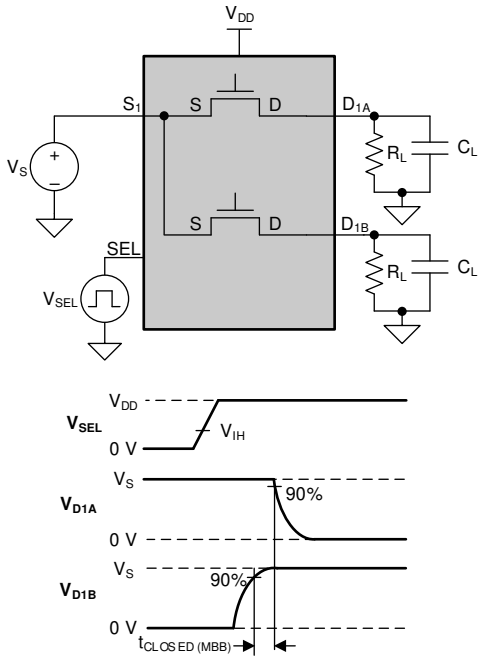


Figure 7-4. Make-Before-Break Time

Propagation delay through the switch (t_{pd}) — The time required for a signal to pass from the input signal pin to the respective output signal pin.

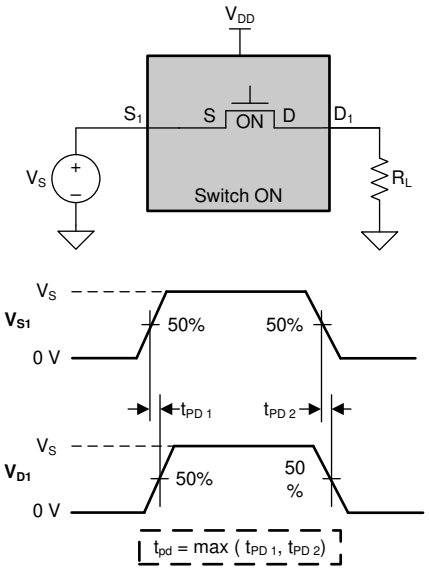
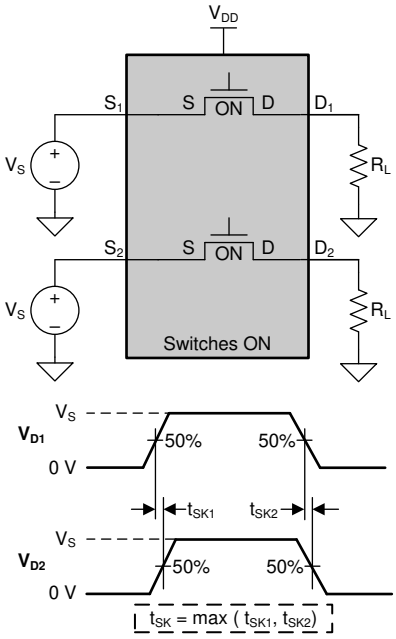


Figure 7-5. Propagation Delay Through the Switch

Figure 7-6. Output-to-Output Skew

Output-to-output skew (t_{SK}) — The maximum difference between the propagation delays of different outputs due to different internal paths.



Fault Response Time ($t_{RESPONSE}$) - Fault response time ($t_{RESPONSE}$) measures the delay between the source voltage exceeding the fault supply voltage (VFP or VFN) by 0.5V and the drain voltage failing to 90% of the fault supply voltage exceeded. This only applies to Fault Protected Devices.

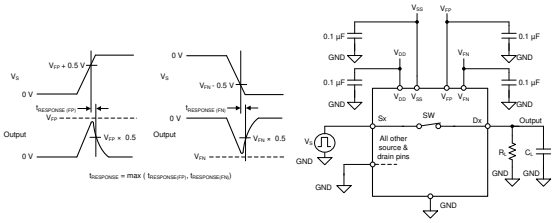


Figure 7-7. Fault Response Time

Fault Flag Response Time ($t_{RESPONSE(FLAG)}$) - Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage (VFP or VFN) by 0.5 V and the general fault flag (FF) pin to go below 10% of its original value. This only applies to devices with an FF pin.

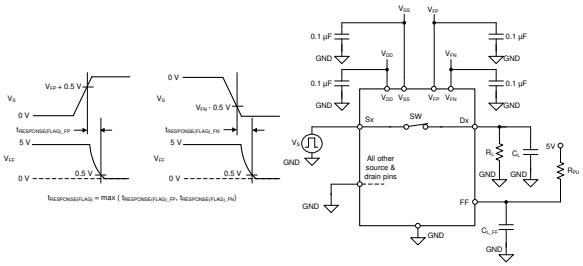


Figure 7-8. Fault Flag Response Time

Fault Drain Enable Time ($t_{RESPONSE(DR)}$) -$t_{RESPONSE(DR)}$ represents the delay between the voltage at the DR pin falling from a high to low signal and the output of the drain pin reaching 90% of the fault supplies (VFP or VFN). tRESPONSE(DR) is a measure of how quickly the internal pull-up engages in response to the DR pin. Only on devices with a DR pin.

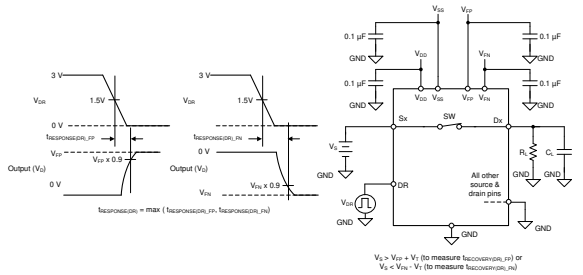


Figure 7-9. Fault Drain Enable Time

Fault Recovery Time ($t_{RECOVERY}$) -
Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (VFP or VFN) plus 0.5 V and the drain voltage rising from 0V to 50% of the fault supply voltage exceeded (only on fault protected devices).

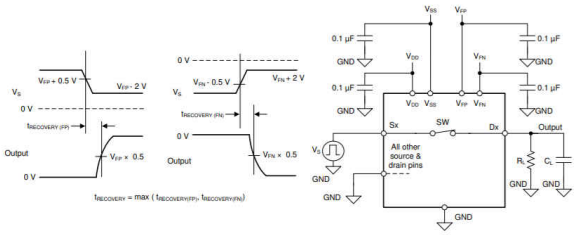


Figure 7-10. Fault Recovery Time

Fault Flag Recovery Time ($t_{RECOVERY(FLAG)}$) – Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from the overvoltage condition to below the fault supply voltage (VFP or VFN) plus 0.5 V and the general fault flag (FF) pin to rise above 3 V with 5 V external pull-up (only on devices with fault flags).

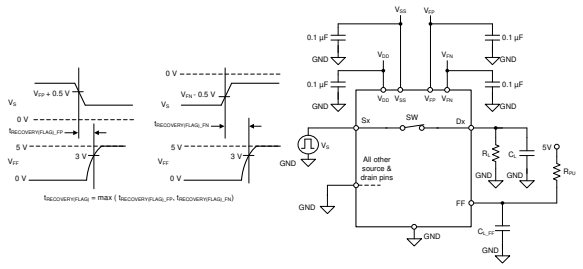


Figure 7-11. Fault Flag Recovery Time

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2021) to Revision B (November 2021)	Page
• Added *Undervoltage protection* topic	8
• Added *Fault Flag Indicators* topic	8
• Added *Drain Response Output* topic	8
• Added *On-Resistance Mismatch between Channels* topic	11
• Added *Supply Current* topic	11
• Added *Insertion Loss* topic	13
• Added *THD + N* topic	13
• Added *Fault Response Time* topic	16
• Added *Fault Flag Response Time* topic	16
• Added *Drain Response Enable Time* topic	16
• Added *Fault Recovery Time* topic	16
• Added *Fault Flag Recovery Time* topic	16

Changes from Revision * (March 2020) to Revision A (June 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3

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