Application Report
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Power Loss Calculation With Common Source Inductance Consideration for Synchronous Buck Converters

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ABSTRACT

The synchronous buck converter is a widely used topology in low-voltage, high-current applications. Low-power loss and highly efficient synchronous buck converters are in great demand for advanced microprocessors of the future. Good understanding of power losses in a synchronous buck converter is critical for improving converter performance. Common source inductance (CSI) is the inductance shared by the main current path and the gate driver loop in a converter and carries the drain-source current and the gate-charging current. A high-side (HS) FET CSI has significant impact on converter performance, especially switching power loss: the greater the HS CSI, the greater the switching loss. This application report analyzes MOSFET-related power losses in a synchronous buck converter. The effects of HS CSI are also discussed and quantified. This document introduces the Texas Instruments NexFET™ Power Block, which uses advanced device and package techniques to minimize CSI and thus reduce system power loss. To simply design efforts, a complementary design calculator (SLPC015) is available.

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1 Introduction

The synchronous buck converter is one of the most popular topologies for today's low-voltage regulators. As transistor counts in a single processor continue to increase, various challenges arise for low-voltage, high-current voltage regulator design. High efficiency is one of the most critical requirements for improving power density.

Good understanding of power loss in synchronous buck converters is important for converter design optimization. Power loss of a synchronous buck converter includes several parts: MOSFET loss, inductor loss, printed-circuit board (PCB) loss, etc. Among these, MOSFET loss is complicated and significant. This application report only discusses the MOSFET loss in synchronous buck converters.

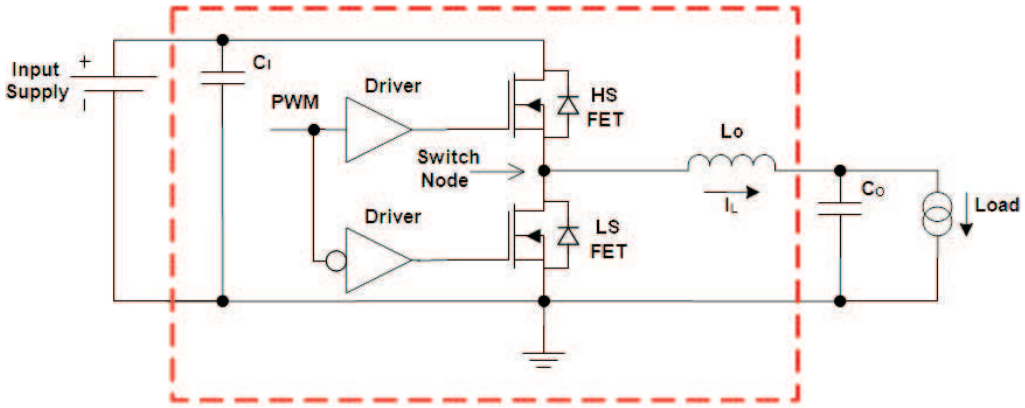

Figure 1. Schematic of Synchronous Buck Converter

Figure 1 shows the schematic of a typical synchronous buck converter. MOSFET-related power loss in a synchronous buck converter is composed of conduction loss and switching loss. Conduction loss is the sum of high side (HS) and low side (LS) FETs conduction loss. This loss is independent with switching frequency. Switching loss consists of HS FET switching loss, LS FET switching loss, gate drive loss, LS body diode loss, and FETs output capacitance loss. Switching loss goes up linearly with increasing switching frequency. Not all calculations for power losses are straightforward. Specifically, MOSFET switching loss is determined by the transition time and influenced by several parameters in the gate drive loop. Common source inductance (CSI) is one of the most important parameters. CSI is the inductance shared by the main-current path and the gate-driver loop and carries the drain-source current and the gate-charging current. Any voltage induced on CSI changes the effective gate-source voltage of the MOSFET. Because of the importance of gate-source voltage on the switching performance of power MOSFETs, CSI has a significant impact on the system performance, especially on HS FET switching loss. This application report first analyzes the MOSFET-related power loss in a synchronous buck converter and then presents the equations for power loss calculations. The impacts of CSI on converter power loss also is discussed and quantified in this document.

2 Conduction Loss

The conduction loss is determined by the on-resistances of the MOSFETs and the transistor RMS current. Specifically, the conduction loss for HS FET and the LS FET can be calculated by Equation 1 and Equation 2, respectively:

$$P_{cond(HS)} = R_{ds(ON)HS} \times I^2_{RMS(HS)} \quad (1)$$

$$P_{cond(LS)} = R_{ds(ON)LS} \times I^2_{RMS(LS)} \quad (2)$$

$$I_{RMS(HS)} = \sqrt{\left(\frac{D}{3} \times \left[\left(I_{OUT} + \frac{I_{ripple}}{2}\right)^2 + \left(I_{OUT} + \frac{I_{ripple}}{2}\right) \times \left(I_{OUT} - \frac{I_{ripple}}{2}\right) + \left(I_{OUT} - \frac{I_{ripple}}{2}\right)^2\right]\right)} \quad (3)$$

$$I_{RMS(LS)} = \sqrt{\frac{1-D}{3} \times \left[\left(I_{OUT} + \frac{I_{ripple}}{2} \right)^2 + \left(I_{OUT} + \frac{I_{ripple}}{2} \right) \times \left(I_{OUT} - \frac{I_{ripple}}{2} \right) + \left(I_{OUT} - \frac{I_{ripple}}{2} \right)^2 \right]} \quad (4)$$

NOTE: See Appendix B for list of symbols.

3 Switching Loss

Switching loss is composed of several parts: MOSFET switching loss (HS and LS), MOSFET gate drive loss, LS body-diode loss, and MOSFET output capacitance loss. These losses are analyzed in the following text.

3.1 MOSFETs Switching Loss

3.1.1 Typical HS Switching Power Loss Calculation

Power converters use semiconductor devices as HS and LS switches. It takes finite time for the devices to turn on and off. During the turnon and turnoff transitions, due to the LS clamping effects, the HS device is affected by both high current and high voltage at the same time, which induces switching losses. Figure 2 shows the HS FET gate-source voltage V_{GS}, drain-source voltage V_{DS} and drain current I_{DS} waveforms during HS turnon for the synchronous buck converter shown in Figure 1.

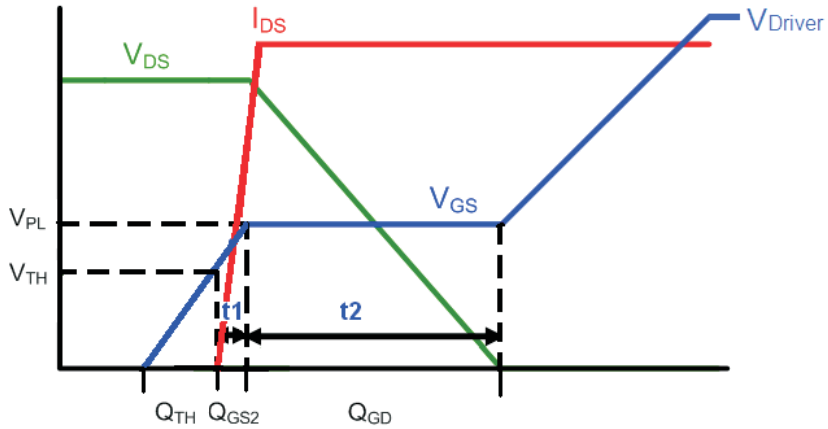

Figure 2. Ideal Waveform at Device Turnon

Typically, the HS gate current and the related switching loss are estimated by Equation 5 and Equation 6:

$$I_g = \frac{V_{Driver} - V_{PL}}{R_g + R_{driver}} \quad (5)$$

$$P_{sw} = VIN \times I_{OUT} \times f_{sw} \times \frac{Q_{sw}}{I_g} \quad (6)$$

NOTE: FET plateau voltage V_{PL} can be found in the gate charge curve on device data sheets.

3.1.2 HS FET Switching Loss Calculation With CSI Consideration

In reality, both the HS and LS transistors have CSI due to device packages and PCB designs. For hard-switching devices, CSIs slow down their turnon and turnoff and hence increase the switching losses.

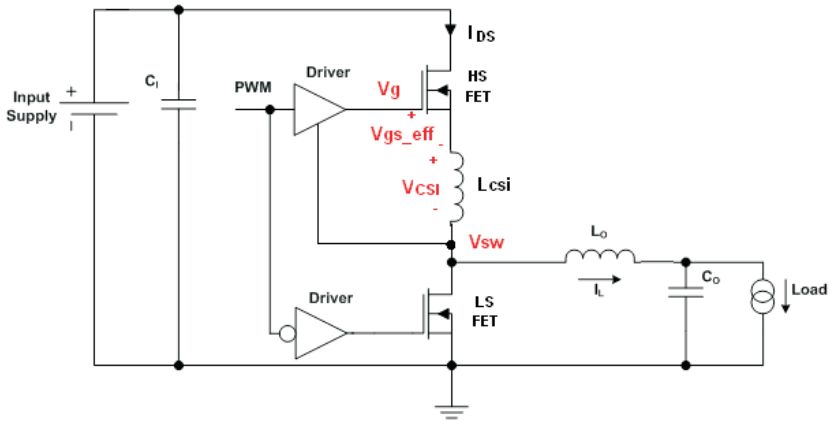

Figure 3. Schematic for Converter With CSI Consideration

Taking the HS FET in Figure 3 as an example, when the HS FET drain-current I_{DS} begins to increase at turnon, a voltage drop proportional to dI_{DS}/dt is generated across the CSI. Therefore, the effective gate-source voltage is reduced by this CSI voltage as shown in Equation 7:

$$V_{gs(eff)} = V_g - V_{sw} - L_{csi} \times \frac{dI_{DS}}{dt} \tag{7}$$

To account for the effect of CSI in power loss, Equation 5 and Equation 6 need to be modified. The new calculations are analyzed in detail as follows:

1. Switching power loss in period t1

   First, analyze area Q_{GS2} in Figure 2. When the gate-source voltage reaches the threshold voltage V_{TH}, the device drain current I_{DS} begins to increase from 0 A until it reaches ($I_{OUT} - I_{ripple}/2$) at the end of t1, where I_{ripple} is the peak-to-peak inductor current ripple. The change of current induces a voltage $V_{Lcsi(t1)}$ on HS common source inductance L_{csi}. $V_{Lcsi(t1)}$ and the gate current $I_{g1(on)}$ during time t1 then can be calculated by Equation 8 and Equation 9:

$$V_{Lcsi(t1)} = L_{csi} \times \frac{dI_{DS}}{dt1} = L_{csi} \times \frac{I_{OUT} - \frac{I_{ripple}}{2}}{dt1} \tag{8}$$

$$I_{g1(on)} = \frac{V_{Driver} - V_{PL(HS)} - V_{Lcsi(t1)}}{R_{g(HS)} + R_{driver}} \tag{9}$$

$$dt1 = \frac{Q_{gs2(HS)}}{I_{g1(on)}} \tag{10}$$

   Solving Equation 8, Equation 9, and Equation 10, the gate current is obtained and shown in Equation 11:

$$I_{g1(on)} = \frac{V_{Driver} - V_{PL(HS)}}{R_{g(HS)} + R_{driver} + L_{csi} \times \frac{I_{OUT} - \frac{I_{ripple}}{2}}{Q_{gs2(HS)}}} \tag{11}$$

   The related switching power loss is then calculated as follows,

$$P_{sw(t1)} = 0.5 \times VIN \times \left(I_{OUT} - \frac{I_{ripple}}{2}\right) \times f_{sw} \times \frac{Q_{gs2(HS)}}{I_{g1(on)}} \tag{12}$$

2. Switching power loss in period t2

   Next, when entering area Q_{GD}, the LS FET output capacitance C_{oss} is charged from 0 V to V_{IN}, and the charge current flows through L_{csi}. Similarly, this current decreases the effective gate-source voltage of

the HS FET and hence gate current $I_{g2(on)}$ by inducing a voltage $V_{Lcsi(t2)}$ across the HS common source inductance. The LS capacitance current, HS CSI voltage, and HS gate current can be obtained by the following equations:

$$I_{Coss} = C_{oss(LS)} \times \frac{dV}{dt2} = C_{oss(LS)} \times \frac{VIN}{dt2} = \frac{Q_{oss(LS)}}{dt2} \quad (13)$$

$$dt2 = \frac{Q_{gd(HS)}}{I_{g2(on)}} \quad (14)$$

$$V_{Lcsi(t2)} = L_{csi} \times \frac{dI_{Coss}}{dt2} = \frac{L_{csi} \times Q_{oss(LS)}}{(dt2)^2} = \frac{L_{csi} \times Q_{oss(LS)} \times I_{g2(on)}^2}{Q_{gd(HS)}^2} \quad (15)$$

$$\frac{L_{csi} \times Q_{oss(LS)}}{Q_{gd(HS)}^2} \times I_{g2(on)}^2 + \left(R_{g(HS)} + R_{driver}\right) \times I_{g2(on)} - \left(V_{Driver} - V_{PL(HS)}\right) = 0$$

$$I_{g2(on)} = \frac{V_{Driver} - V_{PL(HS)} - V_{Lcsi(t2)}}{R_{g(HS)} + R_{driver}} \quad (16)$$

Reorganizing Equation 14, Equation 15, and Equation 16, the following Equation 17 is obtained:

(17)

Defining three parameters as follows,

$$a = \frac{L_{csi} \times Q_{oss(LS)}}{Q_{gd(HS)}^2} \quad (18)$$

$$b = R_{g(HS)} + R_{driver} \quad (19)$$

$$c = -\left(V_{Driver} - V_{PL(HS)}\right) \quad (20)$$

Then, the gate current within t2 is given by Equation 21:

$$I_{g2(on)} = \frac{-b + \sqrt{b^2 - 4 \times a \times c}}{2 \times a} \quad (21)$$

With $I_{g2(on)}$ solved, the switching power loss during time t2 is shown in Equation 22:

$$P_{sw(t2)} = 0.5 \times VIN \times \left(I_{OUT} - \frac{I_{ripple}}{2}\right) \times f_{sw} \times \frac{Q_{gd(HS)}}{I_{g2(on)}} \quad (22)$$

3. Switching power loss at HS turnon

   HS FET turnon loss is the sum of losses in area Q_{gs2} (t1) and area Q_{gd} (t2), given by:

$$P_{sw(HSon)} = 0.5 \times VIN \times \left(I_{OUT} - \frac{I_{ripple}}{2}\right) \times f_{sw} \times \left(\frac{Q_{gs2(HS)}}{I_{g1(on)}} + \frac{Q_{gd(HS)}}{I_{g2(on)}}\right) \quad (23)$$

4. Switching power loss at HS turnoff

   At the end of HS on-time, the inductor current reaches the peak value ($I_{OUT} + I_{ripple}/2$). Then, HS FET begins to turn off. Figure 4 shows the HS FET V_{GS}, V_{DS}, and I_{DS} waveforms at HS turnoff transition.

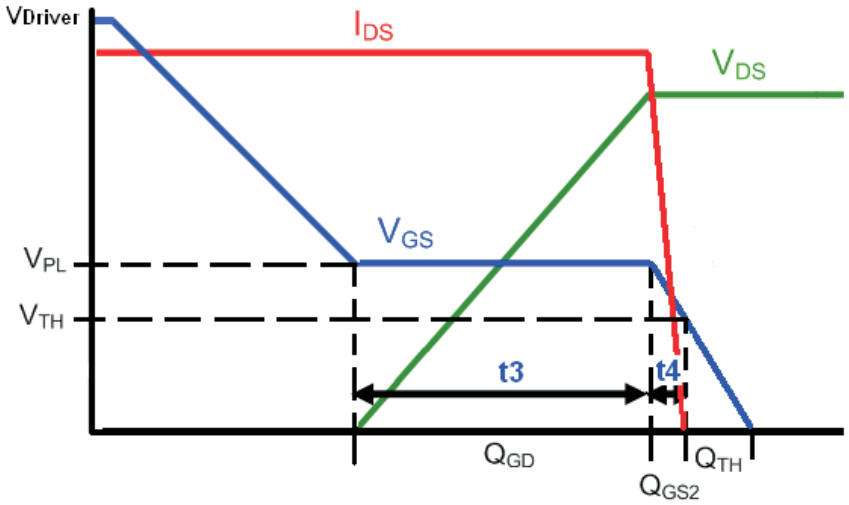

Figure 4. Ideal Waveforms at Device Turnoff

Following the preceding steps 1 to 3, the HS gate current and switching loss at turnoff can be obtained in the following equations:

$$I_{g1(off)} = \frac{V_{PL(HS)}}{R_{g(HS)} + R_{driver} + L_{csi} \times \frac{\left(I_{OUT} + \frac{I_{ripple}}{2}\right)}{Q_{gs2(HS)}}} \quad (24)$$

$$I_{g2(off)} = \frac{-b + \sqrt{b^2 - 4 \times a \times c}}{2 \times a} \quad (25)$$

$$a = \frac{L_{csi} \times Q_{oss(LS)}}{Q_{gd(HS)}^2} \quad (26)$$

$$b = R_{g(HS)} + R_{driver} \quad (27)$$

$$c = -V_{PL(HS)} \quad (28)$$

$$P_{sw(HSoff)} = 0.5 \times VIN \times \left(I_{OUT} + \frac{I_{ripple}}{2}\right) \times f_{sw} \times \left(\frac{Q_{gs2(HS)}}{I_{g1(off)}} + \frac{Q_{gd(HS)}}{I_{g2(off)}}\right) \quad (29)$$

5. Total HS FET switching power loss

   The total HS FET switching loss is the sum of HS turnon and turnoff losses as shown in Equation 30.

$$P_{sw(HS)} = P_{sw(HSon)} + P_{sw(HSoff)} \quad (30)$$

   Note that the HS sourcing and sinking impedance of drivers may be different. The sourcing/sinking impedances must be used for turnon/turnoff loss calculations, respectively.

3.1.3 LS Switching Loss Calculation

Considering LS FETs, both LS turnon and turnoff are soft switching at normal operations when the inductor current is positive: the LS FET turns on and off with its drain-source voltage equal to the body-diode forward voltage. Therefore, the LS switching loss is small and thus neglected in this application report.

3.2 Gate Drive Loss

The gate charge induced loss is straightforward and given by Equation 31.

$$P_{gate} = P_{gate(HS)} + P_{gate(LS)} = \left(Q_{g(HS)} + Q_{g(LS)}\right) \times V_{Driver} \times f_{sw} \quad (31)$$

3.3 LS Body Diode Loss

In order to prevent the cross-conduction of the HS FET and LS FET (shoot-through), two short dead-times are added into the converter: rise edge dead-time between LS FET turnoff and HS FET turnon and fall edge dead-time between HS FET turnoff and LS FET turnon. During these two dead-time intervals, both the HS and the LS FETs are off, and LS FET body diode conducts the inductor current. This LS body diode conduction introduces two power losses into the system: dead-time loss (diode conduction loss) and diode reverse-recovery loss.

3.3.1 Dead-Time Loss

Dead-time loss is induced by LS body diode conduction during dead-times and can be calculated using Equation 32.

$$P_{deadtime} = V_{SD} \times \left[\left(I_{OUT} - \frac{I_{ripple}}{2}\right) \times t_{deadtime(r)} + \left(I_{OUT} + \frac{I_{ripple}}{2}\right) \times t_{deadtime(f)}\right] \times f_{sw} \quad (32)$$

3.3.2 Diode Reverse-Recovery Loss

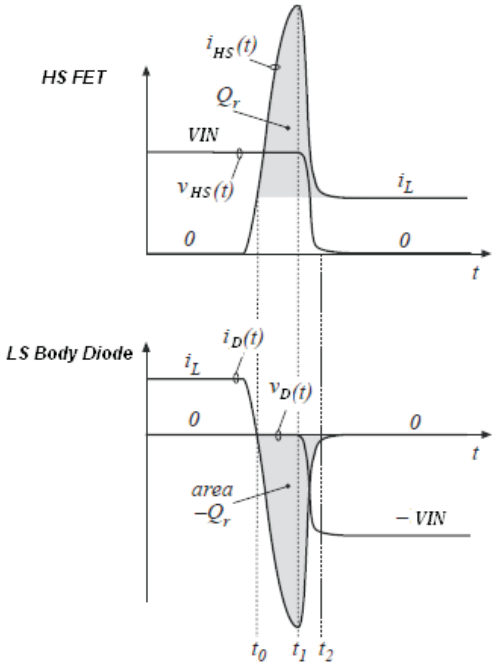

Figure 5. Diode Reverse-Recovery Waveforms

Diode reverse-recovery loss is due to the turnoff of the LS FET body diode. Specifically, when the LS FET body diode conducts the inductor current during the rise edge dead time, minority carriers are injected into and stored in the diode PN junction. As the HS FET starts to turn on, a negative current must first flow through the diode to remove the stored charge before the diode can block any negative voltage. As depicted in Figure 5, during this time, the HS drain-source voltage remains at VIN until the entire diode minority carriers are exhausted at t1 when the diode reverse-recovery current reaches the negative maximum Irr. Then, the diode begins to block negative voltage and the reverse current continues to flow to charge the body diode depletion capacitance. The total charge involved in this period is called reverse-recovery charge Qrr. Therefore, the diode reverse-recovery loss at HS turnon can be calculated as follows:

$$P_{DRR} = Q_{rr(LS)} \times VIN \times f_{sw} \quad (33)$$

3.4 Output Capacitance Loss

Another part of the MOSFET-related power loss in synchronous buck converters is FET output capacitance loss, which is induced by output capacitance charge/discharge. The C_{oss} loss for HS and LS FETs can be calculated in Equation 34 and Equation 35, respectively.

$$P_{Coss\_HS} = 0.5 \times Q_{oss\_HS} \times VIN \times f_{SW} \quad (34)$$

$$P_{Coss\_LS} = 0.5 \times Q_{oss\_LS} \times VIN \times f_{SW} \quad (35)$$

4 Power Loss Calculation Assumption

Note that the preceding equations are only accurate for continuous conduction mode (CCM) at which the output current is greater than or equal to half of the inductor peak-to-peak current ripple (I_{ripple}). In this application report, 0.5 × I_{ripple} is designated as the critical current. If the output current is smaller than the critical current, the converter may work at two different modes: forced continuous conduction mode (FCCM) or discontinuous conduction mode (DCM). For each of the two modes, some of the power loss calculations introduced in this document are not correct. For example, when the converter works in DCM, the inductor current increases from 0 A to (I_{OUT} + I_{ripple}/2) at HS FET on-time, then decreases back to 0 A at LS FET on-time. After that, the inductor current remains at 0 A for a time until HS FET turns on again. Therefore, the RMS current calculations in Equation 3 and Equation 4 are not correct. Another example is for FCCM: when the converter works in FCCM, negative current flows through the HS FET at its turnon transients. This negative current generates a negative voltage across the HS CSI. Therefore, the HS FET turnon is speeded up instead of being slowed down and the HS turnon switching loss then is reduced in FCCM. In the following calculation examples, only the MOSFETs power loss at output currents above the critical current is considered and discussed.

5 Power Loss Calculation Examples

In order to verify the accuracy of the calculations and compare the impacts of different CSIs on power losses, two examples are given in this application report: Converter 1 is a conventional synchronous buck converter with two discrete MOSFETs as HS and LS switches; Converter 2 is a synchronous buck converter using TI Power Block devices as switches. Figure 6 shows the schematic of Converter 1. Both the HS FET and LS FET have drain and source parasitic inductances due to their independent packages as shown in Figure 6. For Converter 2, the TI NexFET™ Power Block device is an optimized design for synchronous buck applications offering high-current, high-efficiency, and high-frequency capabilities. The Power Block device uses an advanced package technology called “source-down stacked die”, which stacks the HS FET and LS FET together and integrates them into one single package. In this way, the source of the HS FET is directly connected to the drain of the LS FET die, and the source of the LS FET contacts right to the GND pad. Therefore, package-induced LS drain inductance and CSIs for both HS and LS FET are significantly reduced in the TI Power Block device as shown in Figure 7. In addition, by integrating the HS and LS FET into one chip, TI Power Block device also minimizes the converter size and simplifies system designs.

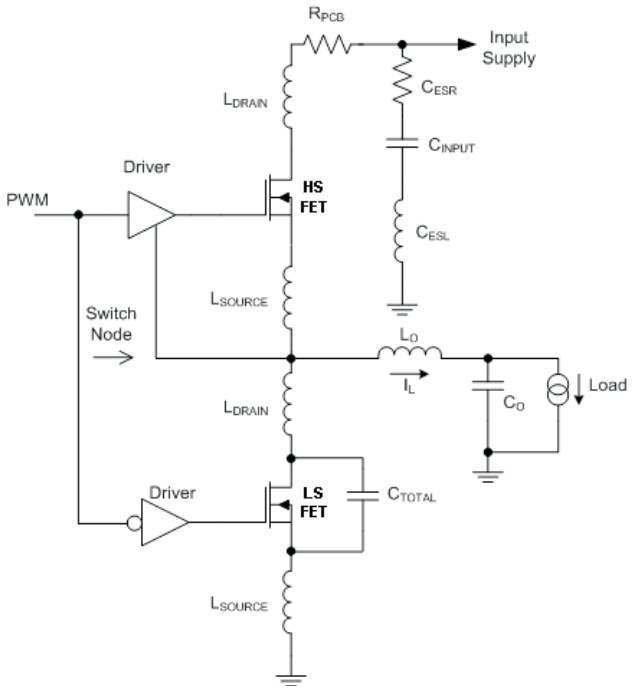

Figure 6. Schematic for Converter 1 – Discrete Solution

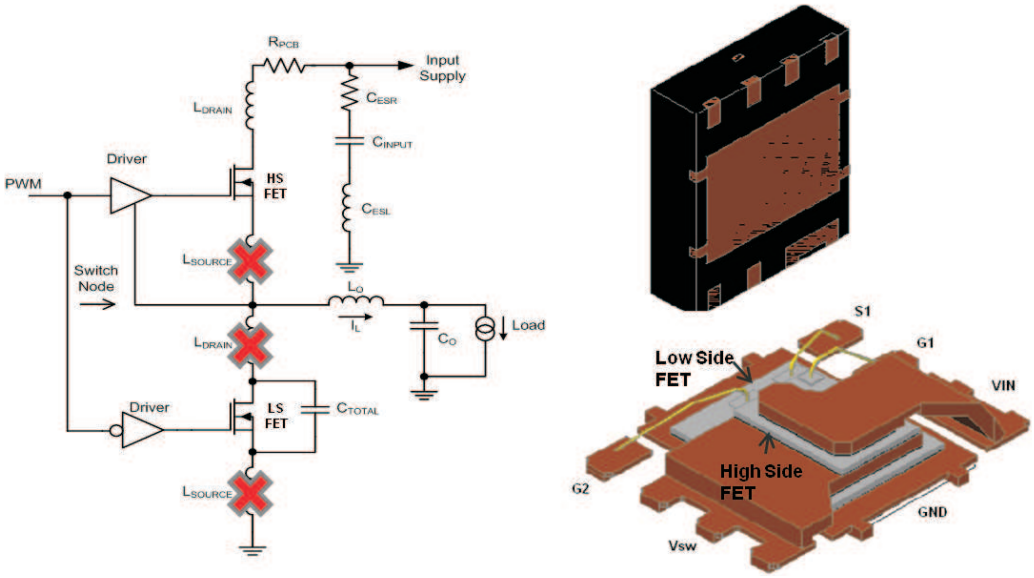

Figure 7. Schematic for Converter 2 – TI Power Block Solution

For this comparison, the same driver ICs are used in both converters, as well as the same output inductor (0.29 µH), similar PCB layout designs, and the same test conditions: V_{IN} = 12 V, V_{Driver} = 5 V, V_{out} = 1.3 V, I_{OUT} = 25 A, f_{sw} = 500 kHz. Table 1 lists the main device parameters for these two buck converters.

Table 1. Device Parameters

	Discrete (HS FET)	Discrete (LS FET)	TI Power Block (HS FET)	TI Power Block (LS FET)
R_{ds_on} (mΩ)	6.01	2.17	5.81	2.17
R_g (Ω)	0.8	1.5	1.4	1.4

Table 1. Device Parameters (continued)

	Discrete (HS FET)	Discrete (LS FET)	TI Power Block (HS FET)	TI Power Block (LS FET)
Q_{gs2} (nC)	1.3	1.9	1.3	2.3
Q_{gd} (nC)	1.9	2.5	1	2.5
Q_g (nC)	6.7	14	8.2	19.4
V_{PL} (V)	2.9	2.0	2.7	1.8
L_{csi} (pH)	400		100	
Q_{rr} (nC)		33		45
Q_{oss} (nC)	15.7	36	12.4	35

As shown in Table 1, the main difference between the discrete solution (Converter1) and the Power Block solution (Converter2) is that the discrete solution has a larger HS FET common source inductance (400 pH to 450 pH); whereas the Power Block solution has very small HS FET CSI (<100 pH) due the advanced package for the TI Power Block. Figure 8 and Table 2 compares the calculated loss and the measured loss for both converters.

Table 2. Power Loss Calculation Example for Synchronous Buck Converters

Power Loss (W)	Discrete Parts	TI Power Block	Power Loss Difference (W)
Calculated HS switching Loss	1.18	0.57	0.62
Calculated HS conduction Loss	0.49	0.48	0.01
Calculated LS Conduction Loss	1.20	1.20	0
Calculated HS Q_g Loss	0.02	0.02	0
Calculated LS Q_g Loss	0.04	0.05	-0.01
Calculated Q_{rr} Loss	0.20	0.27	-0.07
Calculated FETs C_{oss} Loss	0.17	0.15	0.06
Calculated Diode Conduction Loss	0.17	0.17	0.01
Total Calculated Power Loss	3.50	2.95	0.55
Measured Power Loss	3.45	2.98	0.47

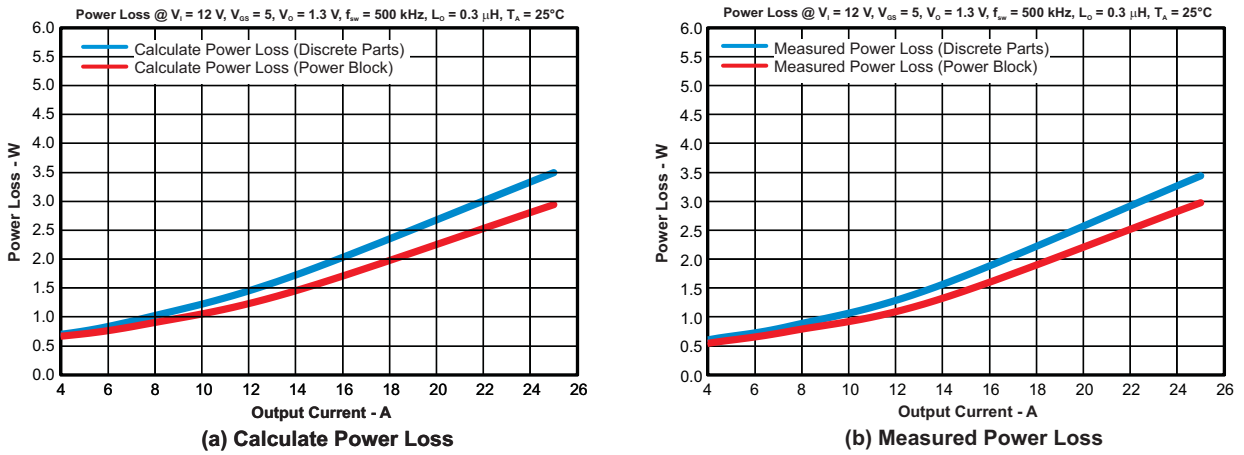

Figure 8. MOSFETs Power Loss in a Synchronous Buck Converter

Figure 8 clearly shows that the equations introduced in this application report can predict the MOSFETs loss in a synchronous buck converter very well. The small difference between the calculated loss and measured loss is due to the inaccuracy of the device parameters and measurement error. Table 2 also

points out that the biggest power loss difference between TI Power Block device and the discrete parts is from the HS FET switching loss. Table 3 and Figure 9 show the different results calculated with the conventional HS FET switching loss equations and the new equations with CSI consideration proposed in this application report. It is clear that the conventional equations underestimate the MOSFETs power loss in synchronous buck converters, and the new equations can give much more accurate results with CSI being considered. As shown Figure 8 and Figure 9, these new calculated results predict the power loss difference due to CSI difference between discrete parts and TI Power Block device. This also explains why TI's NEXFET Power Block products can greatly improve the system efficiency by reducing the key parasitic component – the HS common source inductance.

Table 3. HS FET Switching Loss Calculation With CSI Consideration

	Discrete Solution	Power Block Solution
HS FET Switching Loss (W)	0.41	0.36
HS FET Switching Loss With CSI Consideration (W)	1.18	0.57
Difference (W)	0.77	0.21

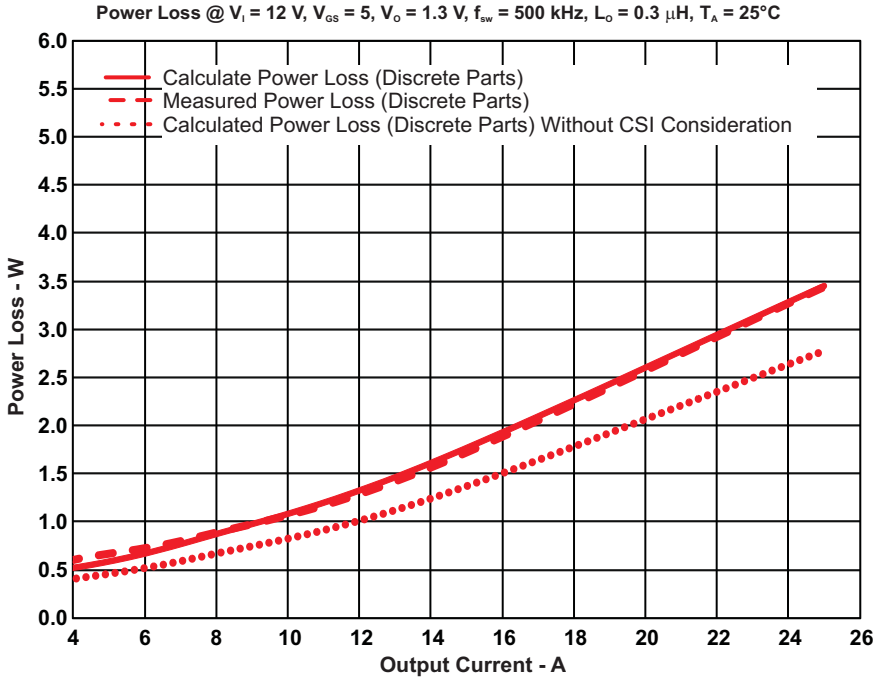

Figure 9. Power Loss Calculation Comparisons With/Without CSI Consideration

6 Summary

This application report analyzes MOSFET-related power loss in synchronous buck converters and presents the detailed calculations for each part of the power loss. The effects of common source inductance also are discussed. The given examples prove that the proposed equations can predict the converter power loss very well. It also shows the impact of CSI on converter power loss: bigger CSI leads to much higher switching loss. In addition, TI Power Block products are introduced. The technical details of why the TI Power Block device outperforms its discrete competition also is explained – minimizing the key parasitic component (CSI) by using advanced device and packaging techniques. In addition, a power loss calculator with CSI consideration based on this application report was built and is available for download.

Appendix A Estimation of Common Source Inductances

The value of common source inductances is determined by the packages of power MOSFETs. Table 4 lists the estimated common source inductance values for several typical packages of low-voltage power MOSFETs. For accurate CSI values, check the device manufacturers.

Table 4. Typical Values of Common Source Inductances

	SOURCE INDUCTANCE
Stacked-Die Power Block/PowerStage	<100 pH
QFN (Clip)	450 pH
QFN (Wire Bonding)	850 pH
SO8	>1.5 nH

Appendix B List of Symbols

SYMBOLS	DESCRIPTION
$C_{oss(HS)}$	HS FET output capacitance
$C_{oss(LS)}$	LS FET output capacitance
D	Converter duty cycle
f_{sw}	Switching frequency
I_{Coss}	LS Coss charge/discharge current
I_{DS}	HS FET drain current
I_g	HS gate current
$I_{g1(on)}$	HS gate current during t1
$I_{g2(on)}$	HS gate current in t2
$I_{g1(off)}$	HS gate current during t4
$I_{g2(off)}$	HS gate current during t3
I_{OUT}	Converter output current
I_{ripple}	Inductor peak- to-peak current ripple
$I_{RHMS(HS)}$	HS FET RMS current
$I_{RHMS(LS)}$	LS FET RMS current
L_{csi}	HS common source inductance
$P_{cond(HS)}$	HS conduction loss
$P_{cond(LS)}$	LS conduction loss
$P_{Coss(HS)}$	HS C_{oss} loss
$P_{Coss(LS)}$	LS C_{oss} loss
$P_{deadtime}$	Diode conduction loss
P_{DRR}	Diode reverse-recovery loss
P_{gate}	Total converter gate loss
$P_{gate(HS)}$	HS FET gate loss
$P_{gate(LS)}$	LS FET gate loss
P_{sw}	MOSFET switching power loss
$P_{sw(HSon)}$	HS FET turnon switching loss
$P_{sw(HSoff)}$	HS FET turnoff switching loss
$Q_{g(HS)}$	HS FET gate charge
$Q_{g(LS)}$	LS FET gate charge
$Q_{gd(HS)}$	HS FET Qgd
$Q_{gs2(HS)}$	HS FET Qgs2
$Q_{oss(LS)}$	LS FET output charge
$Q_{rr(LS)}$	LS body-diode reverse-recovery charge
Q_{sw}	HS FET switching charge
R_{driver}	Gate driver resistance
$R_{dsON(HS)}$	HS FET on-resistance
$R_{dsON(LS)}$	LS FET on-resistance
R_g	HS gate resistance
$R_{g(HS)}$	HS FET gate resistance
$t_{deadtime(r)}$	Rise edge dead-time
$t_{deadtime(f)}$	Fall edge dead-time
V_{Driver}	Gate drive voltage
V_g	HS gate voltage referring to ground
$V_{gs(eff)}$	HS effective gate-source voltage
VIN	Converter input voltage

SYMBOLS	DESCRIPTION
$V_{Lcsi(t1)}$	CSI voltage within t1
$V_{Lcsi(t2)}$	HS CSI voltage during t2
V_{OUT}	Converter output voltage
V_{PL}	HS FET plateau voltage
$V_{PL(HS)}$	HS FET plateau voltage
V_{SD}	Diode forward voltage
V_{sw}	Switch node voltage

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