TEXAS INSTRUMENTS

# The UCC38C42 Family of High-Speed, BiCMOS Current Mode PWM Controllers

Application Note

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**Contents**

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## List of Figures



## List of Tables

# The UCC38C42 Family of High-Speed, BiCMOS Current Mode PWM Controllers

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## 1 Abstract

*Since their introduction in the mid 1980's, the bipolar UC3842 family of Pulse width modulation (PWM) controllers has grown to become the most widely-used control strategy in the power supply industry.[1] The reasons for success are quite clear, the devices feature an elegantly simple yet very effective control architecture, they use only 8 pins, they can drive MOSFET gates directly and they offer superior performance and protection at an affordable price.*

## 2 Introduction

The latest development in the UC3842 based control architecture has been the introduction of enhanced, yet drop-in, replacement devices with features set targeted for much higher frequency applications. The new BiCMOS UCC38C40 through UCC38C45 PWMs are exactly that – they are backwards compatible to the bipolar versions yet are also useable in new designs to one-plus megahertz operation. Delays in all strategic PWM functions have been significantly reduced to match the pace of higher frequency applications. Normally, this is achieved at the expense of higher internal bias currents, yet the new PWMs feature a five-fold reduction in supply current. Other noteworthy improvements have been made to precisely set operating frequency, maximum duty cycle, and output voltage.[2]

### 2.1 UCC38C4x PWM Block Diagram and Overall Description of Operation

The fundamental purpose of using PWM control is to efficiently regulate a power converter stage's output voltage by varying the applied duty cycle of the power switch. The converter's output inductor-capacitor filter stage's long-time constant averages out the applied volt×second product applied by the switch. And as the input line voltage changes, so too does the specific duty cycle required to deliver a constant volt×second product, or pulse width to achieve a regulated output voltage.

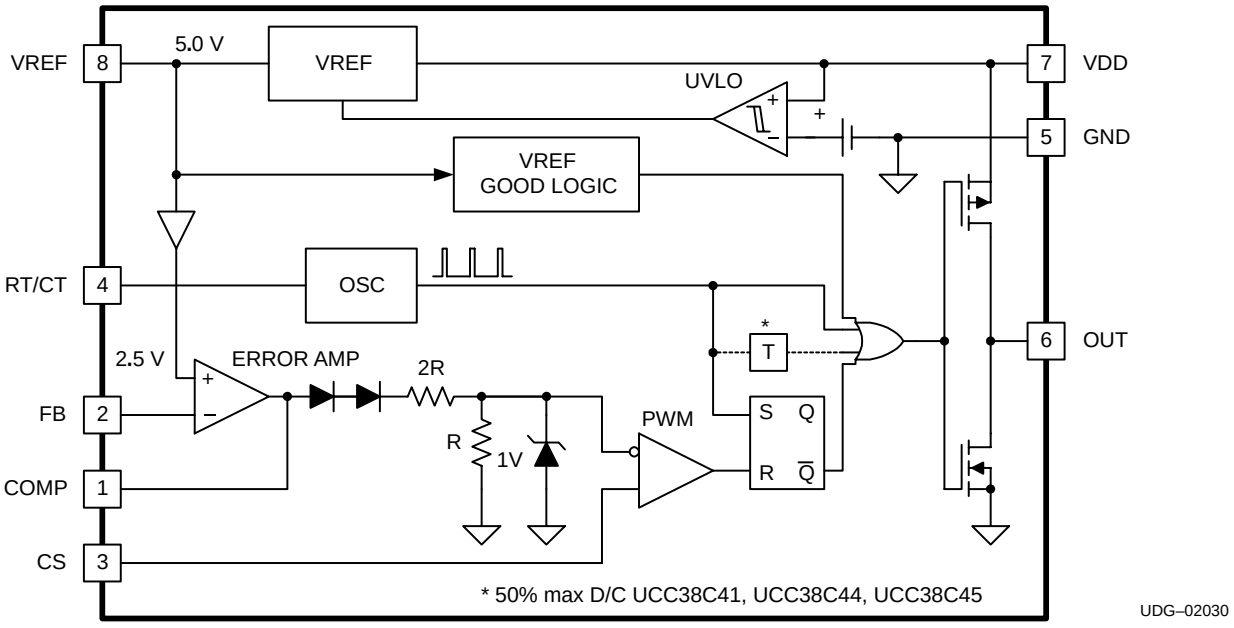


**Figure 1. UCC38C4x Block Diagram**

Determining the exact pulse width needed for a given switching cycle begins with measuring the output voltage. The output voltage is fed into an operational amplifier and compared to a precision 2.5-V reference voltage. Any slight difference between the two inputs, any error, is amplified by the high gain amplifier and feedback network components. Minor differences between the two inputs in the millivolt range result in large swings in the error amplifier's duty cycle controlling output voltage, thus causing the controller's output pulse width to adjust accordingly to correct the output voltage discrepancy.

Current mode control is a more advanced control strategy than conventional duty-cycle control, (voltage mode), and is directly executable with the UCC38C4x devices. Switch current is sensed and applied to the current sense, (CS), pin following some slight noise filtering. With this configuration, the error amplifier output is being compared to primary current waveform, an arrangement that offers several key advantages. Most notably, it makes the converter's power stage resemble a voltage controlled current source. The voltage (error) amplifier defines the level of primary current to be allowed every switching cycle. As the load current changes, so to does the commanding error amplifier output voltage. One first-order effect of this is a simplification of the error amplifier compensation, since the output filter inductor and its associated pole are removed from the loop compensation equation. Current mode control offers other key benefits including instantaneous voltage feedforward of the input voltage and cycle-by-cycle current limiting. When the sensed current exceeds the 1.0-V, (typical), over-current threshold, a high-speed comparator is triggered and the device output is turned off within 35 nanoseconds.

The PWM comparator output is fed into a latch to prevent multiple output pulses from occurring during one switching cycle. This latch is reset at the end of each switching cycle by the oscillator, before initiating the next cycle. A toggle flip-flop is also used on certain devices, (UCC38C41, UCC38C44 and UCC38C45), to absolutely limit the output below 50% duty cycle. On alternating cycles, the toggle flip-flop output directly inhibits the PWM output at the multi-input logic gate.

To drive power a MOSFET directly, the device's output pin, (OUT), houses a fast 1-A peak current totem-pole driver. Also featured within the device is a precision reference voltage used to program the error amplifier noninverting input, the oscillator timing network, internal biases and current sources, under-voltage lockout, and over-temperature protection.

## 2.2 Selecting the Right PWM

Once an operating frequency and maximum duty cycle have been determined, the most suitable PWM for the application should be selected. In most cases, the converter topology selected determines the specific device needed, whether the duty cycle is clamped to 50% maximum, clamped to 100% maximum, or the duty cycle is limited to some number in-between. Applications with a 50% maximum duty cycle, typical of a conventional forward or flyback converter design, should chose a PWM with an internal toggle flip-flop to ensure compliance. On the other hand, buck, boost, and SEPIC converters may require a PWM that can operate out to nearly 100% duty cycle. There are also varieties of forward and flyback converters specifically intended to operate beyond 50% duty cycle, for example 70%, but no higher. Doing so could cause a high voltage reset characteristic if operated beyond the maximum duty cycle limit.

Overall, there are industry needs for all three categories of duty cycle clamped controllers: less than 50%, somewhere greater than 50%, but less than 100%, and those using the full 100% range. To satisfy the <50% applications, three family members, (UCC38C41, UCC38C44, UCC38C45), use a toggle flip-flop between the oscillator and output control logic. With this configuration, the oscillator is programmed to run at twice the intended switching frequency, and only every other pulse can be modulated, and every other pulse is blanked from the output.

The second step in selecting the proper PWM is determining which set of undervoltage lockout (UVLO) thresholds are best suited to the application. Often, this is entirely dependent on the input line voltage and range, and more than one UVLO option may exist. Provided that the minimum input voltage exceeds the maximum turnon UVLO threshold, the amount of UVLO hysteresis affects how quickly the converter's auxiliary bias supply needs to be up and fully functional. Applications requiring a longer soft start period benefit from a wider UVLO hysteresis, whereas those with a brief startup period can opt for less UVLO hysteresis. Note that the desired start-up time, UVLO hysteresis, and startup current affect the supply voltage bulk capacitor value. Sufficient charge must be stored to insure startup before the supply voltage is not drained below the IC's lower UVLO threshold under all start-up conditions.

Three sets of UVLO thresholds are available with the following turnon and turnoff thresholds: 14.5 V/9.0 V, 8.4 V/7.6 V, and 7.0 V/6.6 V respectively. The first set is primarily intended for off-line and 48-V distributed power applications, where the wider hysteresis allows for lower frequency operation and longer soft-starting time of the converter. The second group of UVLO options is ideal for high frequency dc/dc converters typically running from a 12-VDC input. The third, and newest, set has been added to address battery powered and portable applications.[3]

**Table 1. UVLO Options**

| Maximum Duty Cycle | UVLO ON/OFF | Part Number |
|---|---|---|
| 100% | 14.5 V/9.0 V | UCC38C42 |
| 100% | 8.4 V/7.6 V | UCC38C43 |
| 100% | 7.0 V/6.6 V | UCC38C40 |
| 50% | 14.5 V/9.0 V | UCC38C44 |
| 50% | 8.4 V/7.6 V | UCC38C45 |
| 50% | 7.0 V/6.6 V | UCC38C41 |

## 2.3 Comparison of the BiCMOS UCC38C42 to the Bipolar UC3842 Familiy

There are numerous enhancements made to the new BiCMOS family of PWM controllers in comparison to their bipolar predecessors, in lower current consumption, improved accuracy, and higher speed circuitry. A list of the improved key parameters is summarized next.[4]

**Table 2. Improved Key Parameters**

| Parameter | UCC38C42 | UC3842 |
|---|---|---|
| Supply current at 50 kHz | 2.3 mA | 11 mA |
| Start-up Current | 50 μA | 1 mA |
| Over-current propagation delay | 50 ns | 150 ns |
| Reference voltage accuracy | +/– 1% | +/– 2% |
| E/A reference accuracy | +/– 25 mV | +/– 80 mV |
| Maximum operating frequency | > 1 MHz | 500 kHz |
| Output rise/fall times | 25 ns | 50 ns |
| UVLO turnon accuracy | +/– 1 V | +/– 1.5 V |
| Smallest package option | MSOP-8 | SOIC-8 |

# 3 Descriptions of UCC38C4x Pins and Functions by Section

## 3.1 Powering the Device

Once the device best suited for the application has been selected, the next step in the design process is to properly supply power. First, note the absolute maximum supply voltage rating of these devices is 20 VDC, and that includes all noise spikes and transient conditions. If containing the start-up and bootstrap supply voltage below 20 V under all line and load conditions cannot be achieved, then it is advised to use a zener protection diode from the supply to ground. Depending on the impedance and arrangement of the bootstrap supply, this may require adding a resistor in series with the bootstrap winding to limit current into the zener as shown in Figure 3. Insure that overall tolerances and temperatures the minimum zener voltage is higher than the highest PWM UVLO upper turnon threshold.[5]

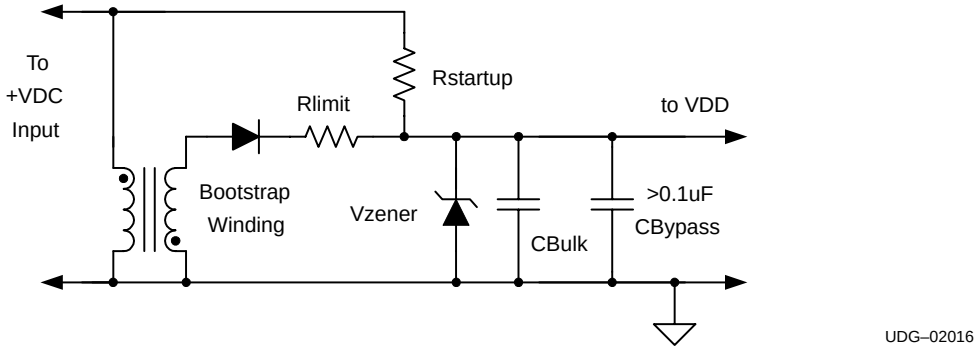


**Figure 2. UCC38C42**

The start-up resistor should be sized to supply more current than the three source of sinking currents, which are: the maximum PWM startup current, (100 μA), the bias supply capacitor network's maximum leakage current over temperature, and finally, the amount of current required to charge the bias capacitor network. Simply supplying 100 μA, the maximum device start-up current does not insure the bias supply capacitor will ever charge, the current could all go to the device, in which case the supply voltage would not rise. The associated power loss for increasing the start-up current is nearly insignificant. Even from a high voltage PFC input, an additional 100 μA of start-up current amounts to a mere 37-mW of power lost. As for calculating the start-up time interval, factor in the tolerance of the bulk storage capacitor, typically +/–20%, or more, depending on the type used.

The UCC38C4x VDD supply must be bypassed as close to the device's supply pins as possible with at least a 0.1-μF capacitor, and a ceramic type is preferred. Higher values may empirically work better depending on the amount of noise generated by the bootstrap winding. When laying out any printed-circuit board, the design should take into consideration the need for this capacitor to be as physically close to the respective pins.

## 3.2 Reference Voltage

Each member of the UCC38C4x family contains a precision 5-V reference voltage that performs several important functions. The reference voltage is divided down internally to 2.500 V +/–1% and connected to the error amplifier's noninverting input for accurate output voltage regulation. Other duties of the reference voltage are to set internal bias currents and thresholds for functions such as the oscillator upper and lower thresholds along with the overcurrent limiting threshold. The reference voltage must be bypassed with at least a 0.1-μF capacitor, and a ceramic type is recommended here too. Placement of this capacitor on the physical printed-circuit board layout should be as close as possible to the respective VREF and GND pins as possible.

Other uses of this precision reference are for external circuitry such as driving an optocoupler feedback network in isolated converters. Internal short circuit current limiting is set to 55 mA maximum, and all VREF dependencies upon line, load and temperature are listed in the data sheet.

## 3.3 Oscillator

The UCC38C4x oscillator design incorporates a trimmed discharge current to accurately program maximum duty cycle and operating frequency. In its basic operation, a timing capacitor, (CT), is charged by a current source, formed by the timing resistor, (RT), connected to the device's reference voltage, VREF. The oscillator design incorporates comparators to monitor the amplitude of the timing capacitor's voltage. The exponentially shaped waveform charges up to a specific amplitude representing the oscillator's upper threshold of 3.0 V. Once reached, an internal current sink to ground is turned on and the capacitor begins discharging. This discharge continues until the oscillator's lower threshold has reached 0.70 V at which point the current sink is turned off. Next, the timing capacitor starts charging again and a new switching cycle begins.

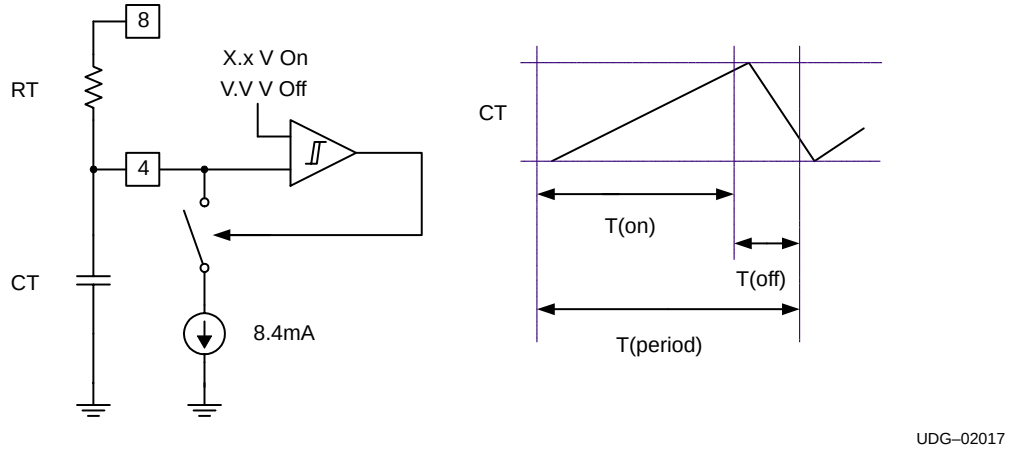


**Figure 3. Oscillator Diagram**

While the device is discharging the timing capacitor, resistor RT is also still trying to charge CT. It is the exact ratio of these two currents, the discharging versus the charging current, that specifies the maximum duty cycle. Note that during the discharge time of CT, the device's output is always off. This represents an ensured minimum off time of the switch, commonly referred to as *deadtime*. To program an accurate maximum duty cycle, use the information provided in Figure 5 for maximum duty cycle versus oscillator frequency. Any number of maximum duty cycles can be programmed for a given frequency by adjusting the values of RT and CT. Once RT is selected, the oscillator timing capacitor can be found using the curves in Figure 6. However, since resistors are available in more precise increments, typically 1%, and capacitors are only available in 5% accuracy, it might be more practical to select the closest capacitor value first and then calculate the timing resistor value next.[6]

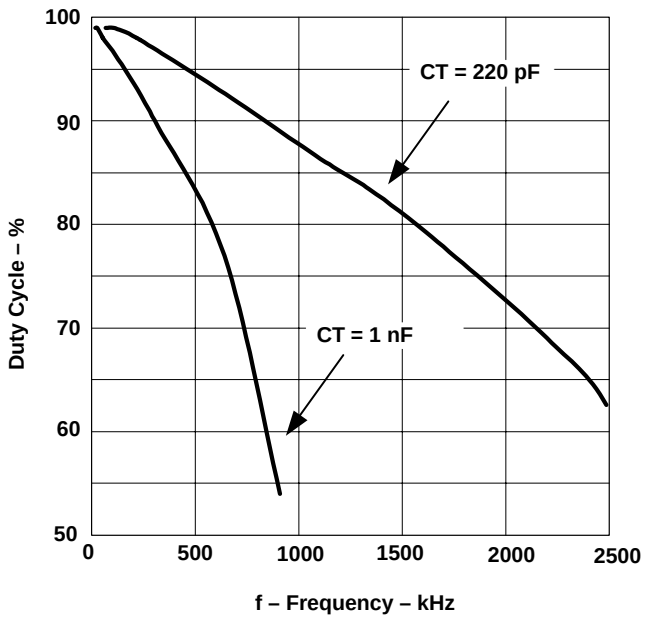


**Figure 4**

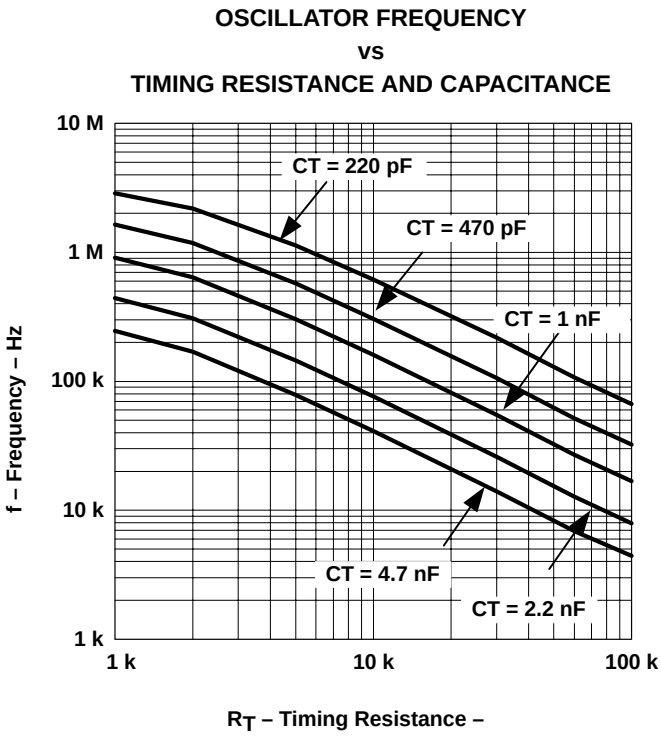


**Figure 5**

## 3.4 Oscillator Printed Circuit Board Layout and Component Selection Notes

Probably the single most critical item in a PWM controlled printed-circuit board layout is the placement of the timing capacitor. While both the supply and reference bypass capacitor locations are important, the timing capacitor placement is far more critical. Any noise spikes on the CT waveform due to lengthy printed circuit trace inductance or *pick-up* noise from being in proximity to high power switching noise causes a variety of operational problems. Dilemmas vary from incorrect operating frequency caused by pretriggering the oscillator due to noise spikes to frequency jumping with varying duty cycles, also caused by noise spikes. The placement of the timing capacitor should be treated as the most important layout consideration.

As for component characteristics, the switching frequency changes as the timing capacitor value varies with initial accuracy and temperature. Therefore, it is best for the timing capacitor to have a flat temperature coefficient, typical of most *COG* or *NPO* type capacitors. The exact composition of the timing capacitor used is not critical, whether polypropylene, metallized polyester, monolithic ceramic, or multilayer ceramic are used. All are excellent choices provided that their equivalent series inductance, (ESL), is negligible. Keep PC traces as short as possible to minimize added series inductance.

## 3.5 Error Amplifier

The error amplifier has its noninverting input internally tied to a precise 2.5-V threshold, plus-or-minus 1% accuracy. The inverting input gets connected to the output voltage under regulation scaled to this 2.50-V input level. This is a classic type operational amplifier and the gain and loop compensation network is connected from the amplifier output back to the inverting input, further detailed in the applications section of this document. Typical characteristics are an open loop gain of 90-dB and a 1.5-MHz gain×bandwidth product. The output can typically source 1 mA and typically sinks 14 mA.

## 3.6 Current Sense and Over-Current Limit

Cycle-by-cycle pulse width modulation performed at the PWM comparator essentially compares the error amplifier output to the current sense input. This is not a direct volt-to-volt comparison, as the error amplifier output network incorporates two diodes in series with a resistive divider network before connecting to the PWM comparator. The reason behind the two diodes drop is to be able to achieve zero duty cycle with a *low* amplifier output. Accounting for slight differences in the amplifier's input offset voltages and high gain stage, one uncomplicated solution is to use an offset voltage to accommodate these parameters and still achieve zero duty cycle. That is exactly what the voltage drop of the two diodes performs in circuit; it acts as an offset voltage. The *2R/R* resistive divider facilitates the use of a wider error amplifier output swing that can be more symmetrically centered around the 2.5-V noninverting input voltage.

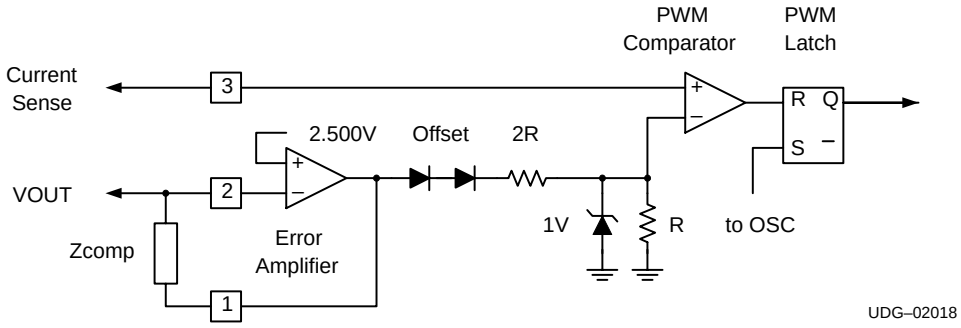


**Figure 6. Error Amplifier and Current Sense Circuitry**

Note the 1-V zener diode associated with the PWM comparator's input from the error amplifier. This is not an actual diode in the device's design, but an indication that the maximum current sense input amplitude is 1-V typical. When this threshold is reached, regardless of the error amplifier output voltage, cycle-by-cycle current limiting occurs, and the output pulse width is terminated within 35 nanoseconds (typical). According to the UCC38C42 data sheet specifications, the minimum value for this current limit threshold is 0.9 V with a 1.1 V maximum. In addition to the tolerance of this parameter, the accuracy of the current sense resistor (or current sense circuitry) must be taken into account. It is advised to factor in the worst case of primary and secondary currents when sizing the ratings and worst-case conditions in all power semiconductors and magnetic components.

## 3.7 Totem Pole, Gate Drive Output

Driving the gates of larger power MOSFETs successfully at high frequency requires high peak current capability and fast transitions from the driver. But peak current is typically rated by many integrated circuit manufacturers as the maximum current capability when the load is at one of the supply rails and the driver is at the opposite supply rail. For example, a 1-A peak rating applies to a device using a 12-V supply and having a 12-Ω output impedance driving a fully discharged capacitor. For a brief instant the device delivers its rated one amp peak current. However, for the rest of the turn-on interval, the available current is an exponentially decaying current driven from 12-V through 12-Ω, and not one amp peaks during the entire interval. The instantaneous current is the 12-V supply minus the gate (capacitor) voltage divided by the 12-Ω impedance. Users should be aware of the driver peak current specifications, interpretations, in-circuit performance, and effects upon switching speed. It is more beneficial to the designer to know the actual impedance of the output stage rather than its peak current capability.

The UCC38C4x family houses unique totem pole drivers exhibiting a 10-Ω impedance to the upper rail and a 5.5-Ω impedance to ground, typically. This reduced impedance on the low side switch helps minimize turnoff losses at the power MOSFET, whereas the higher turnon impedance of the high side is intended to better match the reverse recovery characteristics of many high-speed output rectifiers. Transition times, both rising and falling edges, are typically 25 nanoseconds for a 10% to 90% change in voltage.

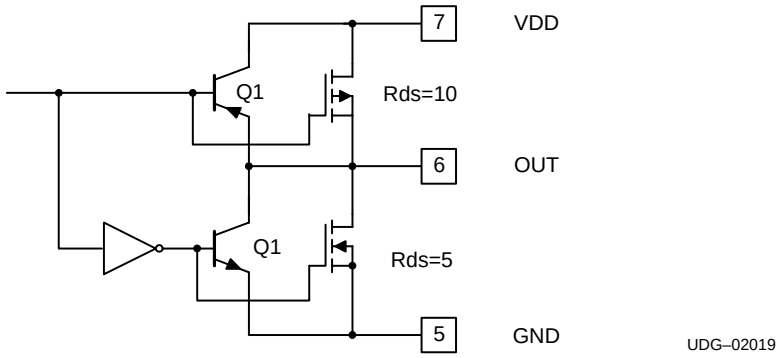


**Figure 7. Output Totem Pole Configuration**

The totem-pole output is actually comprised of a combination of a low impedance MOS structure in parallel with a bipolar transistor, or BiCMOS construction. This more efficient utilization of silicon delivers the high peak current needed along with sharp transitions and full rail-to-rail voltage swings. Furthermore, the output stage is a self-biasing, active low during under-voltage lockout type. With no VDD supply voltage present, the output actively pulls low if an attempt is made to pull the output high. This condition frequently occurs at initial power-up with a power MOSFET as the driver load.

Users have the option to supplement the internal drivers with external ones, such as from the TPS28xx and UCC3732x families of dual, high-current gate driver devices

## 3.8 Packaging Options and Thermal Issues

Standard plastic dual-in-line packaging in both thru-hole, (PDIP-8), and surface mountable, (SOIC-8), are available along with a new small outline surface mount option MSOP-8 package for size constrained applications. The maximum power dissipation for each and junction-to-ambient factors are listed below. Note that the smallest package MSOP-8 has the best thermal ratings.

**Table 3. Maximum Power Dissipation**

| Package | Total Pdiss |
|---|---|
| PDIP-8 | 350 mW |
| SOIC-8 | 650 mW |
| MSOP-8 | 850 mW |

† At 25 degrees C

## 3.9 Open Loop Test Circuit

A simple, open loop test circuit is shown in Figure 8 for evaluating the operation of these devices along with enabling verification of numerous parameters. A legacy, bipolar UC3842 specification calling for an oscillator frequency of 50 kHz is used. All UCC38C42 test conditions and parameters listed in the data sheet reference this frequency for a clear comparison between the two devices.

A voltage follower from the timing capacitor develops an exponential waveform for use as an input to the current sense pin. Ideally this would incorporate a linear sawtooth waveform, but this approximation suffices. A transistor is used as a buffer so the circuitry does not load down the oscillator and cause a shift in frequency. Two potentiometers provide the handles to separately adjust the levels of current and voltage for comparison. Each can be adjusted to simulate different levels of primary (load) current and input line voltage.

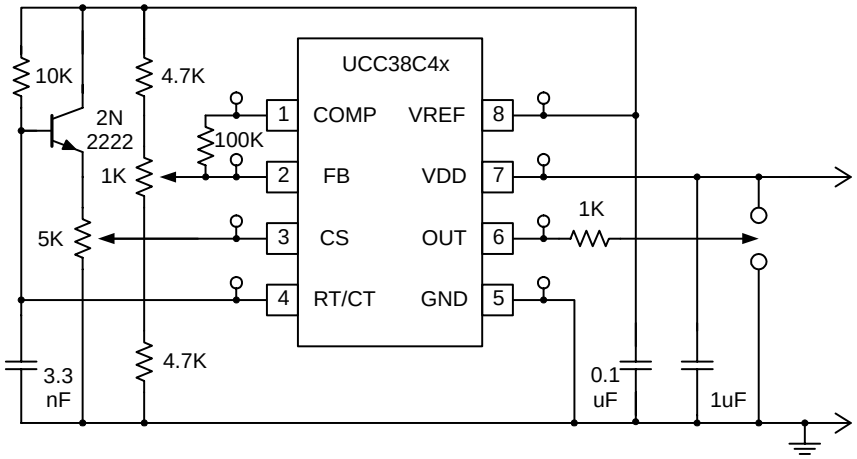


**Figure 8. Open Loop Test Circuit**

# 4 Applications Section[7]

## 4.1 Synchronization

Synchronization is best achieved by forcing the timing capacitor voltage above the oscillator's internal upper threshold. There are a variety of techniques available, but the most common method is to insert a resistor in series with the lower side of the timing capacitor. The other end of the resistor is connected to ground, then a brief pulse is applied across the resistor when synchronization is desired for each cycle. The amplitude needs to be capable of driving the capacitor voltage high enough to cross the upper comparator threshold. This is a function of the worst mismatch between the PWM's lowest free-running frequency and that of the highest incoming synchronization stream.

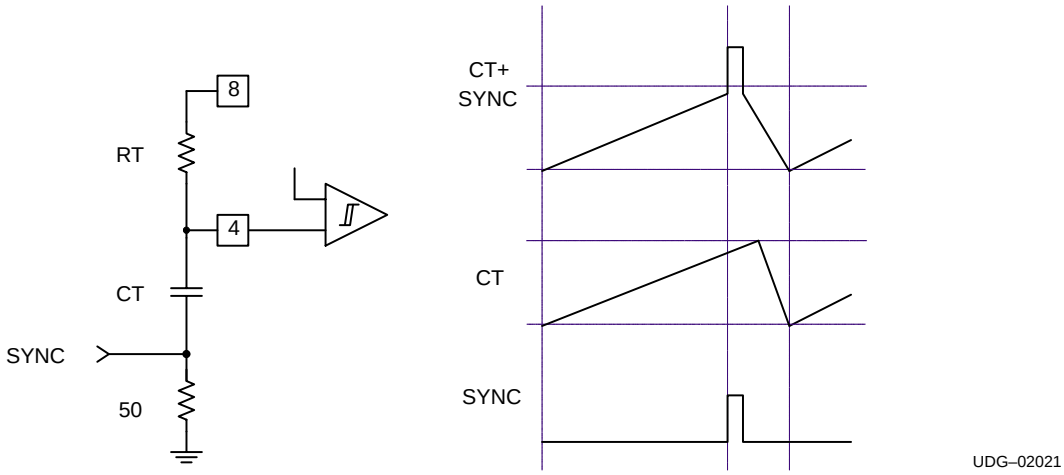


**Figure 9. SYNC**

## 4.2 Current Sense Filter Networks

Typically, the direct current sense signal contains a large amplitude leading edge spike associated with the turnon of the main power MOSFET, reverse recovery of the output rectifier, and other factors including charging and discharging of parasitic capacitances. In many cases, the peak amplitude of the noise grossly exceeds the maximum amplitude of the actual current sense signal, so additional filtering is required. In its simplest form, a series resistor and capacitor network is added to suppress the leading edge spike. However, adequate time to discharge the capacitor each cycle must be available, and the common 1-kΩ series resistor is often too high of a value to properly facilitate this. The filter capacitor can begin charging from some residual voltage each cycle, which may not provide enough filtering under all line and load combinations.

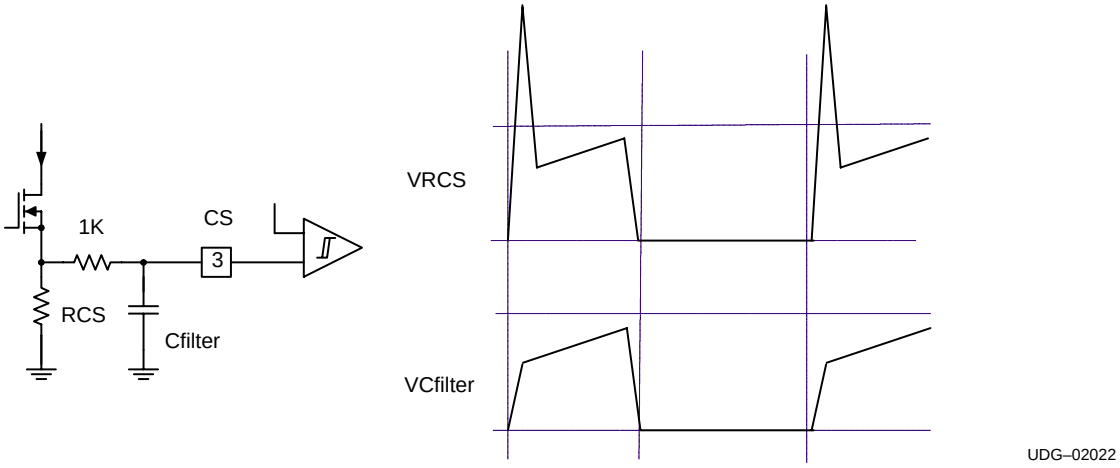


**Figure 10. R/C Filters**

Another example of a current sense filtering uses a transistor to discharge the filter capacitor to get more predictable filtering each cycle. The transistor can also be used to provide intentional leading edge blanking of the current sense signal. One implementation is to capacitively couple the gate to the device's PWM output. When the output turns on, the sharp edge is coupled into the N channel's gate turning it on, so sufficient gate voltage must be generated. The gate to source resistor is used to discharge the gate, and the values of these two components can be adjusted to provide a specific period of leading edge blanking.

While these techniques aid in current sense filtering, note that these interfere with the device's fast over-current protection circuit, and they add delays to sensing instantaneous current. It is therefore imperative to evaluate the operation of these circuits under overload and short-circuit conditions for potential side effects of delayed fault response.

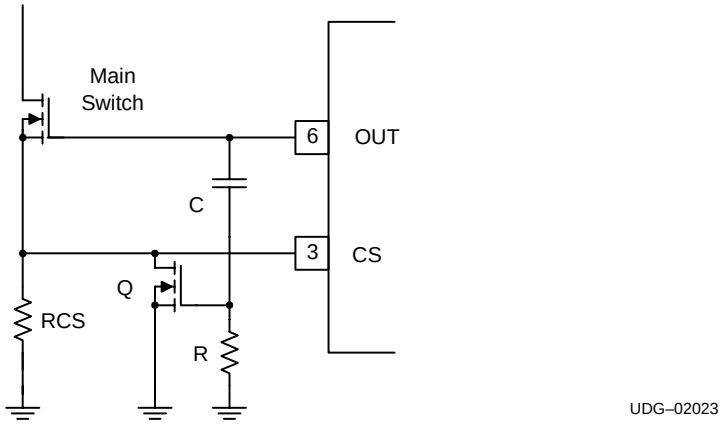


**Figure 11. Current Filtering / Leading Edge Blanking Implementations**

## 4.3 Soft Start Techniques

Soft start is the technique to gradually power up the converter in a well-controlled fashion by slowly increasing the effective duty cycle to the switch starting at zero and gradually rising. Following start-up of the PWM, among other things that are becoming initialized, the error amplifier inverting input is low commanding the error amplifier's output to go high. The output stage of the amplifier can source 1 mA typically, which is plenty to drive most high impedance compensation networks, but not hefty enough for driving large loads quickly. Soft start is achieved by charging a fairly large value >1-µF capacitor connected to the error amplifier output through a diode as shown in Figure 12.

The limited charging current of the amplifier into the capacitor translates into a dv/dt limitation on the error amplifier output. This directly corresponds to some maximum rate of change of primary current in a current mode controlled system as one of the PWM comparator's inputs gradually rises. Note that soft start performs a different, frequently preferred function in current mode controlled systems than it does in voltage mode control. In current mode, soft start controls the rising of the peak switch current. In voltage mode control, soft start gradually widens the duty cycle, regardless of the primary current or rate of ramp-up.

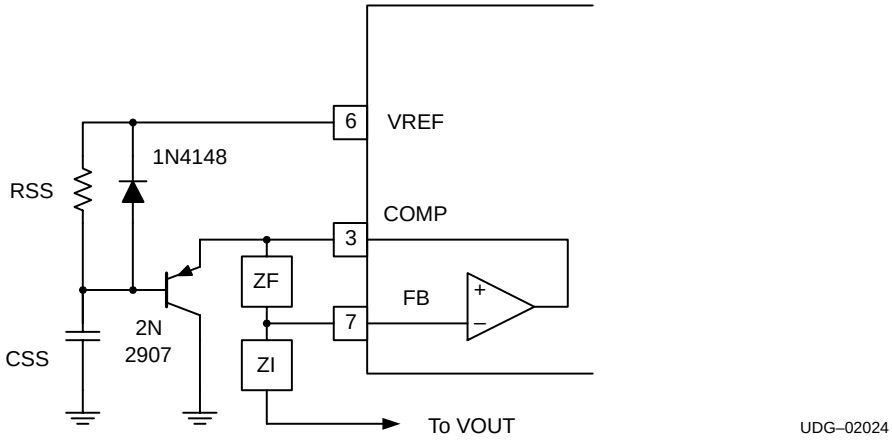


**Figure 12. Soft Start Implementation**

The purpose of the resistor and diode is to take the soft start capacitor out of the error amplifier's path during normal operation, once soft start is complete and the capacitor is fully charged. Another diode should be added across the resistor back to the device's reference voltage. This diode discharges the soft start capacitor every time the PWM goes through an under-voltage lockout condition that forces the device's reference voltage low. This circuit prevents against a *hard* start-up following a brief *brownout* condition.

## 4.4 Bias Supplies

Many designers have successfully masterminded auxiliary bias supplies that intentionally fail upon overload conditions. As soon as a fault is placed on the main output, the coupled bias winding fails to generate sufficient bias voltage and thus collapses. The dropping supply voltage quickly forces the PWM to go through an under-voltage lockout condition, thus turning everything off and restarting the system. This technique is useful in reducing overall power dissipation and semiconductor stress during overloads. It additionally performs as a restart delay function following a fault, a desirable mode of operation. Use the circuit of Figure 2 with the bias winding coupled very closely to the main output winding.

## 4.5 Voltage Mode Control

In certain applications, straight-forward voltage mode control may be a preferred control strategy for a variety of reasons. That being the case, voltage mode control is easily executable with any current mode controller, especially the UCC38C4x family members. Implementation requires generating a 0-V to 0.9-V sawtooth shaped signal to input to the current sense pin, (CSNS), which is also one input to the PWM comparator. This is compared to the divided down error amplifier output voltage at the other input of the PWM comparator. As the error amplifier output is varied, it intersects the sawtooth waveform at different points in time, thereby generating different pulse widths. This is a straightforward method of linearly generating a pulse whose width is proportional to the error voltage.

Implementation of voltage mode control is possible by using a fraction of the oscillator timing capacitor (CT) waveform. This can be either resistively or capacitively divided down and fed to the current sense pin as shown in Figure 14. A small transistor is used to buffer the oscillator timing components from the loading of the resistive divider network. Due to the offset of the oscillator's lower timing threshold, a dc blocking capacitor is be added.

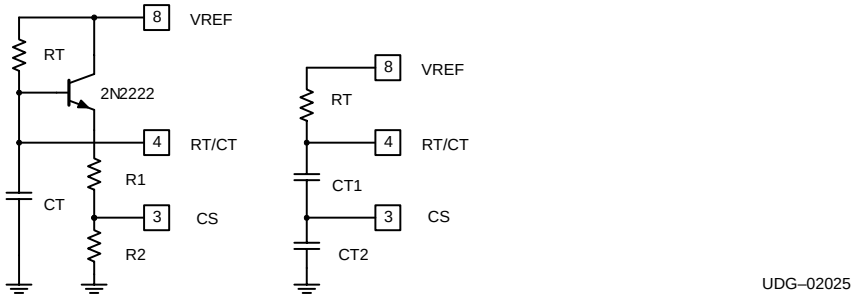


**Figure 13. Voltage Mode Control Implementation**

The oscillator timing components should be selected to approximate as close to a linear sawtooth waveform as possible. Although exponentially charged, large values of timing resistance and small values of timing capacitance help approximate a more linear shaped waveform. This may not be possible, however, if an accurate maximum duty cycle clamp also needs to be programmed at the oscillator. In this situation, the result is that the modulator gain is not be entirely linear over the complete range of adjustment – something that the designer should take into consideration when compensating the overall converter. The general scheme for compensating a voltage mode controlled buck derived converters is shown in Figure 14.

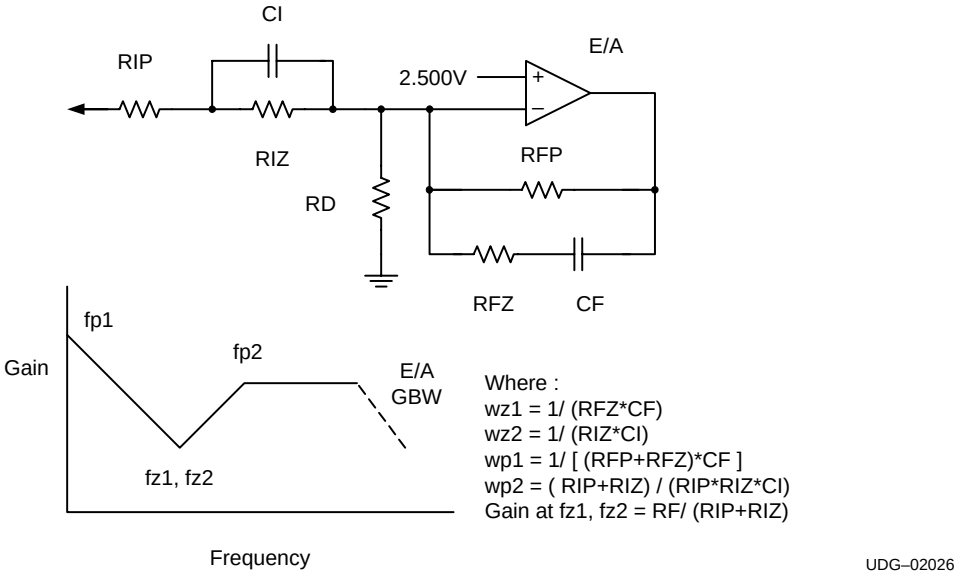


**Figure 14. Voltage Mode Control Overall Compensation for Buck Derived Converters**

# 5 Current Mode Control – Overall Compensation and Implementation

## 5.1 Practical Considerations: Tricks and Alternative Techniques

### *5.1.1 Biasing-up the current sense signal*

In some applications, especially where high efficient is required, when low input voltages are used or when voltage mode control is preferred, it may not be practical to develop the ideal 0.9-V amplitude current sense signal. And when overcurrent limiting is essential to the design, other options deserve consideration. The circuit shown in Figure 15 uses a resistor divider network from the current sense signal to the device's reference voltage to *bias-up* the current sense voltage. This technique still achieves current mode control with cycle-by-cycle over-current protection. Note that because of the lower peak-to-peak amplitude current sense signal, the PWM modulator gain increases since a lower change in error amplifier output voltage is required to span the complete no-to-full load current range.

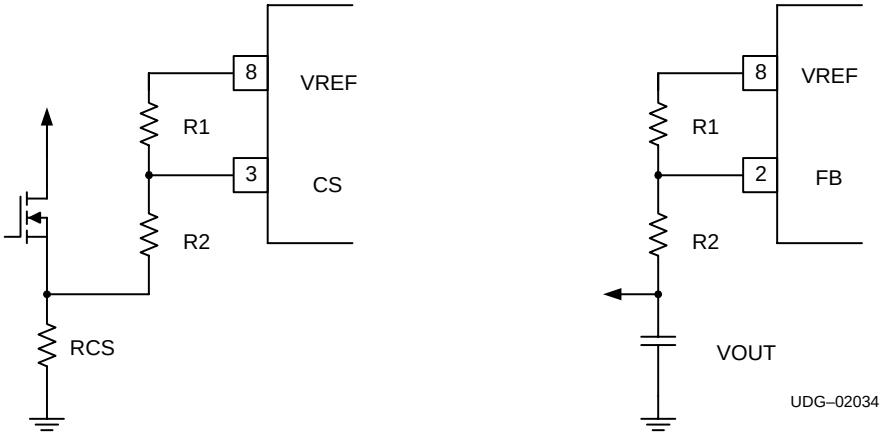


**Figure 15. Cycle-by-Cycle Over-Current Protection and E/A Biasing for $V_O$ <2.5 V**

### *5.1.2 Biasing-up the output feedback voltage – for use with output voltages < 2.5 V*

The UCC38C4x family error amplifier noninverting input is internally tied to a precision 2.5-V reference voltage. It may first appear unclear as to how to use these PWMs with output voltage below the 2.5-V reference. However, the output voltage feedback voltage can just as easily be *biased-up* to the device's reference voltage as it can be divided down to ground, which is just another reference voltage of zero volts. Provided that the device's 5.0-V reference is stable, which it is, it can similarly be used to modify the output voltage feedback amplitude up to the required 2.5-V level. Implementation is shown in Figure 15 using the feedback pin instead of the current sense input. Also note that the resistors used in the divider networks have NO impact whatsoever on the gain. Details can be found in Reference 4. Implementation is shown in Figure 15 by using resistors from VOUT to VREF.

## 5.2 Enable / Disable

There are a few ways to enable or disable the UCC38C4x devices, depending on which type of restart is required. The two basic techniques use external transistors to either pull the error amplifier output low (< 2 $V_{BE}$) or pull the current sense input high (<1.1 V). If a soft start following the enable is desired, then the error amplifier circuit works best as the soft start capacitor is discharged by the external N channel logic level FET and diode following a re-enabling. If no soft start is required then the diode is not used and the amplifier most likely immediately goes to its upper rail voltage trying to achieve regulation of the output. Another choice for restart without a soft start is to pull the current sense input above the cycle-by-cycle current limiting threshold. A logic level P-channel FET from the reference voltage to the current sense input can be used. Placing a MOSFET between the device ground pin and actual circuit, (electrical), ground to facilitate the enable function is not recommended. Large noise spikes from turnoff of the output transistor can create problems with the sensitive analog circuits.

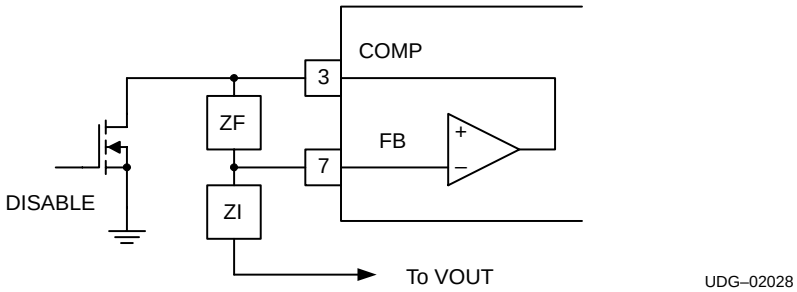


**Figure 16. Enable Circuit**

## 5.3 Slope Compensation

With current mode control, slope compensation is required to stabilize the overall loop with duty cycles exceeding 50%. Although not required, slope compensation also improves stability in applications using below a 50% maximum duty cycle. Slope compensation is introduced by injecting a portion of the oscillator waveform to the actual sensed primary current. The two signals are summed together at the current sense input (CSNS) connection at the filter capacitor. To minimize loading on the oscillator, it is best to buffer the timing capacitor waveform with a small transistor whose collector is connected to the reference voltage. The timing resistor should be broken into two resistors in series with the center-point connected to the transistor's base. This configuration develops more voltage across the slope compensation resistor than others techniques and produces better results.

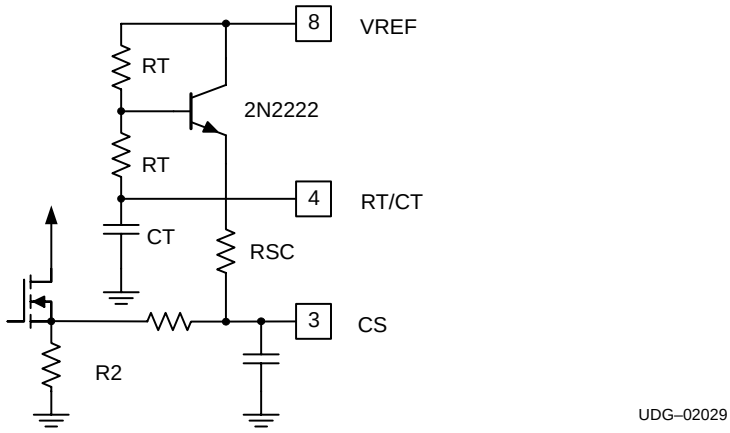


**Figure 17. Slope Compensation**

# 6 Summary

The latest generation of feature-enhanced, high-speed, low-current PWM controllers using the industry standard UC3842 based control architecture are described. Like their predecessors, these devices are ideal solutions to general-purpose, power management applications in the low to medium power levels. This popular control strategy has withstood the test of time in the power supply industry and has now been upgraded to address ongoing higher frequency applications.

# 7 References

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