Application Report
SLVA673A – November 2014 – Revised April 2014

Robust Hot Swap Design

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ABSTRACT

A Hot Swap is usually placed on the input of a plug-in card to manage inrush current and to protect the main bus and the load during faults. Hot-Swap applications place a lot of stress on the MOSFET used as a pass element and a major challenge is to ensure that it is safely operated under all possible conditions. First, this application note discusses key principals and considerations for Hot Swap design. Then a design procedure is outlined using the LM5066I as an example. This procedure is implemented for the design calculators of the following parts: LM25066, LM5066, LM5066I, LM5067, LM5069, TPS24710, and TPS24720. It is recommended to use these calculators for designing Hot Swaps and this application note is meant to describe and justify the procedure used for these tools.

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1 Introduction and Related Material

The focus of this application note is to provide guidelines for ensuring safe MOSFET operation in Hot Swap circuits. Similar topics have been covered in the following application notes from TI: "Selecting Transistors for Hot-Swap Applications"[1] and "Hot Swap Design Using TPS2490/91 and MOSFET Thermal Response"[2]. Both of these works are a solid starting point for learning about Hot Swap design and a similar framework is used here. However, as the power levels continue to rise and designers attempt to squeeze the most out of their MOSFETs there are additional considerations that are introduced in this work:

- Limitation on how low of a power limit Hot-Swap controllers can support
- Using output dv/dt control methods
- Additional techniques for estimating MOSFETs stress capability for non-constant power and intermediate time frames
- Many low R_{DSON} MOSFETs do not have constant power safe operating area (SOA) curves and the thermal transient impedance is not the ideal for estimating stress-handling capabilities
- Using multiple MOSFETs

TI offers Excel-based calculators for Hot Swap with power limiting that follow the approach outlined here. Thus, engineers that want to understand the implementation and reasoning behind these tools will find the information in this application note to be most relevant. Finally, the complete design examples of the LM5066I demonstrate how these principals should be applied.

In addition to MOSFET stress consideration, the TVS selection is another critical area of Hot Swap design. Refer to the "TVS Clamping in Hot-Swap Circuits"[3] article for an in-depth discussion on this topic.

2 Key Considerations for Hot Swap Design

2.1 Hot Swap Controllers with FET SOA Protection

To ensure that the MOSFET stays within its SOA during start-up and fault recovery, many of TI's controllers implement the FET power-limiting feature. The active control loop will regulate the gate to ensure that the current through the MOSFET and the power dissipation of the MOSFET is below their respective pre-programmed thresholds. The maximum current allowed through the MOSFET (I_{LIM}) is determined with Equation 1. $I_{LIM,CL}$ is the programmed current limit, P_{LIM} is the programmed power limit, and V_{DS} is the drain-to-source voltage across the Hot Swap MOSFET.

$$I_{LIM} = MIN(I_{LIM,CL}, \frac{P_{LIM}}{V_{DS}}) \quad (1)$$

This results in an IV curve shown in Figure 1. $I_{LIM,PL}$ denotes the maximum allowed MOSFET current (I_{DS}) when the part is in power limit. As V_{DS} increases, $I_{LIM,PL}$ decreases and $I_{LIM,PL,MIN}$ denotes the lowest $I_{LIM,PL}$, which occurs at the largest V_{DS} ($V_{DS,MAX}$). The controllers enforce this by regulating the voltage across R_{SENSE} (V_{SENSE}). $V_{SNS,PL}$ denotes V_{SENSE} when power limiting is active. Similarly to $I_{LIM,PL}$, $V_{SNS,PL}$ decreases as V_{DS} increases and $V_{SNS,PL,MIN}$ corresponds to the lowest $V_{SNS,PL}$, which occurs at $V_{DS,MAX}$.

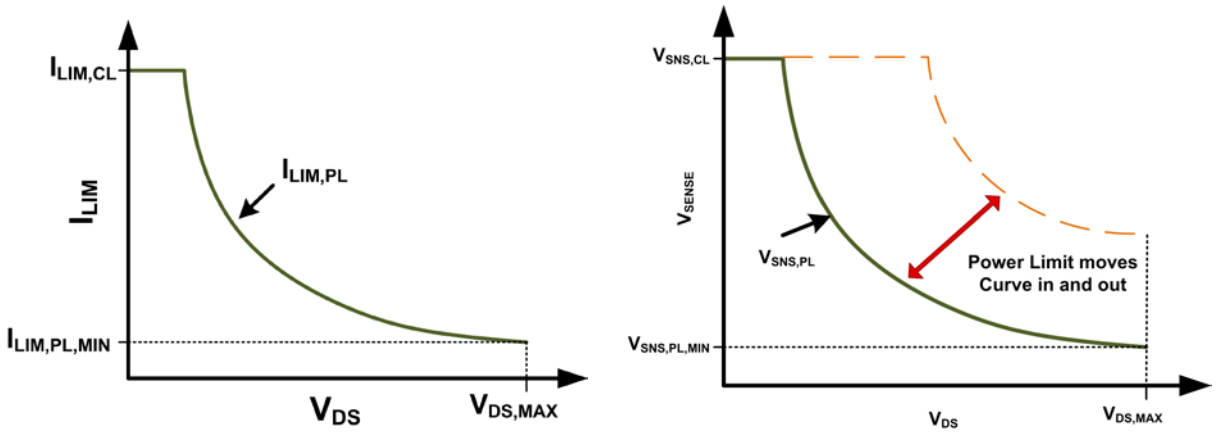

Figure 1. Operation of Power Limit Engine

Note that as $V_{SNS,PL,MIN}$ decreases, there is less signal and thus the error due to offsets increases. To ensure proper operation, most controllers will have a minimum recommended $V_{SNS,PL,MIN}$ that should be adhered to. The $V_{SNS,PL,MIN}$ can be computed with Equation 2. As higher power, high efficiency designs are attempted with small FETs there is a push to reduce P_{LIM} (less stress on FET), reduce $V_{SNS,CL}$ (better efficiency), and increase $I_{LIM,CL}$ (support larger load current). All of these will reduce $V_{SNS,PL,MIN}$ and the designer must be careful to ensure that it is not too low.

$$V_{SNS,PL,MIN} = \frac{P_{LIM} \times V_{SNS,CL}}{V_{DS,MAX} \times I_{LIM,CL}} \quad (2)$$

2.2 Understanding MOSFET Stress in Hot Swap Applications

To ensure a robust Hot Swap, the MOSFET stress should never exceed its ratings. To achieve this goal, one must first understand the different test conditions and the stress they cause on the MOSFET. The following are the three key scenarios to consider:

- Start-up
- Hot-short - Output of a Hot Swap is shorted to ground when the Hot Swap is on
- Start-up into short - Powering up a board when the output and ground are shorted

2.2.1 Hot Swap with only Power Limit

For many applications the design relies on power limit and current limit. The timer is used to shut off the FET if the stress duration exceeds the pre-set duration.

Figure 2 shows a start-up into a purely capacitive load. The Hot Swap will regulate the Hot Swap MOSTFET's gate to maintain a power dissipation which is under the power limit and keep the input current under the current limit. Note that the inrush current increases as V_{OUT} increases, because the V_{DS} of the MOSFETs will decrease. The start time can be computed with Equation 3. Note that the Hot Swap will be in power limit or current limit during most of the start-up and hence one should assume that the timer will run during the entire start-up. Therefore, the timer should be sized larger than T_{START}. The stress on the MOSFET is roughly P_{LIM} watts for T_{START} milliseconds.

$$T_{START} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right] \quad (3)$$

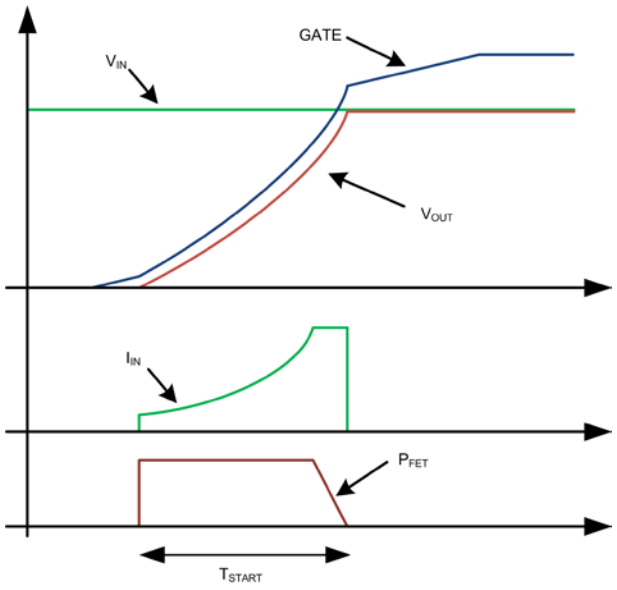

Figure 2. Start-up with only Power Limit

Next, consider start-up into Short. In this case, V_{OUT} starts out shorted to ground and the controller will again regulate the gate to maintain constant power in the FET. Since V_{OUT} = 0 V, the V_{DS} of the FET equals V_{IN}, the inrush current equals P_{LIM}/V_{IN}. The Hot Swap will regulate the gate until the timer expires. Thus, the stress on the MOSFET is roughly P_{LIM} watts for T_{TIMER} seconds. Note that the T_{TIMER} is larger than T_{START}, so this test condition will be more stress than a regular start-up.

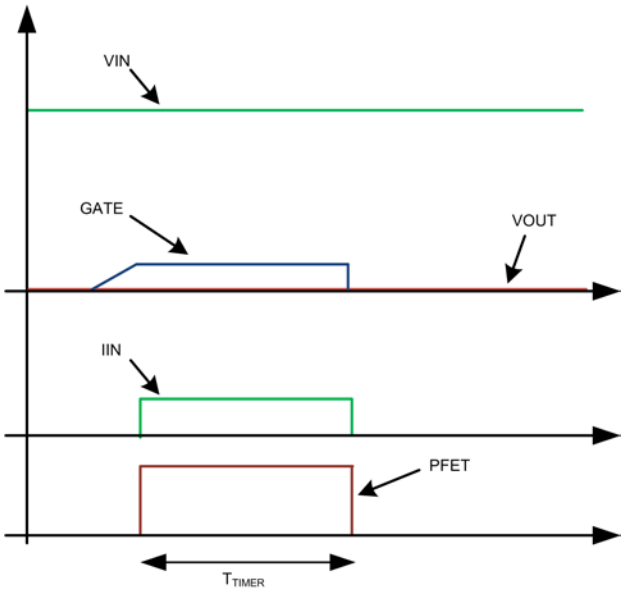

Figure 4. Start-up into Short

Finally, consider the hot-short. In this case, V_{OUT} is shorted to ground and the controller will quickly pull down the gate and then re-start the gate into regulation to maintain constant power in the FET. The power level and duration is the same as the previous test. However, the FET will usually start out being hotter (due to load current) and thus this is considered the most stressful event.

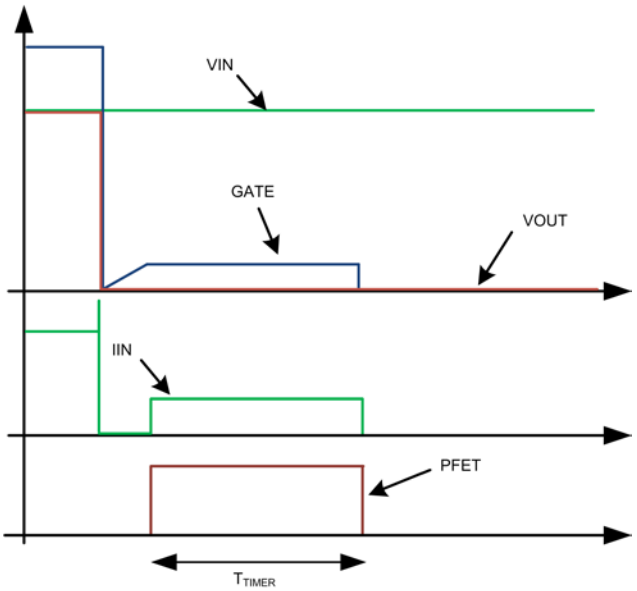

Figure 5. Hot Short

To summarize, the following applies for designing Hot Swap with just power limit:

- Timer size is driven by start time.
- Worst-case FET stress is P_{LIM} watts for T_{TIMER} seconds.

2.2.2 Hot Swap with Power Limit and dv/dt Inrush Control

For designs with large load currents and output capacitances, using a power-limit-based start-up can be impractical. Fundamentally, increasing load currents will reduce the sense resistor, which will increase the minimum Power Limit. Using a larger output capacitor will result in a longer start-up time and require a longer timer. Thus, a longer timer and a larger power limit setting are required, which places more stress on the MOSFET during a hot-short or a start into short. Eventually, there will be no FETs that can support such a requirement. An alternative is to limit the inrush current with a dv/dt control circuit shown in Figure 6. $C_{dv/dt}$ limits the slew rate of the gate and the output voltage, which in turn limits the inrush current.

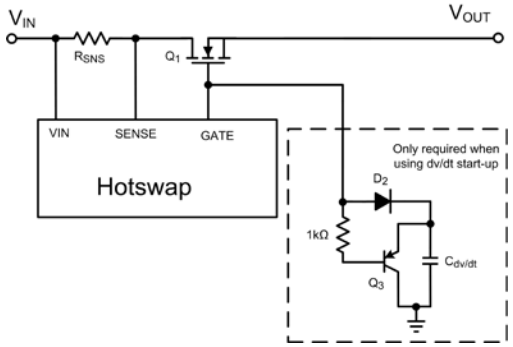

Figure 6. Circuit for Output dv/dt Control

Figure 7 shows a typical start-up waveform. Note that the inrush current is constant and the MOSFET power decreases as the V_{OUT} goes up and V_{DS} decreases. The start into short and hot-short will have similar waveforms as the power-limit-only circuit.

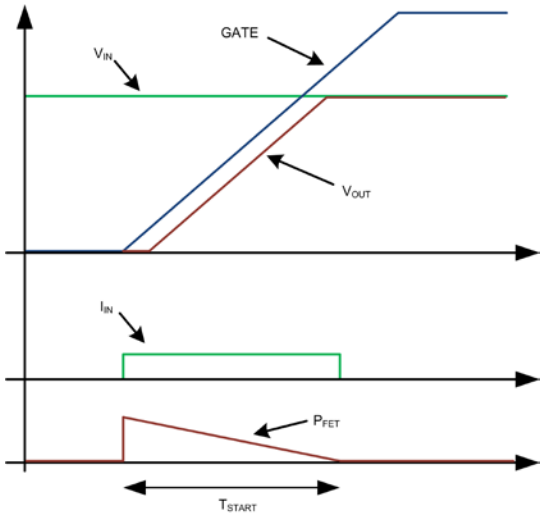

Figure 7. Start Up With Output dv/dt Control

When using a dv/dt control circuit along with power limit, the designer can do the following:

- Reduce the inrush current as necessary to ensure that the MOSFET can survive start-up.
- Reduce the timer as necessary to ensure that the MOSFET can survive start into short and hot-short.

2.3 Understanding MOSFET's Stress Limitations

To design a robust Hot Swap, it is critical to ensure that the MOSFET is safely operated under all conditions. This section describes the techniques for checking whether a given MOSFET will survive various test conditions.

2.3.1 MOSFET SOA Curve and Thermal Model

Figure 8 shows a typical safe operating area (SOA) plot for the PSMN4R8-100BSE FET. For each time duration, there is an IV curve that corresponds to the current and voltage that the device can withstand for that given time. When looking at the 10 ms curve, the MOSFET can handle 80 A at 10 V (800 W) or 4 A at 70 V (280 W). This effect is often observed in MOSFETs due to current crowding and other secondary effects and is worse for high voltage MOSFETs. To ensure a robust design, the power handling of a MOSFET should be based on the maximum V_{DS} that can be applied (typically V_{IN}). It is also important to note that this data is based on T_{MB} = 25°C, which is also referred to as the case temperature (T_C).

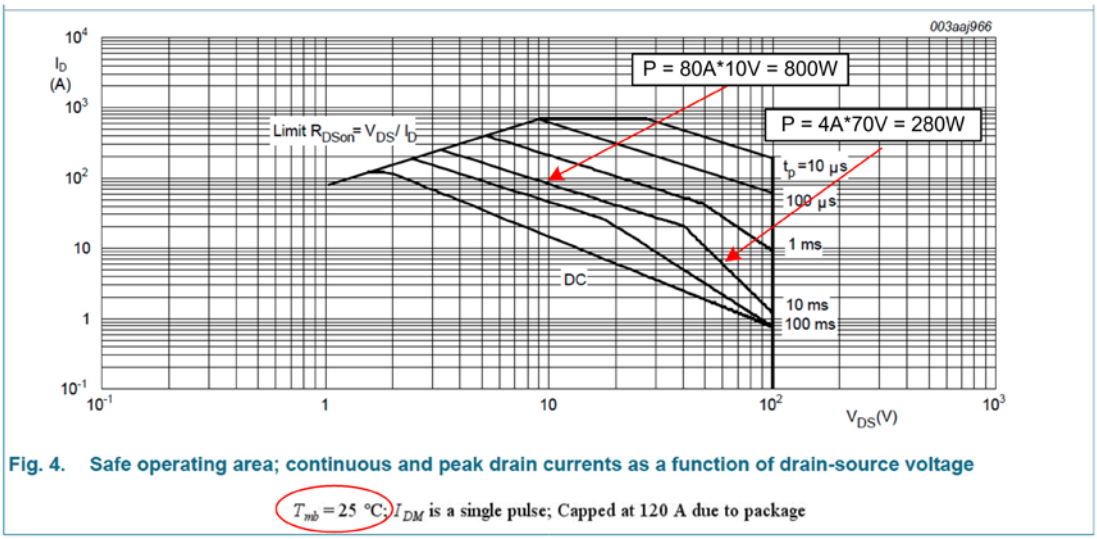

Figure 8. SOA Curve of PSMN4R8-100BSE

For the sake of Hot Swap design, the simplified MOSFET thermal model (Figure 9) is sufficient. T_J represents the junction temperature, T_C is the case temperature, T_A is the ambient temperature, C_J is the thermal capacitance of the junction, C_C is the thermal capacitance of the case, and P_{FET} is the power generated on the die. When the load current is constant and the FET is fully enhanced, P_{FET} is constant and T_J and T_C are purely a function of $R_{\theta CA}$ and $R_{\theta JC}$. Note that in a real test case, T_C may be much hotter than 25°C and the SOA must be derated.

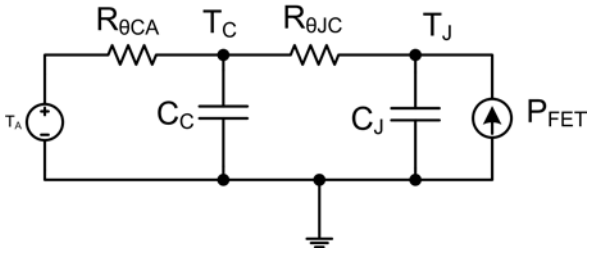

Figure 9. Simplified MOSFET Thermal Model

Often $R_{\theta CA}$ and $R_{\theta JC}$ are lumped together and called $R_{\theta JA}$ which is the junction to ambient thermal resistance. Typically, $R_{\theta CA}$ is a function of the layout and $R_{\theta JC}$ is a function of the package. In addition, $R_{\theta JC}$ is typically much lower than $R_{\theta CA}$ for MOSFETs with a thermal pad, and hence $R_{\theta CA}$ and $R_{\theta JC}$ are very similar and get used interchangeably. In addition, the C_C is quite large and thus T_C can be assumed to be constant during transient thermal events such as a hot short. To properly estimate the FETs stress handling capability, first the steady state case temperature should be computed using Equation 4. Note that R_{DSON} is a function of the junction temperature and Equation 4 may need to be solved iteratively with the R_{DSON} and T_C being updated in each iteration.

$$T_C = T_A + R_{\theta CA} \times I_{LOAD,MAX}^2 \times R_{DSON}(T_J) \quad (4)$$

Once T_C is known, the SOA can be derated accordingly using Equation 5. Note that this assumes that the T_C stays constant during the thermal transient.

$$SOA(T_C) = SOA(25°C) \times \frac{T_{J,ABSMAX} - T_C}{T_{J,ABSMAX} - 25°C} \quad (5)$$

2.3.2 Checking SOA for Intermediate Time Intervals

In addition to accounting for T_C dependence, the designer should consider the dependence of power handling vs time. In many cases, the FET will be "stressed" for an arbitrary time like 5 ms, but SOA data would only be available for 1 ms and 10 ms time intervals. In that case, proper extrapolation is necessary. Table 1 shows the stress handling capability of the PSMN4R8-100BSE vs time. SOA vs Time for V_{DS} = 60 V (PSMN4R8-100BSE)

Table 1. Stress Handling vs Time for PSMN4R8-100BSE (V_{DS} = 60 V)[4]

Time (ms)	SOA (W)	Energy (J)
100	120	12
10	360	3.6
1	1800	1.8
0.1	6000	0.6

Figure 10 plots the data in Table 1. Note that the points tend to follow a line on the log – log plot, which implies that the power function is the best way to estimate the SOA.

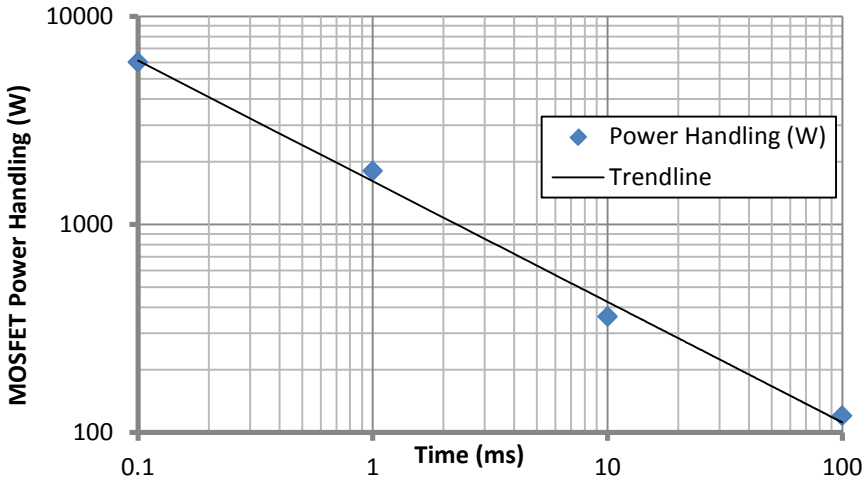

Figure 10. SOA vs Time for V_{DS} = 60 V (PSMN4R8-100BSE)[4]

The power function follows the format shown in Equation 6. The *a* and *m* coefficients can be computed by extrapolation if two data points are available. This principal is used in the Excel design calculators and in the following design examples.

$$SOA(t) = a \times t^m$$
$$m = \frac{ln(SOA(t_1)/SOA(t_2))}{ln(t_1/t_2)}; \quad a = \frac{SOA(t_1)}{t_1^m} \tag{6}$$

2.3.3 Checking SOA for Non-Square Power Pulses

When dv/dt based start-up is used or there is a load present at start-up, the transient FET stress may not be a square pulse. In that case, it needs to be converted to a square pulse as shown in Figure 11 so that it can be compared on the SOA curve.

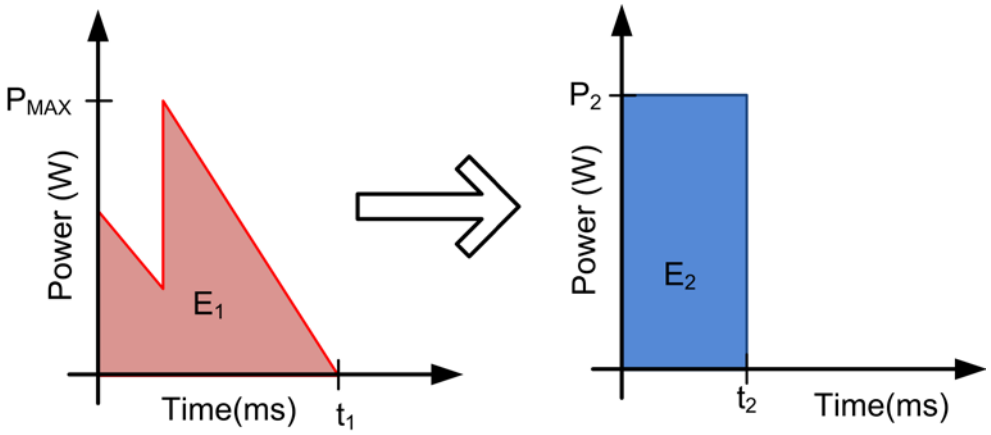

Figure 11. Approximating FET stress for Non-square pulses

To be conservative, the “equivalent square pulse” should be computed as follows:

$$E_2 = E_1 = \int_0^{t_1} P(t)dt \; ; \; P_2 = P_{MAX} \qquad (7)$$
$$t_2 = E_2/P_2$$

As can be seen from Table 1, the FET can handle more energy if it is spread over a longer time. Thus this approach is conservative, because the energy is equal but it is applied over a shorter period.

2.4 Considerations for Parallel MOSFETs

When using parallel MOSFETs, the designer must consider how well they current share. For Hot Swap design, TI recommends using these assumptions:

- When the FETs are fully enhanced, (V_{GS} > 10V) they will share the current evenly. Thus when computing the steady state case temperature, one can assume that each FET’s current equals the load current / # of MOSFETs.
- During start-up, hot-short, and start into short the MOSFETs are in saturation region (V_{GS} close to V_T and large V_{DS}) and a single MOSFET will take all of the current.

The first assumption is based on two facts. First, the R_{DSON} of MOSFET’s will usually not vary more than ±25%. Second, R_{DSON} has a positive temperature coefficient. Thus if one of the MOSFETs takes more than half the current, it will heat up and its R_{DSON} will increase, which will in turn, balance out how much current it draws.

Next consider the FET operation in saturation. The current is a very strong function of V_{GST}, which equals $V_{GS} – V_T$. Note that the V_T will often vary ±1 V. Thus, even if two FETs have the same V_{GS}, their V_{GST} can be quite different, resulting in a big variation in the current being drawn. To make things worse, the MOSFETs will draw more current at high temperature when operated at low V_{GS} as shown in Figure 12. This results in a positive feedback, where a MOSFET that draws more current will get hotter and then draw even more current.

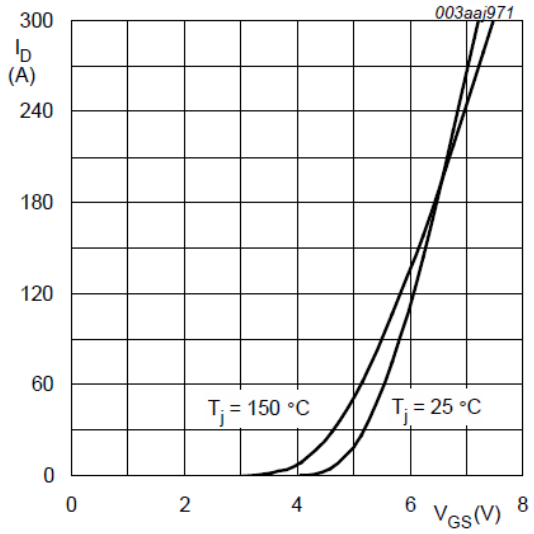

Figure 12. Transfer Characteristics (PSMN4R8-100BSE)[4]

3 Design Examples Using the LM5066I

This section provides a 48 V, 10 A and a 48 V, 20 A design example for the LM5066I. In both examples, the schematic below applies. The analysis shows that the dv/dt circuit is required for the 20-A design, but not necessary for the 10-A design.

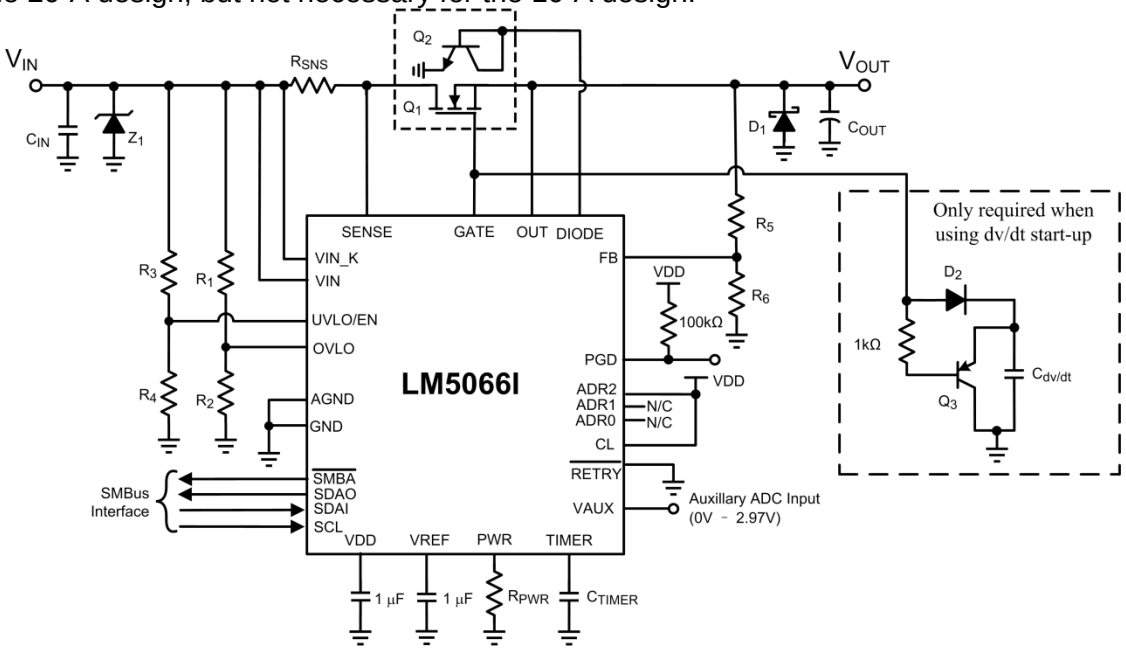

Figure 13. LM5066I Application Schematic

3.1 48-V, 10-A PMBus Hot Swap Design

3.1.1 Design Requirements

Table 2 summarizes the design parameters that must be known before designing a Hot Swap circuit.

Table 2. Design Requirements for 10-A Hot Swap

Design Parameter	Example Value
Input voltage range	40 V – 60 V
Maximum load current	10 A
Maximum Output Capacitance of the Hot Swap	220 µF
Maximum Ambient Temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

When charging the output capacitor through the Hot Swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load current will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET.

3.1.2 Design Procedure

3.1.2.1 Select R_{SNS} and CL setting

LM5066I can be used with a V_{CL} of 26 mV or 50 mV. In general, using the 26-mV threshold will result in a lower R_{SNS} and lower I^2R losses. This option is selected for this design by connecting the CL pin directly to V_{DD}. TI recommends targeting a current limit that is at least 10% above the maximum load current to account for the tolerance of the LM5066I current limit. Targeting a current limit of 11 A, the sense resistor can be computed as follows:

$$R_{SNS,CLC} = \frac{I_{LIM}}{V_{CL}} = \frac{26mV}{11A} = 2.36m\Omega \quad (8)$$

Note that for many applications, a precise current limit may not be required. In that case, it is simpler to pick the next smaller available sense resistor. For this application, a 2-mΩ resistor can be used for a 13-A current limit.

3.1.2.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 48-V systems, a 100-V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of ±20 V is required, because the LM5066I can pull up the gate as high as 16 V above source.

For this design the PSMN4R8-100BSE was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (9)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most D2PACK MOSFETS will be very close to the case temperature. A few iterations of the previous equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the PSMN4R8-100BSE datasheet, its R_{DSON} doubles at 110°C. Equation 10 uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

$$T_{C,MAX} = 85°C + 30°\frac{C}{W} \times (10A)^2 \times (2 \times 4.8m\Omega) = 114°C \quad (10)$$

3.1.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM5066I is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very low value. V_{SNS} can be computed as shown in Equation 11:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (11)$$

To avoid significant degradation of the power limiting a V_{SNS} of less than 4 mV is not recommended. Based on this requirement the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{4mV \times 60V}{2m\Omega} = 120W \quad (12)$$

In most applications the power limit can be set to $P_{LIM,MIN}$ using Equation 13. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{120 \times 0.002 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (13)$$

The closest available resistor should be selected. In this case a 28.2-kΩ resistor was chosen.

3.1.2.4 Set Fault Timer

The fault timer runs when the Hot Swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit ($I_{LIM} \times V_{DS} < P_{LIM}$) the maximum start time can be computed with Equation 14:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM}} \quad (14)$$

For most designs (including this example) $I_{LIM} \times V_{DS} > P_{LIM}$ so the Hot Swap will start in power limit and transition into current limit. In that case the maximum start time can be computed as follows:

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right] = \frac{220\mu F}{2} \times \left[\frac{(60V)^2}{120W} + \frac{120W}{(13A)^2}\right] = 3.38ms \quad (15)$$

Note that the previous start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time (t_{flt}) to be 1.5 × $t_{start,max}$ or 5.1 ms. This will account for the variation in power limit, timer current, and timer capacitance. Thus C_{TIMER} can be computed as follows:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{v_{timer}} = \frac{5.1ms \times 75\mu A}{3.9V} = 98.07\ nF \tag{16}$$

The next largest available C_{TIMER} is chosen as 100 nF. Once the C_{TIMER} is chosen, the actual programmed fault time can be computed as follows:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{100nF \times 3.9V}{75\mu A} = 5.2\ ms \tag{17}$$

3.1.2.5 Check MOSFET SOA

Once the power limit and fault timer are chosen, it is critical to check that the FET will stay within its SOA during all test conditions. During a “Hot-Short” the circuit breaker will trip and the LM5066I will re-start into power limit until the timer runs out. In the worst case, the MOSFET’s V_{DS} will equal $V_{IN,MAX}$, I_{DS} will equal P_{LIM} / $V_{IN,MAX}$ and the stress event will last for t_{flt}. For this design example the MOSFET will have 60 V, 2 A across it for 5.2 ms.

Based on the SOA of the PSMN4R8-100BSE, it can handle 60 V, 30 A for 1 ms and it can handle 60 V, 6 A for 10 ms. The SOA for 5.2 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 18:

$$\begin{gathered} I_{SOA}(t) = a \times t^m \\ m = \frac{\ln(I_{SOA}(t_1)/I_{SOA}(t_2)}{\ln(t_1/t_2)} = \frac{\ln(\frac{30A}{6A})}{\ln(\frac{1ms}{10ms})} = -0.7 \\ a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{30\text{A}}{(1\text{ms})^{-0.7}} = 30A \times (ms)^{0.7} \\ I_{SOA}(5.2ms) = 30A \times (ms)^{0.7} \times (5.2ms)^{-0.7} = 9.46A \end{gathered} \tag{18}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 19:

$$I_{SOA}(5.2ms, T_{C,MAX}) = I_{SOA}(5.2ms, 25\text{°C}) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25\text{°C}} = 9.46A \times \frac{175\text{°C} - 114\text{°C}}{175\text{°C} - 25\text{°C}} = 3.85A \tag{19}$$

Based on this calculation, the MOSFET can handle 3.85 A, 60 V for 5.2 ms at elevated case temperature, but is only required to handle 2 A during a hot-short. Thus there is good margin and this will be a robust design. In general, it is recommended that the MOSFET can handle 1.5x more than what is required during a hot-short. This provides margin to cover the variance of the power limit and fault time.

3.2 48-V, 20-A PMBus Hot Swap Design

3.2.1 Design Requirements

Table 3. Design Requirements for 20-A Hot Swap

Design Parameter	Example Value
Input voltage range	40 V – 60 V
Maximum load current	20 A
Maximum Output Capacitance of the Hot Swap	440 µF
Maximum Ambient Temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	30°C/W
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG asserted?	Yes
Can a hot board be plugged back in?	Yes

3.2.2 Detailed Design Procedure

3.2.2.1 Selecting the Sense Resistor and CL Setting

LM5066I can be used with a V_{CL} of 26 mV or 50 mV. In general using the 26-mV threshold will result in a lower R_{SNS} and lower I^2R losses. This option is selected for this design by connecting the CL pin directly to V_{DD}. It is recommended to target a currently limit that is at least 10% above the maximum load current to account for the tolerance of the LM5066I current limit. Targeting a current limit of 22 A, the sense resistor can be computed as follows:

$$R_{SNS,CLC} = \frac{I_{LIM}}{V_{CL}} = \frac{26mV}{22A} = 1.18m\Omega \quad (20)$$

For this application, a 1-mΩ resistor can be used for a 26-A current limit.

3.2.2.2 Selecting the Hot Swap FET(s)

For this design the PSMN4R8-100BSE was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times R_{DSON}(T_J) \quad (21)$$

Note that the R_{DSON} is a strong function of junction temperature, which for most D2PACK MOSFETS will be very close to the case temperature. A few iterations of the previous equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the PSMN4R8-100BSE datasheet, its R_{DSON} doubles at 110°C. Equation 22 uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is already above the absolute maximum of the FET.

$$T_{C,MAX} = 85°C + 30°\frac{C}{W} \times (20A)^2 \times (2 \times 4.8m\Omega) = 200°C \quad (22)$$

This suggests that 2 FETs should be used for the design. During steady-state operation, the MOSFETs are fully enhanced and will share current evenly. Thus assuming that each FET carries half of the current, the $T_{C,MAX}$ can be computed with Equation 23. Now $T_{C,MAX}$ is 114°C, which is quite reasonable.

$$T_{C,MAX} = 85°C + 30° \frac{C}{W} \times \left(\frac{20A}{2}\right)^2 \times (2 \times 4.8m\Omega) = 114°C \quad (23)$$

3.2.2.3 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, when the LM5066I is set to a very low power limit setting, it has to regulate the FET current and hence the voltage across the sense resistor (V_{SNS}) to a very low value. V_{SNS} can be computed as in the following:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} \quad (24)$$

To avoid significant degradation of the power limiting, a V_{SNS} below 4 mV is not recommended. Based on this requirement, the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}} = \frac{4mV \times 60V}{1m\Omega} = 240W \quad (25)$$

In most applications, the power limit can be set to $P_{LIM,MIN}$ as shown in Equation 26. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{240 \times 0.001 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (26)$$

The closest available resistor should be selected. In this case a 28.2-kΩ resistor was chosen.

3.2.2.4 Set Fault Timer

The maximum start time can be computed to 3.37 ms as shown in Equation 27.

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM}^2}\right] = \frac{440\mu F}{2} \times \left[\frac{(60V)^2}{240W} + \frac{240W}{(26A)^2}\right] = 3.37ms \quad (27)$$

Note that the previous start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time (t_{flt}) to be 1.5 × $t_{start,max}$ or 5.1 ms. This will account for the variation in power limit, timer current, and timer capacitance. Thus C_{TIMER} can be computed as follows:

$$C_{TIMER} = \frac{t_{flt} \times i_{timer}}{v_{timer}} = \frac{5.1ms \times 75\mu A}{3.9V} = 98.07\ nF \quad (28)$$

The next largest available C_{TIMER} is chosen as 100 nF. Once the C_{TIMER} is chosen the actual programmed fault time can be computed as follows:

$$t_{flt} = \frac{C_{TIMER} \times v_{timer}}{i_{timer}} = \frac{100nF \times 3.9V}{75\mu A} = 5.2\ ms \tag{29}$$

3.2.2.5 Check MOSFET SOA

Once the power limit and fault timer are chosen, it is critical to check that the FET will stay within its SOA during all test conditions. During a “Hot-Short” the circuit breaker will trip and the LM5066I will re-start into power limit until the timer runs out. In the worst case the MOSFET’s V_{DS} will equal $V_{IN,MAX}$, I_{DS} will equal P_{LIM} / $V_{IN,MAX}$ and the stress event will last for t_{flt}. For this design example the MOSFET will have 60 V, 4A across it for 5.2 ms.

When the Hot Swap is in power limit and the FETs are operating in saturation region (V_{GS} close to threshold voltage) the designer cannot assume that the FETs will share. Even a small V_T mismatch will cause a large difference in the current carried by the 2 MOSFETs. Thus, the SOA checking should be done assuming that all of the current is flowing through a single FET.

Based on the SOA of the PSMN4R8-100BSE, it can handle 60 V, 30 A for 1 ms and it can handle 60 V, 6 A for 10 ms. The SOA for 5.2 ms can be extrapolated by approximating SOA vs time as a power function as shown in Equation 30:

$$I_{SOA}(t) = a \times t^m$$
$$m = \frac{\ln(I_{SOA}(t_1)/I_{SOA}(t_2)}{\ln(t_1/t_2)} = \frac{\ln(\frac{30A}{6A})}{\ln(\frac{1ms}{10ms})} = -0.7$$
$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{30\text{A}}{(1\text{ms})^{-0.7}} = 30A \times (ms)^{0.7}$$
$$I_{SOA}(5.2ms, 25°\text{C}) = 30A \times (ms)^{0.7} \times (5.2ms)^{-0.7} = 9.46A \tag{30}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much hotter during a hot-short. The SOA should be de-rated based on $T_{C,MAX}$ using Equation 31:

$$I_{SOA}(5.2ms, T_{C,MAX}) = I_{SOA}(5.2ms, 25°\text{C}) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°\text{C}} = 9.46A \times \frac{175°\text{C} - 114°\text{C}}{175°\text{C} - 25°\text{C}} = 3.85A \tag{31}$$

Based on this calculation, the MOSFET can handle 3.85 A, 60 V for 5.2 ms at elevated case temperature, but it is required to handle 4 A during a hot-short. In addition, there will be tolerance on the power limit and timer so using these settings would not produce a robust Hot Swap design.

3.2.2.6 Switching to dv/dt based Start-up

Since the design requirements were not met with a power limit only approach, output dv/dt control should also be used, the benefits of which were described in Section 2.2.2.

3.2.2.7 Choosing the V_{OUT} Slew Rate

The inrush current should be kept low enough to keep the MOSFET within its SOA during start-up. Note that the total energy dissipated in the MOSFET during start-up is constant regardless of the inrush time. Thus, stretching it out over a longer time will always reduce the stress on the MOSFET as long as the load is off during start-up.

When choosing a target slew rate, one should pick a reasonable number, check the SOA and reduce the slew rate if necessary. Using 4 V/ms as a starting point, the inrush current can be computed as follows:

$$I_{INR} = C_{OUT} \times \frac{dV_{OUT}}{dt} = 440\mu F \times \frac{4V}{ms} = 1.76A \tag{32}$$

Assuming a maximum input voltage of 60 V, it will take 15 ms to start-up. Note that the power dissipation of the FET will start at $V_{IN,MAX} \times I_{INR}$ and reduce to zero as the V_{DS} of the MOSFET is reduced. Note that the SOA curves assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where $P_{FET} = V_{IN,MAX} \times I_{INR}$ for t = $t_{start\text{-}up}$ /2. In this instance, the SOA can be checked by looking at a 60 V, 1.76 A, 7.5 ms pulse. Using the same technique as section 3.2.2.5, the MOSFET SOA can be estimated as follows:

$$I_{SOA}(7.5ms) = 30A \times (ms)^{0.7} \times (7.5ms)^{-0.7} = 7.32A \tag{33}$$

This value has to also be derated for temperature. For this calculation, it is assumed that T_C can equal $T_{C,MAX}$ when the board is plugged in. This would only occur if a hot board is unplugged and then plugged back in before it cools off. This is worst case and for many applications, the $T_{A,MAX}$ can be used for this derating.

$$I_{SOA}(7.5ms, T_{C,MAX}) = I_{SOA}(7.5ms, 25°C) \times \frac{T_{J,ABSMAX} - T_{C,MAX}}{T_{J,ABSMAX} - 25°C} = 7.32A \times \frac{175°C - 114°C}{175°C - 25°C} = 2.98A \tag{34}$$

This calculation shows that the MOSFET will stay well-within its SOA during a start-up if the slew rate is 4 V/ms. Note that if the load is off during start-up, the total energy dissipated in the FET is constant regardless of the slew rate. Thus a lower slew rate will always place less stress on the FET. To ensure that the slew rate is at most 4 V/ms, the $C_{dv/dt}$ should be chosen as follows:

$$c_{dv/dt} = \frac{I_{SOURCE,MAX}}{4\,V/ms} = \frac{40\,\mu A}{4\,V/ms} = 10nF \tag{35}$$

Next, the typical slew rate and start time can be computed to be 2 V/ms as shown in Equation 36, making the typical start time 30 ms.

$$V_{OUT,dv/dt} = \frac{I_{SOURCE}}{c_{dv/dt}} = \frac{20\,\mu A}{10\,nF} = 2\,V/ms \tag{36}$$

3.2.2.8 Select Power Limit and Fault Timer

When picking the power limit it needs to meet 2 requirements:

- Power limit is large enough to avoid operating with V_{SNS} < 4 mV
- Power limit is large enough to ensure that the timer does not run during start up. Picking a power limit such that it is 2x of $I_{INR,MAX} \times V_{IN,MAX}$ is good practice.

Thus, the minimum allowed power limit can be computed as follows:

$$P_{LIM,MIN} = \max\left(\frac{V_{SNS,MIN} \times V_{IN,MAX}}{R_{SNS}}, 2 \times V_{IN,MAX} \times I_{INR,MAX}\right) = \max(240W, 211.2W) = 240W \quad (37)$$

Next, the power limit is set to $P_{LIM,MIN}$ using Equation 38. Here R_{SNS} and R_{PWR} are in ohms and P_{LIM} is in watts.

$$R_{PWR} = \frac{P_{LIM} \times R_{SNS} - 0.043}{7 \times 10^{-6}} = \frac{240 \times 0.001 - 0.043}{7 \times 10^{-6}} = 28143\Omega \quad (38)$$

The closest available resistor should be selected. In this case a 28.2-kΩ resistor was chosen.

Next a fault timer value should be selected. In general, the timer value should be decreased until there is enough margin between available SOA and the power pulse the FET experiences during a hot-short. For this design a 100 nF C_{TIMER} was chosen corresponding to a 520 µs. The available SOA is extrapolated using the method previously described.

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln(I_{SOA}(t_1)/I_{SOA}(t_2)}{\ln(t_1/t_2)} = \frac{\ln(\frac{100A}{30A})}{\ln(\frac{0.1ms}{1ms})} = -0.52$$

$$a = \frac{I_{SOA}(t_2)}{t_2^m} = \frac{30\text{A}}{(1\text{ms})^{-0.52}} = 30A \times (ms)^{0.52}$$

$$I_{SOA}(0.52ms, 25°\text{C}) = 30A \times (ms)^{0.52} \times (0.52ms)^{-0.52} = 42.3A \quad (39)$$

Next the available SOA is derated for temperature:

$$I_{SOA}(0.52ms, T_{C,MAX}) = 42.3A \times \frac{175°\text{C} - 114°\text{C}}{175°\text{C} - 25°\text{C}} = 17.17A \quad (40)$$

Note that only 4 A was required, while the FET can support 17.17 A. This confirms that the design will be robust and have plenty of margin.

4 Conclusion

This application note presented a framework for ensuring that a MOSFET is safely operated in a Hot-Swap circuit.

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