D-CAP+™ Control for Multiphase, Step-Down Voltage Regulators for Powering Microprocessors

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ABSTRACT

This application report introduces the basics of 3 generations of D-CAP+™ multiphase step-down controllers. For the multiphase voltage regulators (VRs) powering microprocessors, fast load-transient performance is one of the most important specifications to ensure the performance of the microprocessors. This application report explains the benefits of using D-CAP+ control to achieve fast load-transient performance, while keeping good dynamic current sharing. The mathematical small-signal model of the 2nd-generation D-CAP+ control is also presented in this application report with considerations of adaptive voltage positioning (AVP). Two design examples are given to validate the model based on the designs with TPS53661 and TPS53667.

Contents

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1   Introduction

With growing demands on the mobile devices, the related infrastructures, such as servers, storage, or telecommunication equipment, are required to be upgraded with higher computing power, higher efficiency, and higher power densities. The microprocessors inside the equipment determine the computing power, and the voltage regulators (VRs) for powering these microprocessors are the key to improve its dynamic peformance, reliability, and efficiency with less costs and higher power densities. In order to fulfill the high-power requirements, multiphase VRs are required. Figure 1 shows the multiphase VRs used for servers.
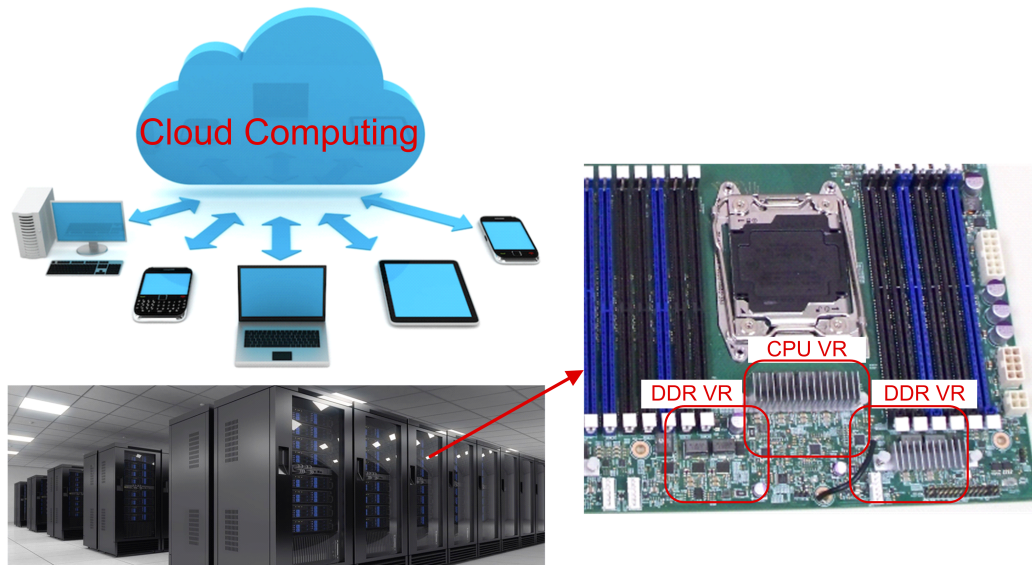
Figure 1. Multiphase Voltage Regulators for Servers

1.1 History of TI D-CAP+™ Step-Down Multiphase Controllers

TI offers three generations of D-CAP+ ™ step-down multiphase controllers for powering Intel processors and ASICs. Table 1 lists the comparisons of three generations.

Table 1. Comparisons of 3 Generations of TI D-CAP+ Multiphase Controllers.

Functionality	1st Generation	2nd Generation	3rd Generation
Output Channels	Single output	Single output	Dual outputs
Maximum Phase Numbers Per Channel	Up to 3 phases	Up to 6 phases	Up to 6 phases
Current Sensing Methods	Inductor DCR sensing	Inductor DCR sensing or smart power stage current sensing	Smart power stage current sensing
Mode Configurations	Pinstraps	Pinstraps or Non-Volatile Memory (NVM)	Non-Volatile Memory (NVM)
Temperature Sensing	NTC	NTC or smart power stage	smart power stage
Loop Compensations	External components	External components	Internal circuits
Communication Interfaces	Intel SVID™	Intel SVID™ and PMBus	Intel SVID™ and PMBus
Loadline Settings	External resistor without on-the-fly programmability	External resistor with on-the-fly programmability	Internal circuit with on-the-fly programmability
Dynamic Phase Adding/Shedding	Not supported	Support 1-2-4-6 phases	Support 1-2-3-4-5-6 phases
TI Product Family	TPS51623, TPS51631, TPS53625, TPS53626	TPS53640, TPS53640A, TPS53631, TPS53641, TPS53661, TPS53647, TPS53667	TPS53679, TPS53678, TPS53659, TPS53659A, TPS53658, TPS53622, TPS53622A, TPS53681

2 Basics of D-CAP+™ Control for Multiphase Converters

2.1 Block Diagram

Figure 2 shows the 2nd-generation D-CAP+™ control block diagram being used in TPS53661 and TPS53667. The individual phase currents are sensed from TI smart power stages as V_{IX} and are averaged as V_{ISUM_AC} as follows, which will be sent to the PWM modulator.

$$V_{ISUM\_AC} = \sum_{x=1}^{N} \frac{i_{Lx} \times R_{CS}}{6} + V_{REF}$$

where

- N is the total phase number
- i_{Lx} is the per-phase inductor current
- R_{cs} is the equivalent current sensing resistance from TI smart power stage, which is 5 mΩ (typ)
- V_{REF} is the internal reference voltage, which is 1.7V (typ)   (1)

In the meanwhile, the averaged phase currents can also be used to generate a droop voltage, V_{ISUM}, as shown in Equation 2.

$$V_{ISUM} = (V_{ISUM\_AC} - V_{REF}) \times g_{M(ISUM)} \times R_{ISUM} + V_{REF}$$

where

- R_{ISUM} is the external resistor put between the ISUM pin and the VREF pin
- $g_{M(ISUM)}$ is the internal gain of the transconductance amplifier, which is 0.5mS (typ)   (2)

The compensation voltage, V_{COMP}, is generated to regulate the feedback voltage with droop, V_{FBDRP}, at the DAC voltage, V_{DAC}.

$$V_{COMP} = (V_{DAC} - V_{FBDRP}) \times g_{M(COMP)} \times Z_{COMP} + V_{REF}$$

where

- Z_{COMP} is the equivalent impedance to be put from the COMP pin to the VREF pin as the compensator
- $g_{M(COMP)}$ is the gain of the transconductance amplifier for the compensator, which is 1 mS (typ)   (3)
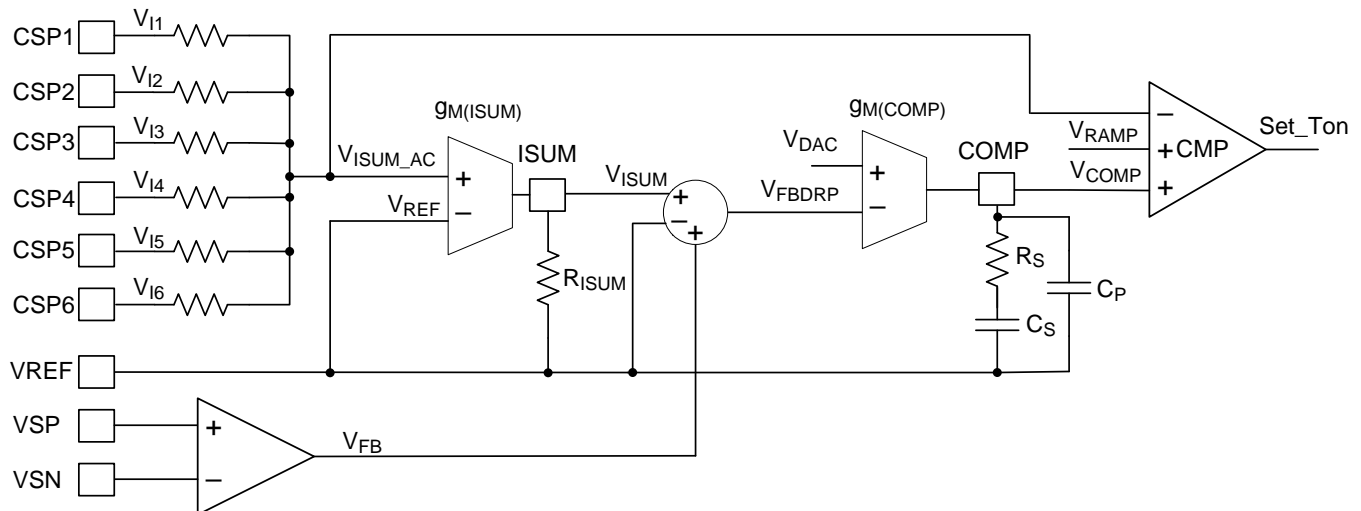
$$V_{FBDRP} = (V_{ISUM} - V_{REF}) + V_{FB}$$

(4)

Figure 2. 2nd-Generation D-CAP+™ Control Block Diagram

2.2   *Phase Interleaving and Ramp Compensation*

As shown in Figure 2, in addition to the compensation voltage, V_{COMP}, and the averaged current, V_{ISUM_AC}, there is also a ramp voltage, V_{RAMP}, to the PWM comparator. Figure 3 shows the operational waveforms of the D-CAP+ control at the steady-state conditions. Once the valley of the averaged current reaches the summation of the compensation voltage and the ramp voltage, a Set_Ton signal is triggered to generate the PWM signal, and distributed to different phases based on phase management, to achieve phase interleaving for reducing input and output voltage and current ripples.

However, the averaged current ripple amplitude would be attenuated due to the ripple cancellation effect with multiphase operations depending on different duty ratios and different phase numbers, as shown in Figure 4. Therefore, a ramp voltage is generated as shown in Figure 5 and Figure 6 to improve the signal-to-noise ratio during operations to improve the jitter performance. Figure 7 and Figure 8 show the comparison of the jitter performance with and without ramp compensation for a 6-phase operation from 12-V input voltage to 1.8-V output voltage. Figure 7 and Figure 8 clearly show that the ramp compensation could effectively improve the jitter performance, especially when operating in multiphase operations. It should also be noted that the more ramp voltage is injected to the PWM comparator, the slower loop response would be expected, so the ramp voltage needs to be adjusted based on the actual operating conditions.
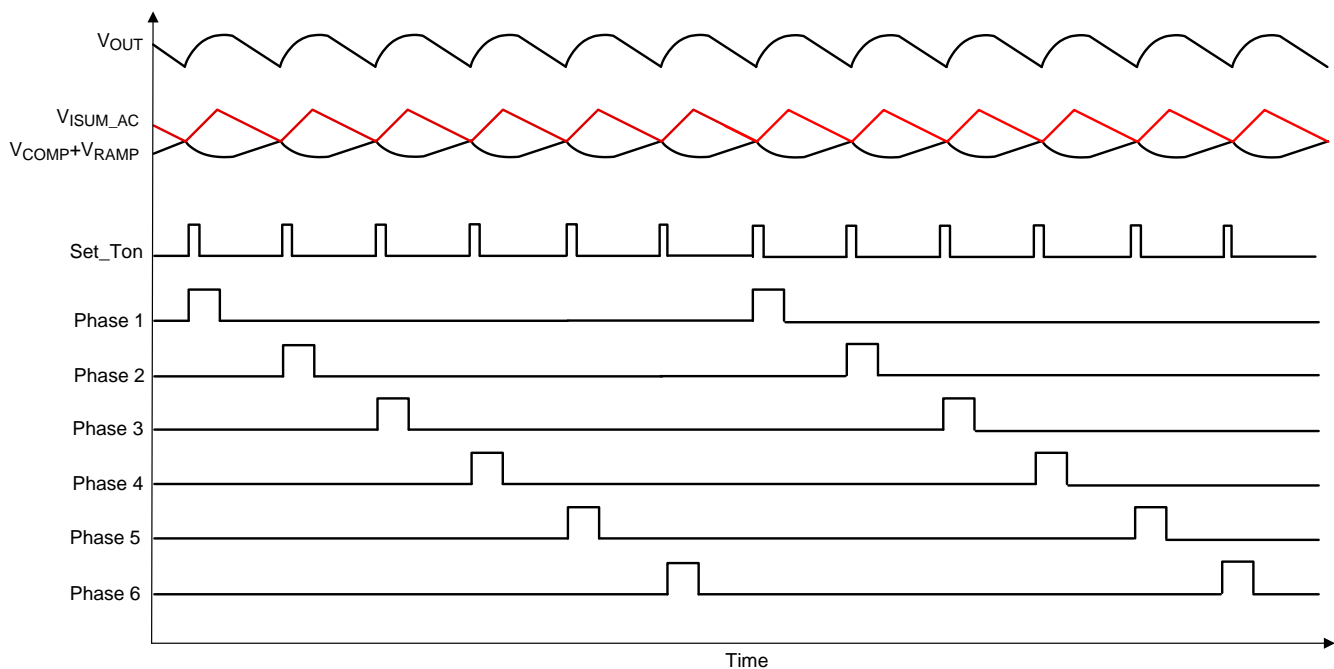

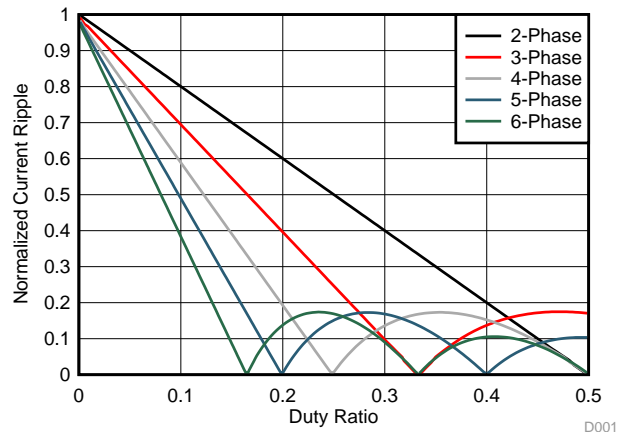**Figure 3. Operational Waveforms of D-CAP+™ Control**

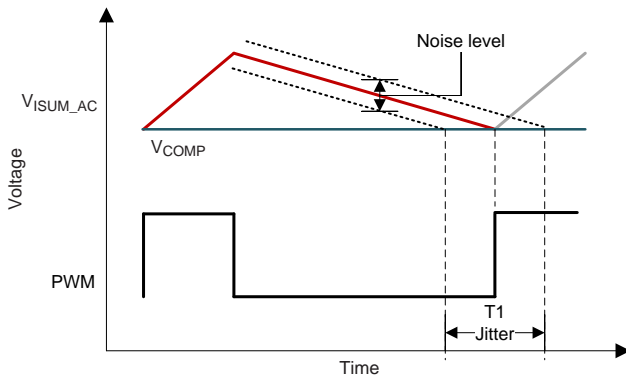**Figure 4. Ripple Cancellation Effects With Different Operating Duty Ratios and Phase Numbers**
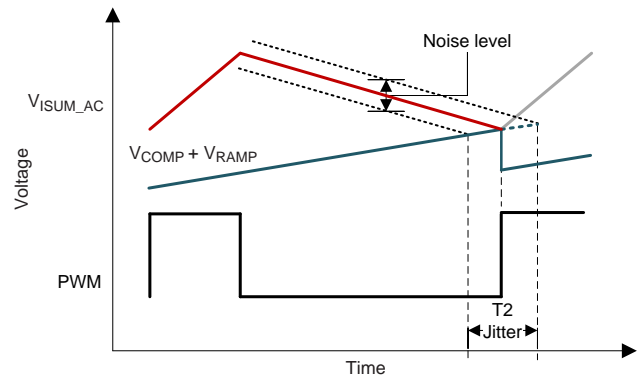

Figure 5. Operation Without Ramp Compensation

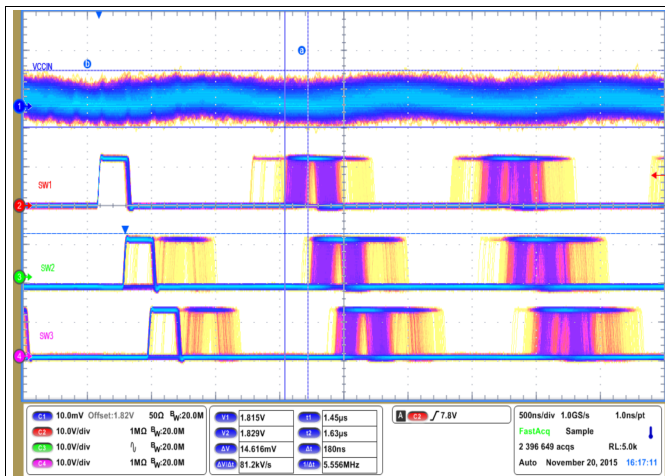**Figure 6. Operation With Ramp Compensation**

Figure 7. Jitter Performance With 6-Phase Operations at 12-V_{IN} to 1.8-V_{OUT} Without Ramp Compensation
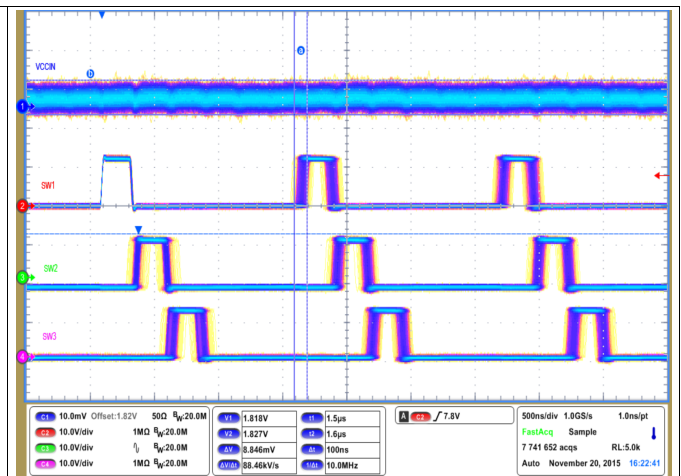

Figure 8. Jitter Performance With 6-Phase Operations at 12-V_{IN} to 1.8-V_{OUT} With Ramp Compensation

2.3 *Adaptive Voltage Positioning*

Due to the stringent load transient requirements for VRs powering the microprocessors, the concept of adaptive voltage positioning (AVP) has been proposed to reduce the output capacitance[1]. Figure 9 shows how to reduce the peak-to-peak voltage deviations by half during load transients with enabling AVP. To achieve the AVP design, the loadline is required to lower the output voltage with increasing load currents, as shown in Figure 10, and can be defined as shown in Equation 5.

$$V_{DAC} = V_{OUT} + I_{OUT} \times R_{LL} = V_{FBDRP}$$

where

- R_{LL} is the defined loadline. (5)

Derive the defined loadline for the 2nd-generation D-CAP+ control using Equation 1 through Equation 5, and adjust by changing the external R_{ISUM} resistor as shown in Equation 6.

$$R_{LL} = \frac{(V_{ISUM} - V_{REF})}{I_{OUT}} = \frac{R_{CS}}{6} \times g_{M(ISUM)} \times R_{ISUM}$$
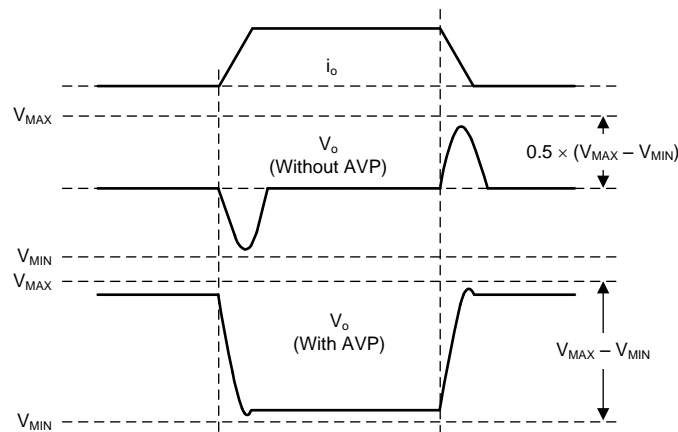
(6)

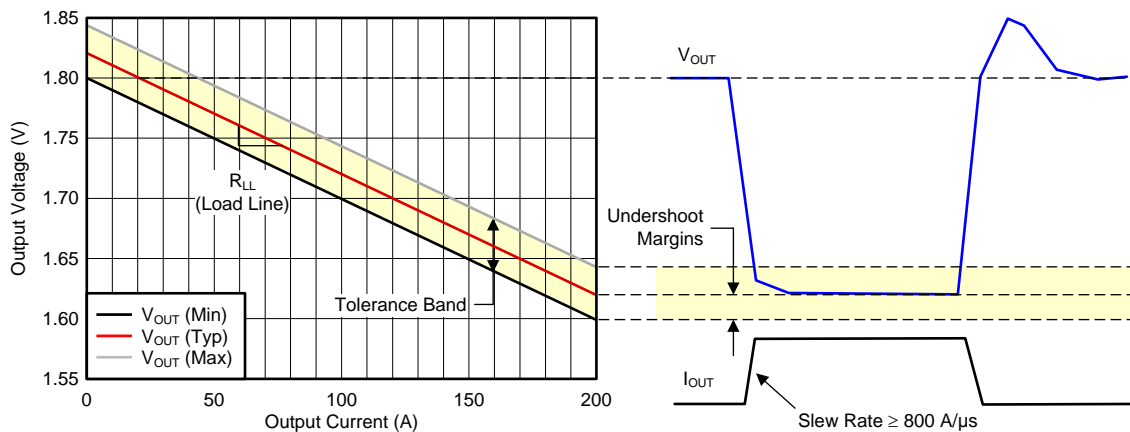**Figure 9. Waveforms of Adaptive Voltage Positioning (AVP). [1]**

**Figure 10. Waveforms of the Loadline and Droop Voltage**

2.4 *Fast Load Transient Response with Variable Switching Frequencies*

In the steady-state operations, D-CAP+ control can have a *pseudo* fixed-frequency operation for each phase by distributing PWM pulses. During load transients, D-CAP+ control can distribute PWM pulses faster to improve the load transient performance naturally. Figure 11 and Figure 12 show the operational waveforms during load transients. At load step-up transients, the Set_Ton signals can be generated faster to provide more energy to the load, to reduce the undershoot voltage. On the other hand, at load step-down transients, the switching clock can be held off to discharge the load faster to reduce the overshoot voltage.

Figure 11. Load Step-Up Transient Performance

Figure 12. Load Step-Down Transient Performance
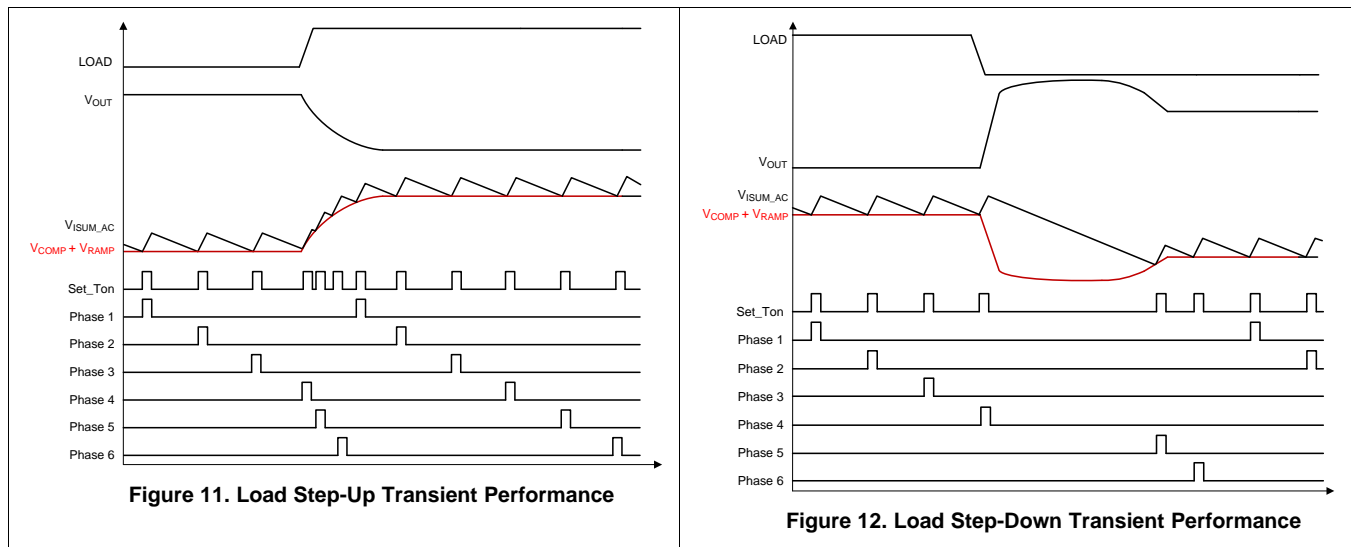
2.5 *Dynamic Current Sharing*

Current sharing performance is very important for the multiphase voltage regulator to balance thermal distributions among phases. Figure 13 shows the block diagram of dynamic current sharing implemented with the D-CAP+ control architecture. Only light filtering is added for each phase current, so the on-time for individual phases can be adjusted quickly to achieve superior dynamic current sharing performance even during load transients.
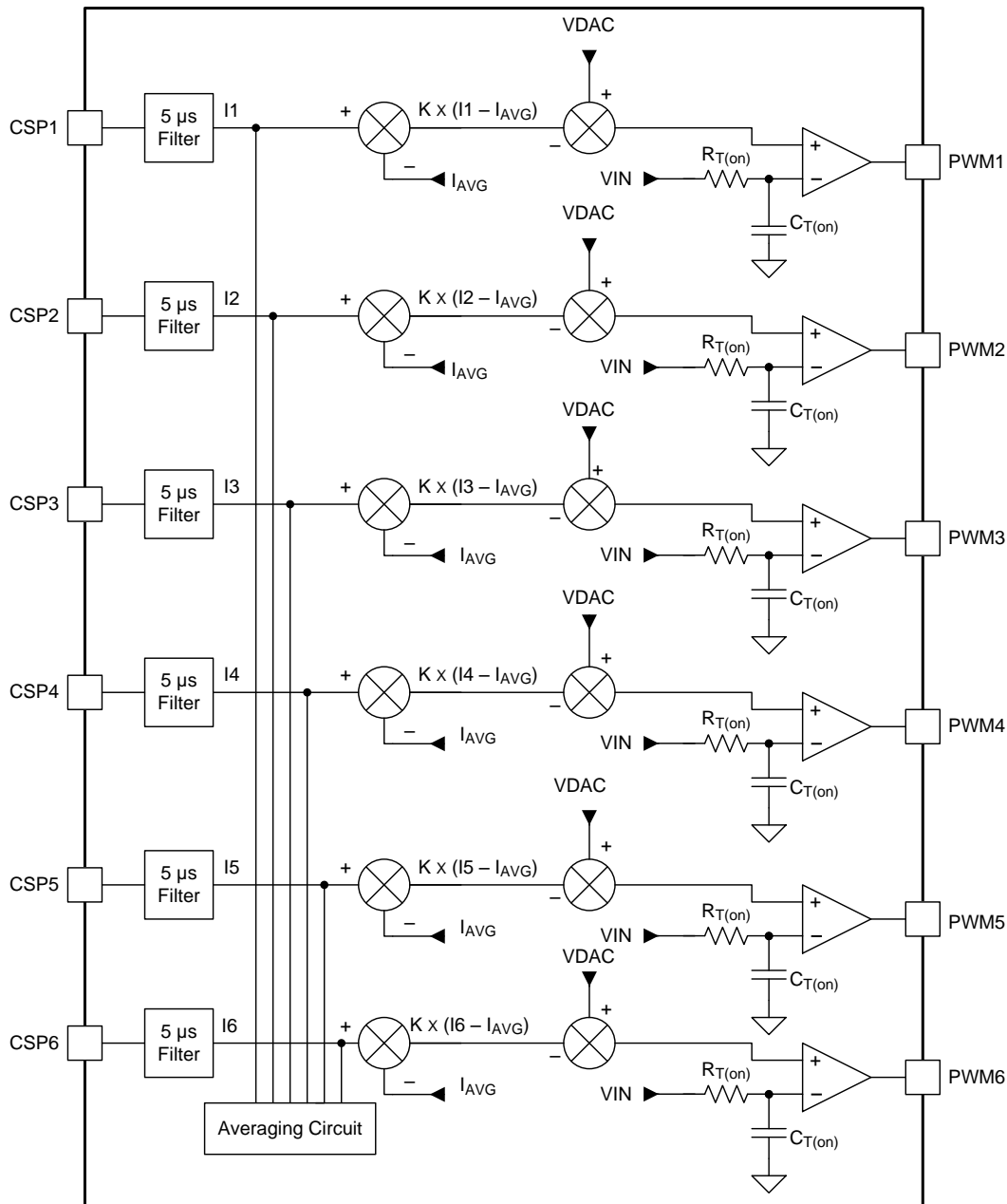
Figure 13. Current Sharing Block Diagram

Figure 14 and Figure 15 show the current sharing waveforms with different load frequencies. As seen in Figure 14 and Figure 15, the phase currents can be balanced well under both low and high rep-rate load transients. In addition, due to the nature of the variable switching frequency characteristics mentioned previously, there is no beat-frequency oscillation issue when the load frequency is close to the switching frequency, as shown in Figure 15.
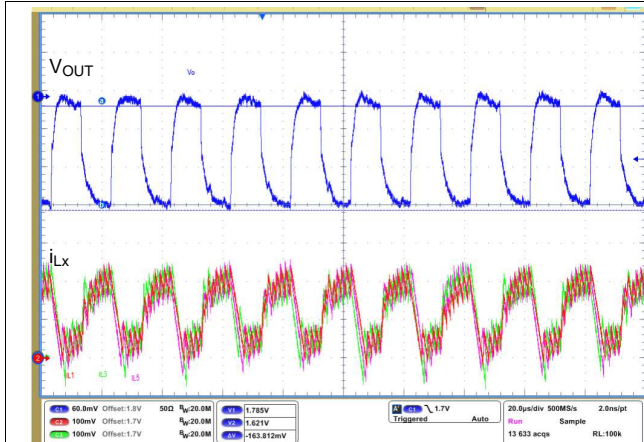

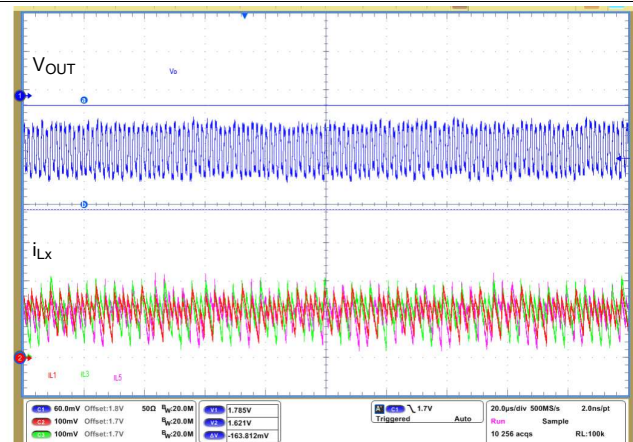**Figure 14. Dynamic Current Sharing Performance With 50-kHz Load Frequency**

Figure 15. Dynamic Current Sharing Performance With 600-kHz Load Frequency

3   Compensation Design for the 2nd-Generation D-CAP+ Control

3.1   *Mathematical Small-Signal Model Derivations*

To design the compensators, the loop gain transfer function is required. As shown in Figure 2, the D-CAP+ control architecture consists of two loops[2]. The inner loop is the fast current loop with ramp compensation, and the control-to-inductor current transfer function can be derived as follows in Equation 7.

$$G_{c2iL}(s) = \frac{i_{SUM\_AC}(s)}{v_{COMP}(s)} \cong \frac{N}{R_{CS}} \times \frac{1}{\left(1 + \frac{s}{Q_1 \times \omega_1} + \frac{s^2}{(\omega_1)^2}\right)} \times \frac{1 + \frac{T_{SW}}{2 \times N} \times s}{1 + \left(\frac{s_e}{s_f} + \frac{1}{2}\right) \times \frac{T_{SW}}{N} \times s}$$

where
- $Q_1 = 2 / \pi$ and $\omega_1 = N\pi / T_{ON}$
- T_{ON} is the on-time
- T_{SW} is the switching period
- s_e is the slope of the ramp voltage
- s_f is the down slope of the phase inductor current   (7)

Figure 16 shows the frequency response of the derived control-to-inductor current transfer function with different ramp slopes. As shown in Figure 16, increasing the ramp slopes causes phase drops at high-frequency ranges, compared to an ideal current mode control system. Therefore, the guideline for ramp voltage selection is to have minimum ramp slopes with acceptable jitter performance, to ensure the loop performance.
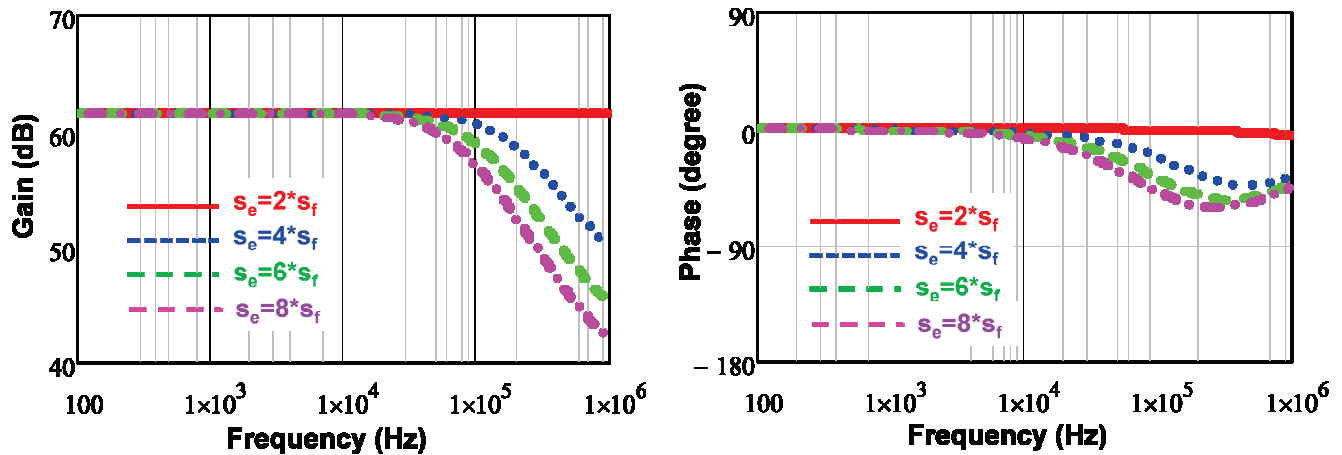
Figure 16. Frequency Response of Control-to-Inductor Current Transfer Function of the Inner Loop

The second loop contains both the current loop for droop design and the voltage loop. The loop gain transfer function can be derived as shown in Equation 8

$$G_{\text{LOOP}}(s) = H_{\text{COMP}}(s) \times G_{\text{c2iL2}}(s) \times Z_{\text{cap}}$$

where

- Z_{cap} is the equivalent impedance of the output capacitors, which consists of bulk capacitors, cavity capacitors, and the socket impedance for VRs, as shown in Figure 17.
- $H_{\text{COMP}}(s)$ is the transfer function of the compensator as follows. (8)

$$H_{\text{COMP}(s)} = g_{\text{M(COMP)}} \times Z_{\text{COMP}(s)}$$

(9)

$$G_{\text{c2iL2}}(s) = \frac{G_{\text{c2iL}}(s)}{1 + G_{\text{c2iL}}(s) \times R_{\text{LL}} \times H_{\text{COMP}}(s)}$$
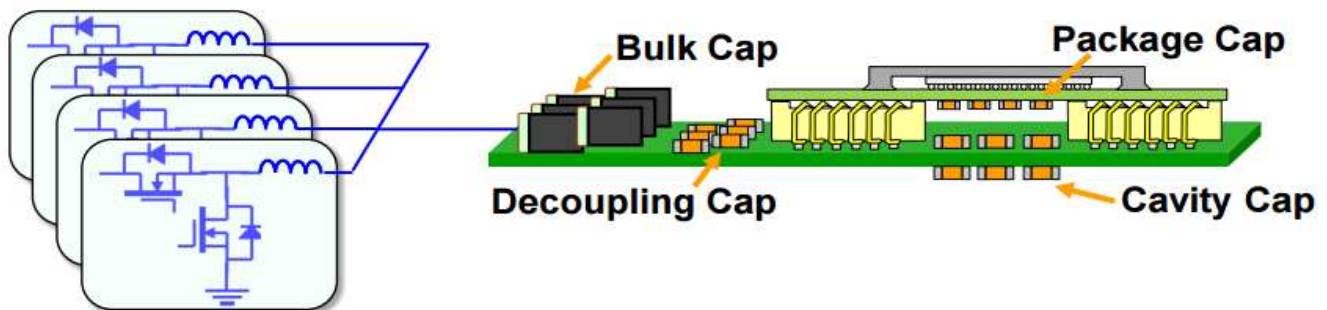
(10)

Figure 17. Output Capacitors in the Power Delivery Path for VRs

Figure 18 shows an example of a type II compensation network being put as Z_{COMP}, and its frequency response. The low-frequency pole is dominated by internal parasitics of the transconductance amplifier, such as C_{gm} and R_{gm}, and the zero is determined by the series resistor, R_{COMP}, and the series capacitor, C_S. The high-frequency pole for noise attenuation is dominated by R_{COMP} and the parallel capacitor, C_P.
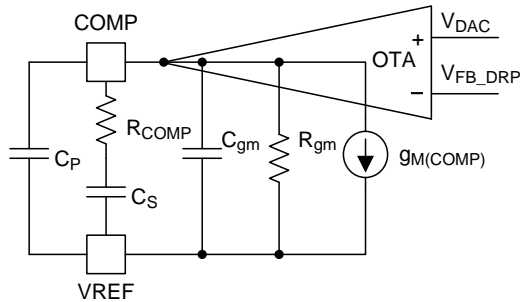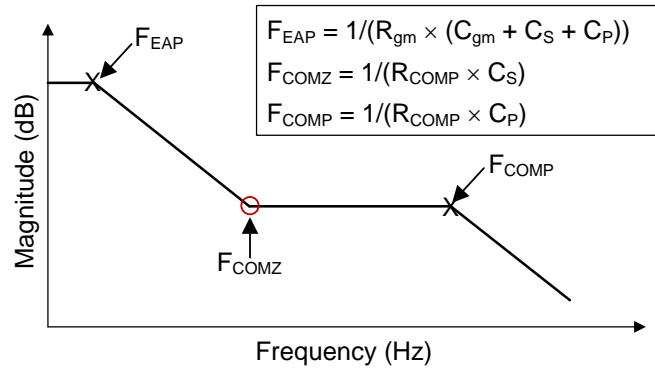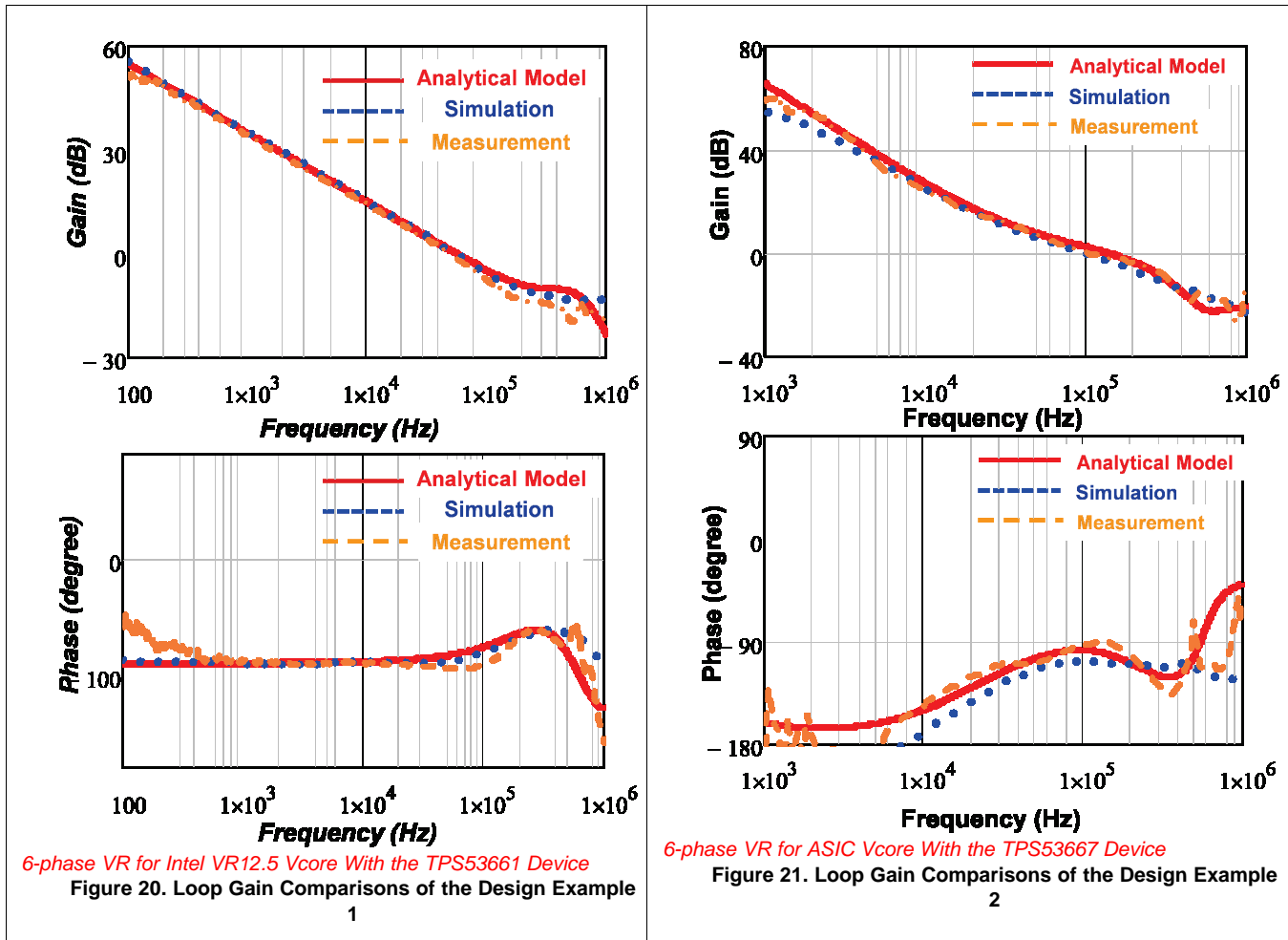
Figure 18. Type-II Compensation Circuit

Figure 19. Type-II Compensation Frequency Responses

$$F_{EAP} = 1/(R_{gm} \times (C_{gm} + C_S + C_P))$$
$$F_{COMZ} = 1/(R_{COMP} \times C_S)$$
$$F_{COMP} = 1/(R_{COMP} \times C_P)$$

3.2 Design Examples With the TPS53661 and TPS53667 Devices

To verify the loop gain model, two design examples are provided in this application note. The first design example uses the TPS53661 device to design a 6-phase VR to power the Intel VR12.5 Vcore rail. The second design example uses the TPS53667 device to design a 6-phase VR to power the ASIC Vcore rail. Table 2 lists the design parameters of both examples. Based on the loop gain model from Equation 8, Equation 9, and Equation 10 the frequency response of the loop gain transfer function can be calculated. Figure 20 and Figure 21 show the comparisons of the frequency responses with the presented analytical model, simulation data, and measurement data. As shown in Figure 20 and Figure 21, the analytical model presented in this application note can predict the loop gain performance for the design.

Table 2. Design Example Parameters

Parameters	Design Example 1: VR for Intel VR12.5 Vcore With the TPS53661	Design Example 2: VR for ASIC Vcore With the TPS53667
Input voltage	12 V	12 V
Output voltage	1.8 V	1.0 V
Phase numbers	6	6
Inductor	150 nH	150 nH
Output capacitors	4 × 470 µF / 3 mΩ 60 × 22 µF	4 × 470 µF / 4.5 mΩ 20 × 100 µF
Loadline	1.0 mΩ	0 mΩ
Switching frequency	650 kHz	500 kHz
Ramp voltages	260 mV	150 mV
Compensation	R_{COMP} = 6 kΩ C_S = 200 pF C_P = 10 pF	R_{COMP} = 8.06 kΩ C_S = 1000 pF C_P = 12 pF

6-phase VR for Intel VR12.5 Vcore With the TPS53661 Device

Figure 20. Loop Gain Comparisons of the Design Example 1

6-phase VR for ASIC Vcore With the TPS53667 Device

Figure 21. Loop Gain Comparisons of the Design Example 2

4   Summary

This application note summarized the features of the D-CAP+ control architecture used in multiphase VRs. The analysis of the control loop and its analytical model were also presented to help users design the compensator for different applications. Two design examples were presented to verify the effectiveness of the presented model.

5   References

1. K. Yao, Y. Ren, J. Sun, K. Lee, M. Xu, J. Zhou, and F. C. Lee, *Adaptive Voltage Position Design For Voltage Regulators*, in Proc. IEEE APEC'04 Conf., 2004, pp. 272 – 278.
2. K. Y. Cheng and Y. Su, *Adaptive Voltage Positioning Design of Multiphase Constant On-time I^2 Control For Voltage Regulators With Ramp Compensations*, in Proc. IEEE APEC'16 Conf., 2016.

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