Application Report
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Loop Response Considerations for Peak Current Mode Buck LED Driver Application

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ABSTRACT

A popular LED driver is the internal loop compensated Peak Current Mode (PCM) buck. The loop response is good for proper inductor and output capacitor design, but improper inductor and output capacitor values can lead to instability or bad transient performance. This application report details the PCM buck LED driver, analyzes the stability constraint, and provides a simple equation to calculate bandwidth and phase margin of the converter.

The model proposed in this application report is introduced in Section 1. Section 2 provides peak current mode loop modeling. The inside current loop is simplified as a single pole. The overall loop response transfer function is obtained. The inductor and output capacitor design limits are derived considering loop response. At the end of this section, the equation to calculate bandwidth and phase margin is provided. In Section 3, the inductor and output capacitor is designed step-by-step considering loop response. The theory is verified by simulation and bench measurement results.

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1 Introduction

This application report uses the TPS92200D1 and TPS92200D2[1] (hereafter referred to as TPS92200D1/D2) as the example to analyze the control loop. The TPS92200D1/D2 regulator is an easy-to-use synchronous step-down LED driver operating from 4-V to 30-V supply voltage. It is capable of delivering up to 1.5-A DC load current in a very small solution size with very flexible dimming method. The device is suitable for a wide range of applications from consumer to industrial for power conditioning from an unregulated source. The TPS92200D1/D2 employs peak-current mode control with internal loop compensation, which reduces design time, and requires few external components.

A lot of PCM loop models are available for system design. The most popular model is provided in *A New Small-Signal Model for Current-Mode Control* [2]. The model predicted the sample and hold effects in the current loop, while using a three-terminal switch model to calculate the power stage small-signal model. Using this method, a simplified loop model is provided in the *TPS65270 Loop Compensation Design Consideration Application Report*[3], and an equivalent circuit is obtained to simulate the loop response. However, all of the models require simulation tools to draw the bode plot, then find a crossover frequency and phase margin based on the bode plot. Besides, the transfer function of inner current loop is quite complex, making it hard to understand how it impacts the whole loop response. In this document, a simple equation is provided to calculate bandwidth. The phase margin is obtained by simplifying the inside current loop as a single pole. The inner current loop stability criteria can be obtained based on the model. Each zero and pole in the model has a clear physical meaning, making it easy to analyze the impact of each component value on the loop response. The inductor and output capacitor design procedure of the internally compensated PCM buck LED driver is given using the model. The model accuracy is verified by both simulation and bench measurement results.

2 Peak Current Mode Loop Modeling

2.1 Overall Control Block Diagram and Transfer Function Derivation

Figure 1 shows the simplified schematic for the PCM buck LED driver.

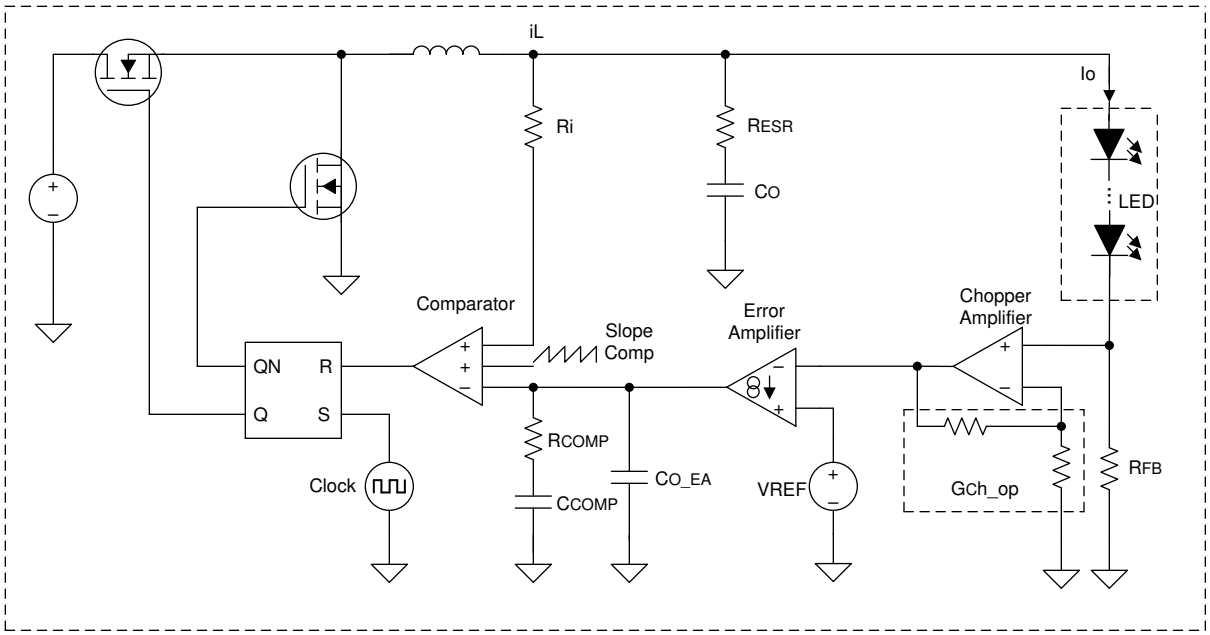

Figure 1. Simplified Schematic for PCM Buck LED Driver

Since this is for an LED driver, the load is a little different comparing with traditional resistor load when considering the loop. The LED has the non-linear V-I characteristic, Figure 2 shows a typical V-I characteristics of the Osram Infrared (IR) LED: SFH4715A.

It is clear that the LED needs a threshold bias voltage, it only conducts some leakage current below the minimum forward threshold bias voltage. And it is also non-linear above threshold bias voltage. When considering the loop response of the LED load, it needs to linearize near the working point. For example, when it works under 1.5 A, the forward voltage is about 1.44 V, it can gets the linearized resistance R_{LED} as shown in Figure 2.

It models the LED load with a DC bias power supply Vth with a serial resistance R_{LED} as Figure 2 shows.

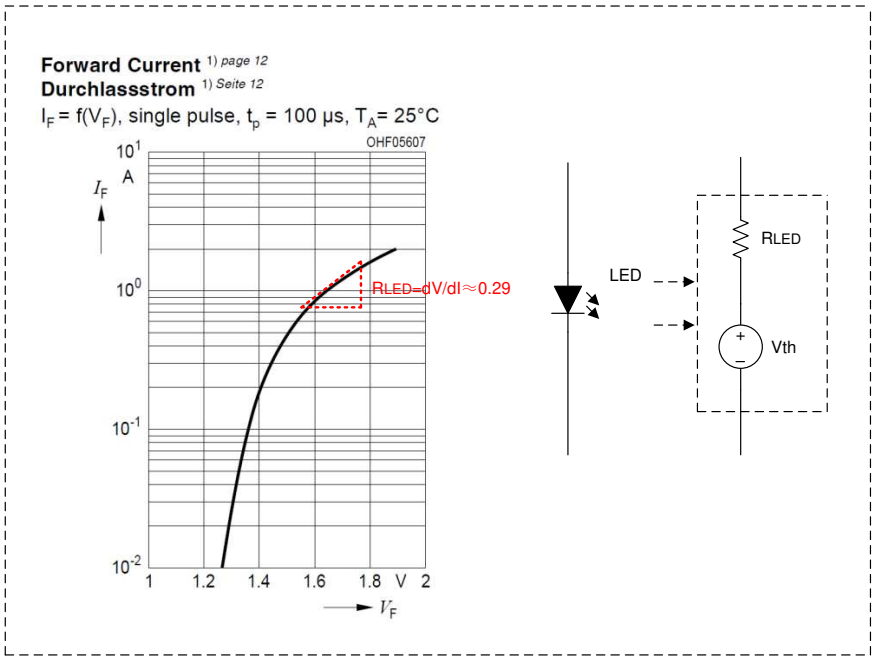

Figure 2. V-I Characteristic of LED(SFH4715A)

Figure 3 shows the tested R_{LED} of IR LED (SFH4715A) and White LED (XMLAWT0T5051).

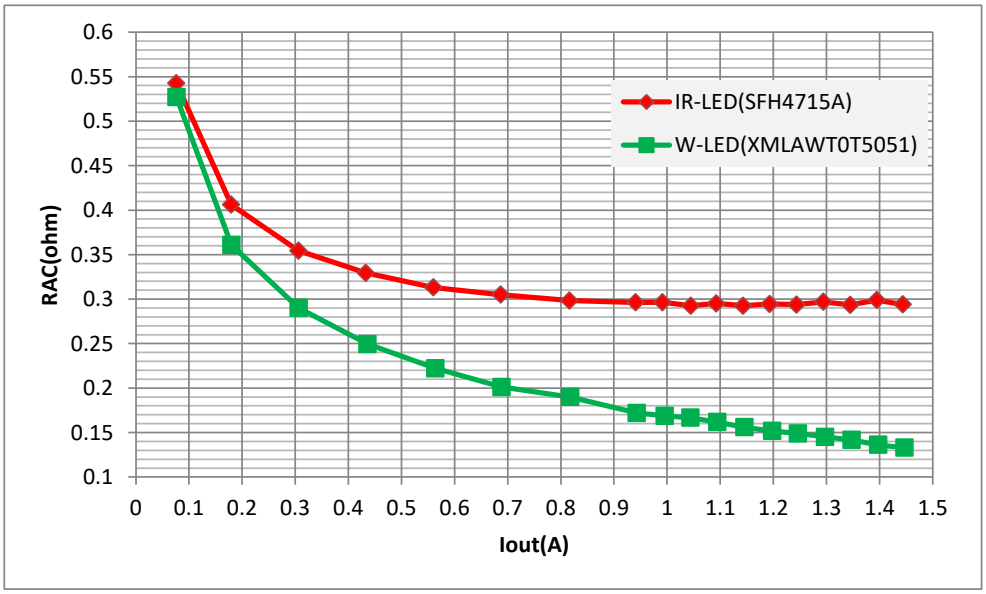

Figure 3. R_{LED} Test

When the LED model is connected to the circuit in Figure 1, you get a simplified schematic for the PCM buck LED driver as Figure 4 shows.

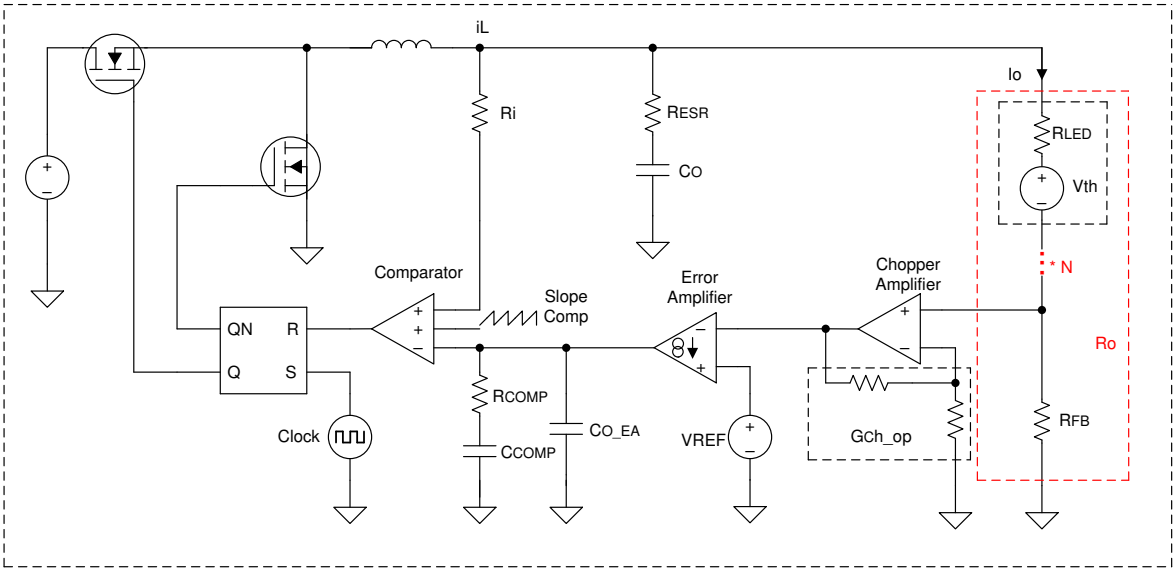

Figure 4. Update Simplified Schematic for PCM Buck LED Driver

R_{FB} is used to set the maximum current, Since R_{FB} is serially connected with the LED load, so the total output resistance load is obtained as Figure 5 illustrates.

$$R_o = N * R_{LED} + R_{FB} \quad (1)$$

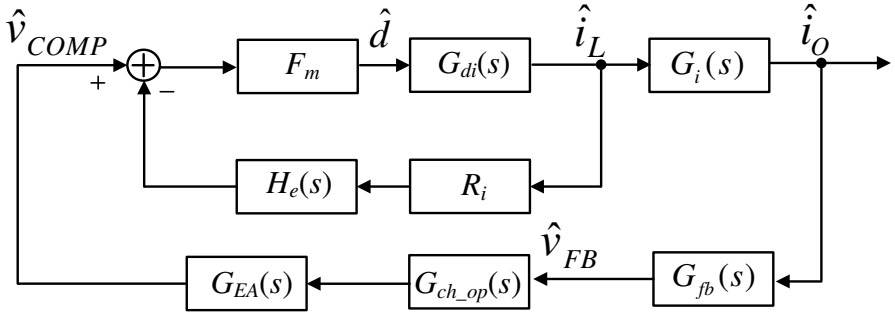

Figure 5. Overall Control Implementation

Figure 5 shows the overall control block model where:

- $G_{di}(s)$ is the duty cycle to i_L transfer function
- $G_i(s)$ is the i_L to i_o transfer function
- $G_{fb}(s)$ is the i_o to V_{FB} transfer function
- $G_{ch\_op}(s)$ is the gain of the chopper amplifier
- $G_{EA}(s)$ is the transfer function of the error amplifier with certain compensation
- F_m is the gain of PCM PWM comparator
- R_i is the current sensing resistor
- $H_e(s)$ is the transfer function model of inductor current sampling-hold effect

Equation 2 shows the transfer function from the inductor current to the output current.

$$G_i(s) = \frac{\hat{i}_O(s)}{\hat{i}_L(s)} = \frac{1 + sR_{ESR}C_O}{1 + s(R_{ESR} + R_O)C_O} \quad (2)$$

$G_{di}(s)$ is the duty cycle to the i_L transfer function.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_{IN}(1 + sC_OR_O)}{R_O + sL + s^2LC_OR_O} \quad (3)$$

The internal loop compensation is designed so that the crossover frequency is much higher than the corner frequency, $1/(2\pi\sqrt{LC_O})$. For crossover frequency and higher frequency, Equation 3 can be simplified as Equation 4.

$$G_{di}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} \approx \frac{V_{IN}}{sL} \quad (4)$$

The sensed inductor current, external ramp, and the output of error amplifier V_{COMP} are compared, which determines when to turn off the high-side MOSFET, hence the duty cycle is determined. F_m is the comparator gain. f_{SW} is the switching frequency. S_n is the on-time slope of the sensed-current waveform and S_e is the external ramp slope.

$$F_m = \frac{f_{SW}}{S_n + S_e}$$

where

- $S_n = R_i \frac{V_{IN} - V_O}{L}$
- $S_e = V_{Se} \times f_{SW}$ (5)

$H_e(s)$ is the transfer function model of inductor current sampling-hold effect. [2]:

$$H_e(s) = \frac{s/f_{SW}}{e^{s/f_{SW}} - 1} \approx 1 - \frac{s}{2f_{SW}} + \frac{s^2}{(\pi f_{SW})^2} \quad (6)$$

Equation 7 shows the transfer function from i_L to i_o.

$$G_{fb}(s) = \frac{\hat{v}_{FB}(s)}{\hat{i}_O(s)} = R_{FB} \quad (7)$$

Equation 8 shows the transfer function of the error amplifier with certain compensation.

$$G_{EA}(s) = \frac{\hat{v}_{COMP}(s)}{\hat{v}_{FB}(s)} = -G_m \frac{1 + sR_{COMP}C_{COMP}}{s(C_{COMP} + C_{O\_EA}) * \left(1 + sR_{COMP}\frac{C_{COMP}C_{O\_EA}}{C_{COMP} + C_{O\_EA}}\right)} \quad (8)$$

2.2 Inside Current Loop Model

Based on Equation 4 to Equation 6 and Figure 5, the transfer function from control to inductor current is $G_{ci}(s)$:

$$G_{ci}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)} = \frac{1}{R_i} \frac{1}{1 + s \times \left[\frac{V_{Se}f_{SW}L + (0.5V_{IN} - V_O)R_i}{V_{IN}R_if_{SW}}\right] + s^2 \times \frac{1}{(\pi f_{SW})^2}} \quad (9)$$

For the PCM buck converter, the crossover frequency is much smaller than half of the switching frequency, so around the crossover frequency, Equation 9 can be simplified as Equation 10. The inside current loop is simplified as a single pole, which is very helpful for the loop response analysis of the PCM buck converter.

$$G_{ci}(s) = \frac{\hat{i}_L(s)}{\hat{v}_{COMP}(s)} = \frac{1}{R_i} \frac{1}{1 + s \times \left[\frac{V_{Se}f_{SW}L + (0.5V_{IN} - V_O)R_i}{V_{IN}R_if_{SW}}\right]} \quad (10)$$

If the inside current loop $G_{ci}(s)$ is not stable, subharmonic oscillation occurs. A system is stable as long as each of the poles of the closed loop transfer function lies in the left half plane. The minimum inductor value is calculated to prevent subharmonic oscillation:

$$L > \frac{R_i(V_O - 0.5V_{IN})}{V_{Se} f_{SW}} \tag{11}$$

2.3 Overall Loop Model

f_{Z_EA} and f_{P_EA} are zeros and poles introduced by the error amplifier with certain compensation. f_{Z_OUT} and f_{P_OUT} are zeros and poles introduced by the output capacitor and load. f_{P_ci} is the pole introduced by the inside current loop. Based on Equation 2, Equation 7, Equation 8, and Equation 10, the open loop transfer function L(s) around crossover frequency is obtained:

$$L(s) = G_i(s) \times G_{fb}(s) \times G_{EA}(s) \times G_{ci}(s) = -K \frac{\left(1 + \frac{s}{2\pi f_{Z\_EA}}\right) \times \left(1 + \frac{s}{2\pi f_{Z\_OUT}}\right)}{s \times \left(1 + \frac{s}{2\pi f_{P\_EA}}\right) \times \left(1 + \frac{s}{2\pi f_{P\_ci}}\right) \times \left(1 + \frac{s}{2\pi f_{P\_OUT}}\right)}$$

where

- $K = \frac{Gch\_op * G_m * R_{FB}}{R_i(C_{COMP} + C_{O\_EA})}$
- $f_{Z\_EA} = \frac{1}{2\pi R_{COMP} C_{COMP}}$
- $f_{P\_EA} = \frac{1}{2\pi R_{COMP} \frac{C_{COMP} C_{O\_EA}}{C_{COMP} + C_{O\_EA}}}$
- $f_{P\_ci} = \frac{V_{IN} R_i f_{SW}}{2\pi[V_{Se} f_{SW} L + (0.5V_{IN} - V_O)R_i]}$
- $f_{Z\_OUT} = \frac{1}{2\pi R_{ESR} C_O}$
- $f_{P\_OUT} = \frac{1}{2\pi(R_{ESR} + R_O)C_O}$

(12)

2.4 Inductor and Output Capacitor Design Limits

Figure 6 shows the Bode plot with proper inductor and output capacitor design.
$f_c > f_{P\_OUT}$, $f_c > f_{Z\_EA}$, $f_c \ll f_{P\_EA}$, $f_c \ll f_{P\_ci}$, $f_c \ll f_{Z\_OUT}$

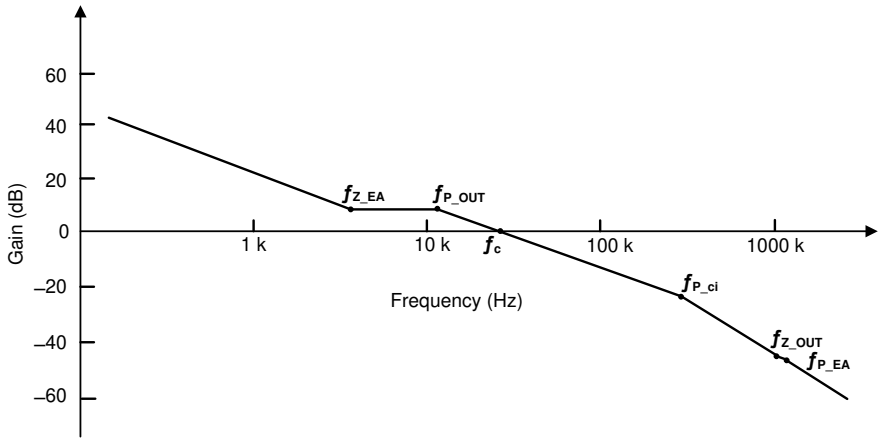

Figure 6. Bode Plot Model for PCM Buck LED Driver

The gain curve must go across 0 dB with a –20 dB/dec slew rate, so that the phase margin is enough. The zero introduced by the compensation network f_{Z_EA} cancels the pole of output impedance f_{P_OUT}, and they are placed before crossover frequency: $f_{P\_OUT} < f_c$, $f_{Z\_EA} < f_c$. The parasitic capacitor of error amplifier C_{O_EA} is quite small, so $f_{P\_EA} \gg f_c$.

If L is too large, the pole introduced by the current loop f_{P_ci} is smaller than the crossover frequency f_c. The gain curve goes across 0 dB with a –40 dB/dec slew rate, and the phase margin is not enough. Additionally, the loop response is influenced by V_{IN} since f_{P_ci} is influenced by V_{IN}. To prevent that from happening, L must be properly designed to ensure $f_{P\_ci} \gg f_c$. Equation 13 calculates the maximum inductor value.

$$L \ll \frac{V_{IN} R_i}{2\pi f_c V_{Se}} + \frac{(V_O - 0.5V_{IN})R_i}{V_{Se} f_{SW}} \tag{13}$$

If the Equivalent Series Resistance (ESR) of the output capacitor is too large, the zero introduced by the output capacitor f_{Z_OUT} is smaller than the crossover frequency f_c. The gain curve has a 0 dB/dec slew rate after f_{Z_OUT}, which makes the crossover frequency too large. Some high-frequency poles introduced by the parasitic parameters in the IC influence the phase margin, and the phase margin is not enough. To prevent that, the ESR of the output capacitor must be properly designed to ensure $f_{Z\_OUT} \gg f_c$. Equation 14 calculates the maximum ESR.

$$R_{ESR} \ll \frac{1}{2\pi f_c C_O} \tag{14}$$

2.5 The Equation to Calculate Bandwidth and Phase Margin

From Equation 12 and considering $f_c \gg f_{P\_OUT}$, $f_c \gg f_{Z\_EA}$, $f_c \ll f_{P\_EA}$, $f_c \ll f_{P\_ci}$, and $f_c \ll f_{Z\_OUT}$, the magnitude of the open loop transfer function at crossover frequency f_c is shown in Equation 15.

$$|L(j2\pi f_c)| = K \frac{\left|1 + j\frac{f_c}{f_{Z\_EA}}\right| \times \left|1 + j\frac{f_c}{f_{Z\_OUT}}\right|}{2\pi f_c \times \left|1 + j\frac{f_c}{f_{P\_EA}}\right| \times \left|1 + j\frac{f_c}{f_{P\_ci}}\right| \times \left|1 + j\frac{f_c}{f_{P\_OUT}}\right|} \approx K \frac{\left|1 + j\frac{f_c}{f_{Z\_EA}}\right|}{2\pi f_c \times \left|1 + j\frac{f_c}{f_{P\_OUT}}\right|} = 1 \tag{15}$$

Considering $R_{ESR} \ll R_O$, the crossover frequency f_c is obtained in Equation 16.

$$f_c = \frac{(KR_{COMP}C_{COMP} - 1) + \sqrt{(1 - KR_{COMP}C_{COMP})^2 + 4KR_oC_o}}{4\pi R_o C_O} \tag{16}$$

Phase margin is the phase of the open loop transfer function at f_c minus –180º: Equation 17

$$PhaseMargin = 90° - \arctan\left(2\pi f_c R_O C_O\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_c R_{COMP} C_{COMP}\right) \times \frac{180°}{\pi} - \arctan\left(2\pi f_c R_{COMP} C_{O\_EA}\right) \times \frac{180°}{\pi} - \arctan\left(\frac{2\pi f_c \left[V_{Se} f_{SW} L + (0.5V_{IN} - V_O)R_i\right]}{V_{IN} R_i f_{SW}}\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_c R_{ESR} C_O\right) \times \frac{180°}{\pi} \tag{17}$$

3 Inductor and Output Capacitor Design

In this section, the inductor and output capacitor is designed in a practical application using TPS92200D1/D2. The loop response is considered during the process. Table 1 lists the design specifications.

Table 1. Design Example Specification

V_{IN} (V)	V_O (V)	I_O (A)	I_{O_min} (A)	f_{SW} (kHz)	OUTPUT RIPPLE (mV)	V_{REF} (V)
8 V to 16 V, typical 12 V	3.6 (2 IR-LED)	1.0	0.1	1000	< 30	1.2

3.1 Inductor Design

Equation 18 calculates the value of the output conductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device (For TPS92200D1/D2, the maximum output current I_{O_max} is 1.5 A). A reasonable value of K_{IND} is 0.2 – 0.4. Since the ripple current increases with the input voltage, the maximum input voltage is used to calculate the minimum inductance L_{MIN}, while K_{IND} = 0.2 is selected. The maximum inductor value is calculated to be 4.65 µH. Choose the nearest standard inductor: L= 4.7 µH.

$$L_{max} = \frac{V_{IN\_max} - V_O}{I_{O\_max} \times K_{IND}} \times \frac{V_O}{V_{IN\_max} \times f_{SW}} \tag{18}$$

From Equation 13, the maximum inductor value is calculated to get enough phase margin. Three times margin is suggested and the limit is calculate in Equation 19 with the TPS92200D1/D2 internal parameter. If you assume the target crossing over frequency f_c is about 20 kHz, then the result is L < 60 µH at the minimum V_{IN}. The selected 4.7-µH inductor meets the requirement.

$$L < \frac{1}{3}\left[\frac{V_{IN}}{2\pi f_c \times 0.441} + \frac{(V_O - 0.5V_{IN})}{f_{SW} \times 0.441}\right] \tag{19}$$

The TPS92200D1/D2 is protected from overcurrent conditions with the cycle-by-cycle current limit. To prevent inductor saturation in case of short circuit conditions, the inductor saturation current must be greater than the device maximum peak current limit, which is 3.3 A (typical) for the TPS92200D1/D2.

3.2 Output Capacitor Design

The output capacitor is designed based on output ripple and loop response. The output voltage ripple is composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitor, see Equation 20. The other is caused by the inductor current ripple charging and discharging the output capacitor, see Equation 21. The target output ripple is 30 mV, so ΔV_{O_ESR} < 30 mV and ΔV_{O_C} < 30 mV, then R_{ESR} < 125 mΩ and C_O > 0.91 µF.

$$\Delta V_{O\_ESR} = I_O \times K_{IND} \times R_{ESR} \tag{20}$$

$$\Delta V_{O\_C} = \frac{I_O \times K_{IND}}{8 \times f_{SW} \times C_O} \tag{21}$$

From Equation 14, the maximum ESR value is calculated to get a reasonable crossover frequency and enough phase margin. If you assume the target crossing over frequency f_c is about 20 kHz, then the result is $R_{ESR} \ll$ 796 mΩ. Three times the margin is suggested and the result is R_{ESR} < 265 mΩ.

Output capacitor value determines loop response in internally compensated PCM buck converters, as Equation 16 and Equation 17. With TPS92200D1/D2 internal parameter, the calculation equation is as in Equation 22 and Equation 23. The target f_c is about 20 kHz, so C_O is about 12.4 µF. One 10-µF, 16-V ceramic capacitor with 2-mΩ ESR is used: C_O = 10 µF, R_{ESR} = 2 mΩ. The crossover frequency is f_c = 20.8 kHz and the phase margin is calculated as 114.6º at V_{IN} = 12 V, I_O = 1.0 A.

$$f_c = \frac{(13.638R_{FB} - 1) + \sqrt{(1 - 13.638R_{FB})^2 + 2727272R_{FB}R_OC_O}}{4\pi R_OC_O} \tag{22}$$

$$PhaseMargin = 90° - \arctan\left(2\pi f_c R_{_O} C_O\right) \times \frac{180°}{\pi} + \arctan(2\pi f_c \times 20\mu) \times \frac{180°}{\pi} - \arctan(2\pi f_c \times 0.01115\mu) \times \frac{180°}{\pi} - \arctan\left(\frac{2\pi f_c\left(f_{SW}L \times 0.441 + 0.5V_{IN} - V_O\right)}{V_{IN}f_{SW}}\right) \times \frac{180°}{\pi} + \arctan\left(2\pi f_c R_{ESR} C_O\right) \times \frac{180°}{\pi} \tag{23}$$

3.3 Simulation and Bench Verification

Figure 7 shows the schematic for bench verification. SIMPLIS is used to simulate the loop response as shown in Figure 8. Figure 9 and Figure 10 are the loop responses from the SIMPLIS simulation and bench test under V_{IN} = 12 V, V_O = 3.6 V, I_O = 1.5 A, and f_{SW} = 1.0 MHz. Table 2 compares the calculation results, simulation results, and bench measurement at different V_{IN}. It can be seen that the proposed model in this application report is accurate.

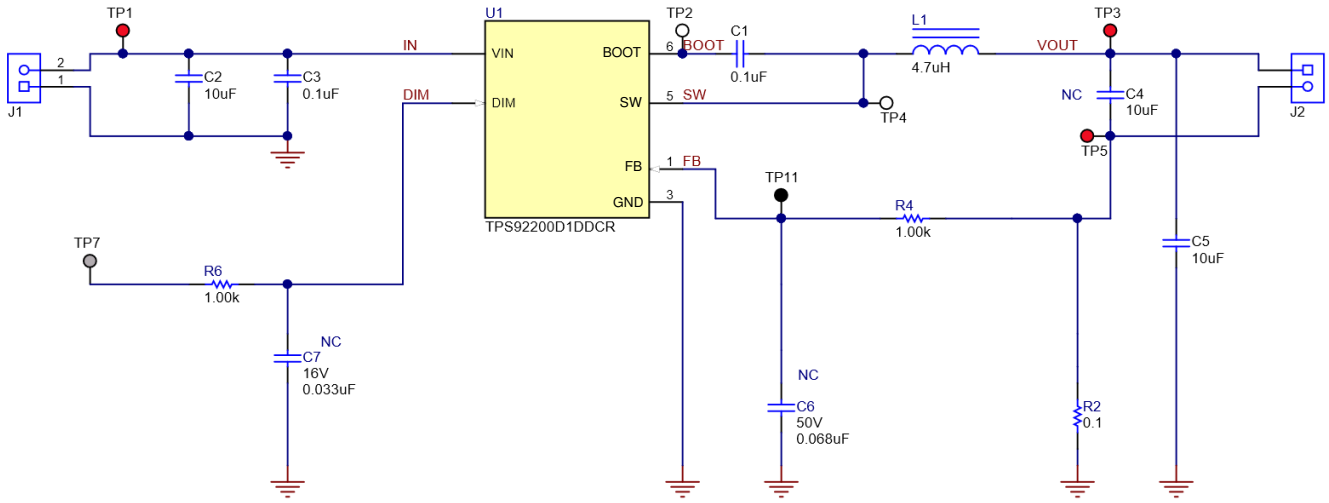

Figure 7. TPS92200D1 Design With 2 IRLED, 1.0-A Output

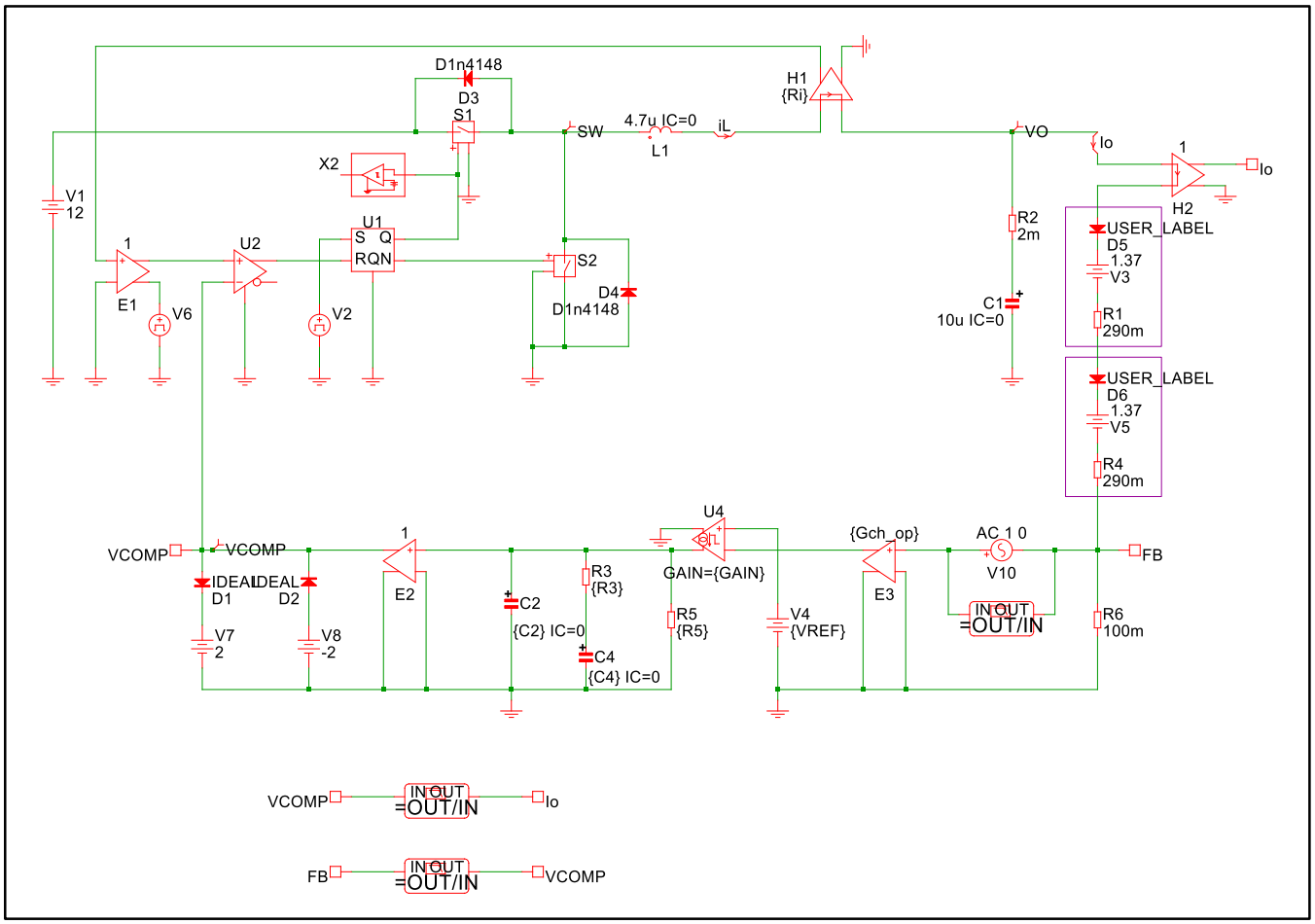

Figure 8. Schematic of a Simplified SIMPLIS Model

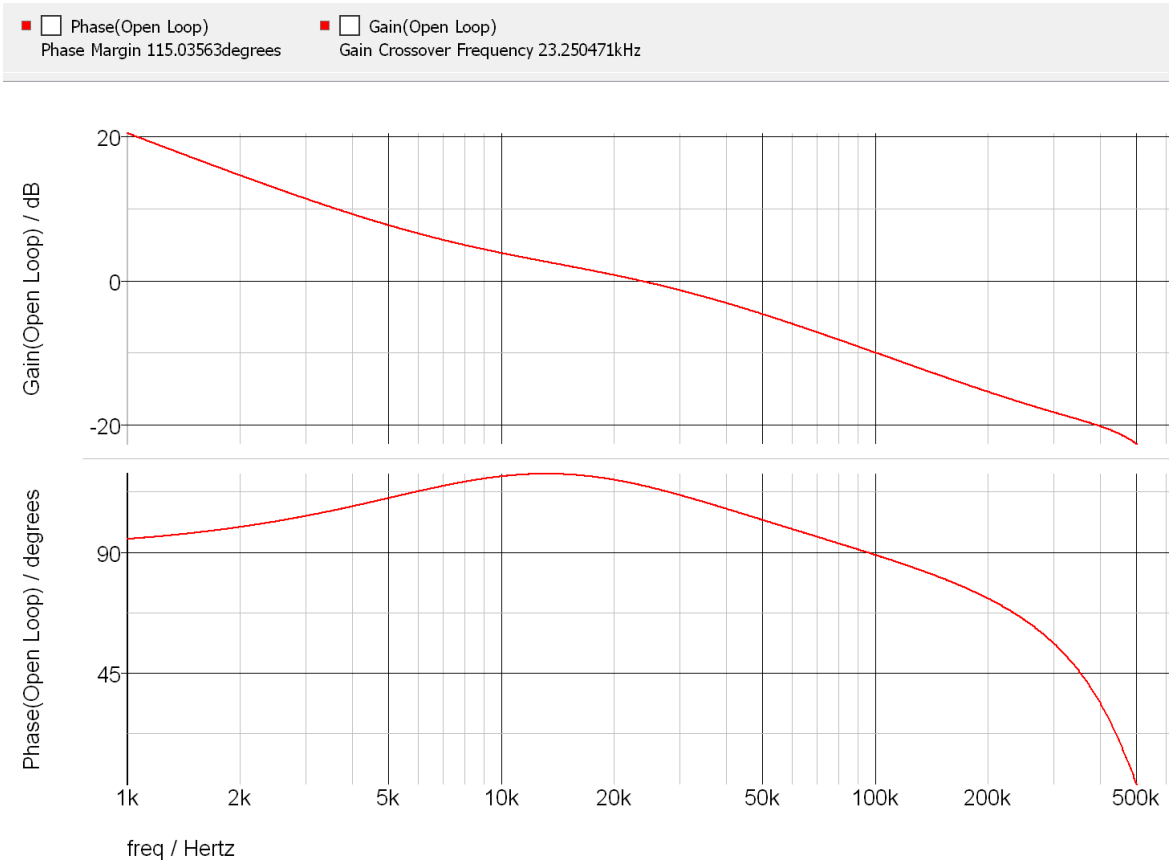

Figure 9. Bode Plot Simulation Result at V_{IN} = 12 V, I_O = 1 A

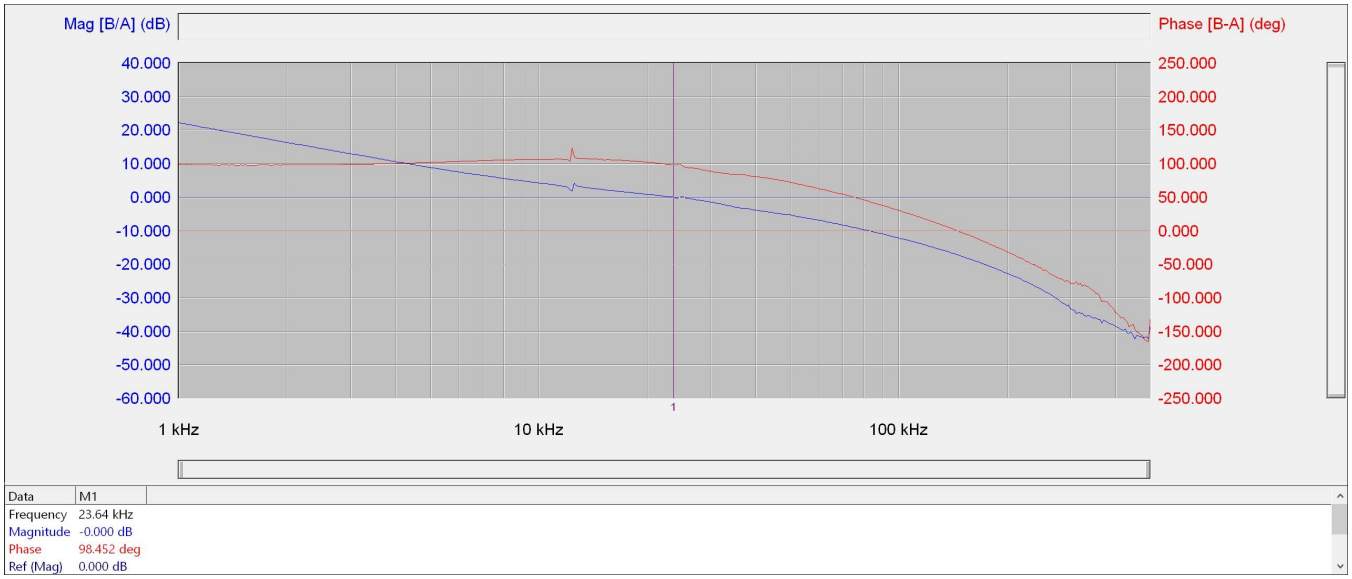

Figure 10. Bode Plot Test Result at V_{IN} = 12 V, I_O = 1 A

Table 2. Calculation, Simulation, and Bench Measurement Results Comparison

V_{IN} (V)	I_O (A)	LED Load	CALCULATION RESULTS		SIMULATION RESULTS		BENCH MEASUREMENT	
			f_c (kHz)	PHASE MARGIN (°)	f_c (kHz)	PHASE MARGIN (°)	f_c (kHz)	PHASE MARGIN (°)
12	1	2 IR LED	20.8	114.6	23.25	115.0	23.64	98.5
12	1	4 IR LED	14.2	100.5	15.25	101.46	12.69	101.4
24	1	6 IR LED	11.8	93	12.55	97.2	12.0	90.1
24	1	4 White LED	20.91	117.2	21.39	113.1	23.26	100.7
24	1	6 White LED	13.6	101.24	16.94	104.7	17.45	94.7

4 Summary

For an internally-compensated, Peak Current Mode buck LED driver, the loop response is very different to the traditional buck converter due to the different load connection and character [4][5]. It should pay more attention to choose the inductor and output capacitor. This application report analyzes the whole loop of the PCM buck LED driver, simplifies the inside current loop as a single pole, provides the constraint to ensure loop stability, and gives out an equation to calculate bandwidth and phase margin. The inductor and output capacitor is designed step-by-step considering loop response. The theory is verified by simulation and bench measurement results.

5 References

1. Texas Instruments, *TPS92200 4-V to 30-V, 1.5A Synchronous Buck LED Driver With Flexible Dimming Options Data Sheet*
2. R.B. Ridley, A New Small-Signal Model for Current-Mode Control, PhD Dissertation, Virginia Polytechnic Institute and State University, November, 1990.
3. Texas Instruments, *TPS65270 Loop Compensation Design Consideration Application Report*
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5. Texas Instruments, *Loop Response Consideration in Peak Current Mode Buck Converter Design Application Report*

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