Application Note

Implementation of PSYS Monitor Using TPS25984, TPS25985, or TPS25990 eFuses

Avishek Pal, Abhinay Patil, Vasav Gautam

ABSTRACT

In enterprise server applications, the latest Intel® VR14 specification introduces the requirement for accurate system input power monitoring. This allows tracking of average system input power, estimating the execution time of high power bursts, and signaling to reduce power when system input power exceeds a critical threshold. System input power can be directly monitored using an input-power signal or indirectly using system input current and system-input voltage as alternatives.

This application note demonstrates accurate and high-speed system input current monitoring using TPS25984, TPS25985, or TPS25990 eFuses to implement PSYS™ and PSYS_CRIT#™ in a VR14 multi-phase controller. This document begins with the definitions of PSYS™ and PSYS_CRIT#™, along with their accuracy and bandwidth requirements. Next, the implementation of the PSYS monitor is discussed. Then, the ISYS register and gain selection guidelines in conjunction with TPS25984, TPS25985, or TPS25990 eFuses are depicted, along with a design example. After that, the functional verification of PSYS™ and PSYS_CRIT#™ in the TPS536C9T VR14 controller are presented. Finally, the aggregation of the voltage outputs from multiple PSYS monitors connected to the same input power supply is illustrated in detail.

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Trademarks

1 Introduction

A typical server platform contains one or more processor units (CPU) as well as other sub-systems and is powered by one or multiple power supplies (PSU). In a broader sense, the PSUs are categorized as common redundant power supply (CRPS) and non-CRPS PSUs. CRPS PSUs have crisply defined peak power capabilities, whereas non-CRPS PSUs have no standard of behavior beyond their 100% rated power. The most critical case of PSU configurations is one where a single PSU is operational and that cannot handle all the projected peak power envelope demanded by the platform. Therefore, the total power drawn by the platform must be continuously monitored, and there must be a protection mechanism to throttle the power demanded by the platform quickly once a pre-programmed threshold is exceeded.

The system input power monitor, PSYS is designed to provide information necessary for the processor to dynamically allocate power between different system components, such as the CPU, memory, and the rest of the platform, within a designated power budget. This helps in optimal use of total available platform power by facilitating the dynamic employment of surplus system power to assist the platform turbo. In the absence of accurate system current monitoring, the platform designer sets the peak power limit too low, potentially settling for a too conservative power envelope. This results in sub-optimal utilization of available platform power.

PSYS_CRIT#™ is a must-have requirement in the case of non-CRPS generic PSUs to handle peak power events. Otherwise, these peak power events can, depending on their dwell time, shut down or damage platform power sources. Implementing the PSYS_CRIT#™ functionality enables the use of PSUs with generic specifications without making it mandatory to procure CRPS PSUs.

2 What are PSYS™ and PSYS_CRIT#™?

In multi-phase voltage regulator (VR) systems, system input power is delivered at a single nominal voltage level. This voltage can be supplied by a single PSU or by multiple redundant PSUs connected in parallel. A simplified block diagram is shown in Figure 2-1.

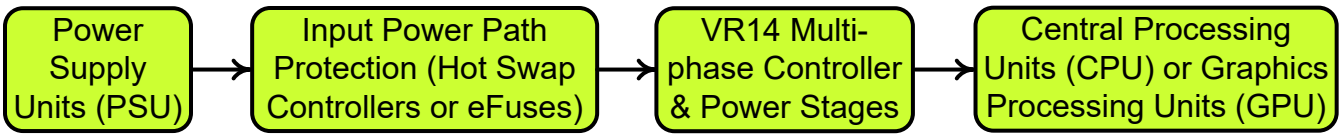

Figure 2-1. Simplified Block Diagram: Voltage Regulator (VR) Systems

The PSU can be either an AC/DC supply or a bus bar from a rack-level power supply. The VR14 controller computes system input power from input current (ISYS) and voltage (VSYS) signals. Even at the very highest power levels, the system input voltage, VSYS, is assumed to be nearly constant. At peak PSU output, VSYS can have a predictable droop. System input power is computed via the product of ISYS and VSYS. This power monitoring functionality is called PSYS™ and is used for the manipulation of CPU performance by taking advantage of available surplus average (and, in some instances, peak) energy.

The PSYS interconnection block diagram is shown in Figure 2-2. It illustrates the location of the PSYS monitor, which is typically located near the input power source connector(s) or PSU and the VR14 PWM controller. These are situated at the opposite ends of a platform assembly. This helps improve the noise immunity of the analog signal used to track input power, in this case, PSU current, or ISYS.

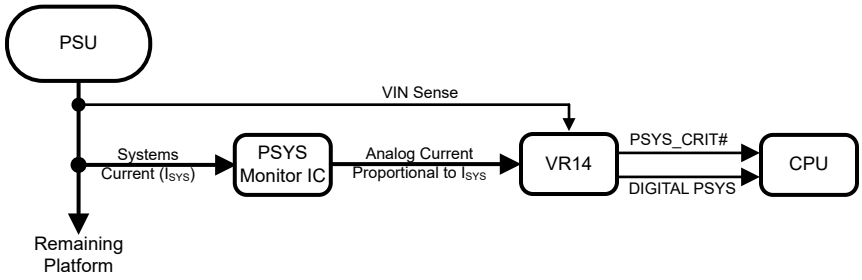

Figure 2-2. Simplified Diagram of the PSYS Interconnection

VSYS and ISYS are tracked separately, digitized, and multiplied in the VR14 PWM controller to obtain the PSYS digital output, as shown in Figure 2-3(a). Alternatively, VSYS and ISYS are multiplied in real time in the analog domain, and the result is digitized to obtain the PSYS digital output, as shown in Figure 2-3(b). Both approaches are valid if the digital PSYS output accuracy expectations are met.

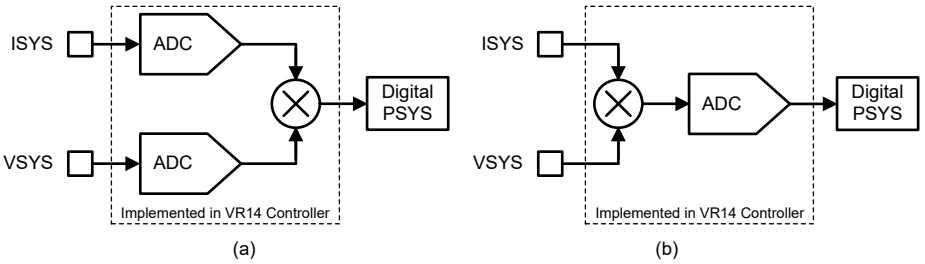

Figure 2-3. Implementation of the Digital PSYS™ in VR14 Controller

ISYS: To improve noise immunity, PSU current information is required to be represented using a current proportional to the current observed at the sensor. The ways to generate the ISYS output are described in detail in Section 3.

VSYS: It is the voltage at the input to the platform, near the output of the PSU(s). VSYS is used to convert the ISYS information into PSYS in watts. VSYS needs to be sensed near the PSYS monitor or PSU to consider the voltage drops across the platform. If it is required to implement a resistor divider to bring the magnitude of the input voltage down to the acceptable levels of the VSYS pin in the VR controller, tight tolerance resistors (± 0.1%) are recommended to meet the PSYS accuracy requirements.

An over-stressed PSU can enter fold-back constant power mode. Observing power instead of current can not indicate to the VR14 controller the magnitude at which the PSU is being stressed. Therefore, ISYS is used as the main measurement parameter here. Another benefit of an analog ISYS-measured system is the potential aggregation of several PSYS monitor outputs.

VR14 PWM Hardware Alarms (for example, VR_HOT#™ and PSYS_CRIT#™) are needed to handle peak power events; otherwise, that can cause local voltage regulators to over-heat or damage the power supplies. Both the VR_HOT#™ and PSYS_CRIT#™ are open drain logics, active low, and are used to drive the processor's force thermal throttle input (PROCHOT#™). The VR_HOT#™ asserts when the temperature sensed by the VR controller exceeds a pre-programmed threshold (TMAX) value. The detailed implementation and functionality are not discussed in this document.

Hardware alarms are the last line of defense for systems that attempt to operate at near hardware peak power limits. This helps eliminate the requirement of over-designing the systems to handle severe (for example, much larger in magnitude than thermal design power) peak power events.

Digital versions of PSYS are useful for the monitoring of average power events. Digital PSYS is a poor indicator of peak power events. Because the time taken to digitize the VSYS and ISYS signals and multiply them to generate PSYS digital output and then react to a peak power event is beyond the input power handling capability of a generic PSU.

VR14 controller allows for monitoring peak power events. PSYS_CRIT#™ is an active low, open drain logic derived from the ISYS data to drive the processor's force thermal throttle input. The differences between VR_HOT#™ and PSYS_CRIT#™ are as follows:

- In a multi-CPU system, VR_HOT#™ is implemented in each VR14 controller by sensing their own temperature. Whereas PSYS_CRIT#™ is implemented only in one VR14 controller connected to a CPU, suppose CPU0, by sensing the total platform current drawn by the multiple CPUs and other loads.
- Each VR_HOT#™ assertion (low) only throttles the power consumption of the associated CPU, not all the CPUs. Whereas the assertion of PSYS_CRIT#™ throttles the power consumption of all the CPUs drawing power from the PSU.

The preferred method of PSYS_CRIT#™ alarm implementation is at the VR14 PWM controller level, not the PSYS monitor level. The VR14 controller implements the PSYS_CRIT#™ functionality in two ways.

- The analog ISYS signal is fed to a high-speed analog comparator to trigger the assertion of PSYS_CRIT#™ output once a threshold of current is exceeded, as shown in Figure 2-4(a).
- The digitized ISYS data is fed to a high-speed digital comparator to trigger the assertion of PSYS_CRIT#™ output once a threshold of current is exceeded, as shown in Figure 2-4(b).

Digital PSYS™ and PSYS_CRIT#™ need to maintain high accuracy (± 2%) and low latency (PSYS_CRIT#™ assertion delay of 10 µs).

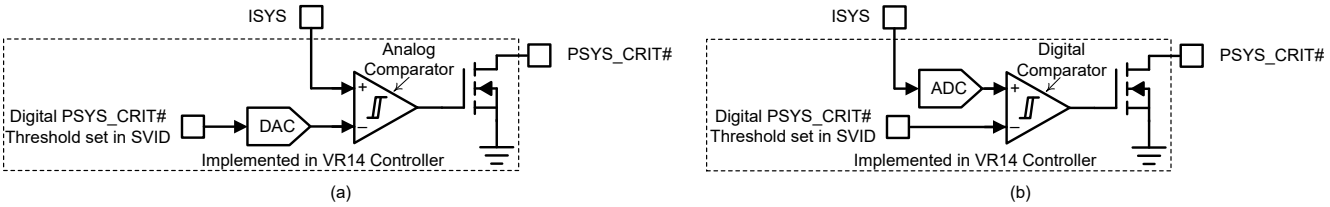

Figure 2-4. Implementation of the PSYS_CRIT#™ in VR14 Controller

3 Implementation of PSYS Monitor

The PSYS monitor is used to obtain the analog VSYS and ISYS data to implement the digital PSYS™ output and PSYS_CRIT#™ functionality in the VR14 controller.

3.1 Existing Designs

The most basic implementation consists of a sense resistor, a current sense amplifier, and a trans-conductance amplifier. Figure 3-1 depicts this implementation. These components add a significant cost to the design and an additional area on the PCB.

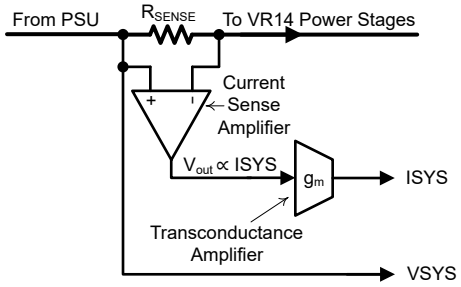

Figure 3-1. PSYS Monitor Functionality Done With Sense Resistor and Trans-Conductance Amplifier

Some implementations use the sense resistor used in hot swap designs to implement input power path protection. An additional current sense amplifier and a trans-conductance amplifier are needed in this implementation, as shown in Figure 3-2. These two discrete approaches are susceptible to system noise and tend to have lower accuracy and higher propagation delays.

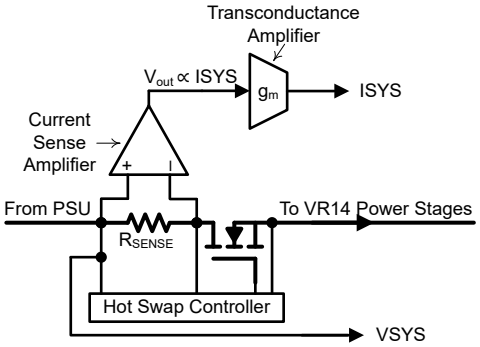

Figure 3-2. PSYS Monitor Functionality Using the Sense Resistor Used in Hot Swap Designs

Some hot swap controllers, such as the TPS2477x, feature an analog current monitoring output, which is a voltage output proportional to the load current, as shown in Figure 3-3. A trans-conductance amplifier is required to convert this voltage output to a current source proportional to the load current, which is fed to the ISYS pin of the VR14 controller. However, the accuracy and large-signal bandwidth requirements for PSYS™ implementation cannot be achieved through this approach.

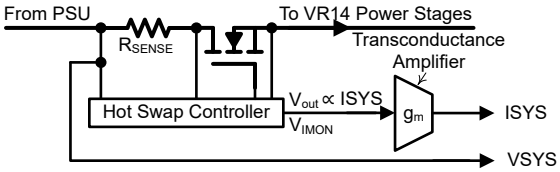

Figure 3-3. PSYS Monitor Functionality Done With Hot Swap Controller With V_{IMON} Output and Trans-Conductance Amplifier

3.2 Proposed Designs

Integrated FET-based hot swap designs, subsequently called eFuses, are commonly used in input power path protections for high-current enterprise server power supply designs because of improved power density and cost competitiveness. TI released the TPS25984, TPS25985 (both without PMBus® interface), and TPS25990 (with PMBus® interface) eFuses in the aforementioned market space.

In addition to providing several input power path protection features, these three eFuses allow the systems to monitor the output load current accurately by providing an analog current output (IMON) on the IMON pin. IMON is proportional to the current through the FET inside the eFuse. This IMON output is fed to the ISYS pin to implement PSYS™ in the VR14 controller, as shown in Figure 3-4.

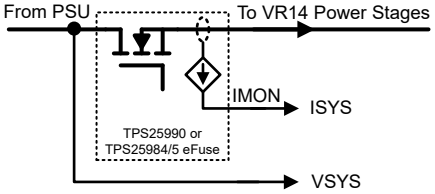

Figure 3-4. PSYS Monitor Functionality Implemented Using TPS25984, TPS25985, or TPS25990 eFuses

The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The current output also allows the IMON pins of multiple eFuse devices in a parallel configuration to be tied together to get the total current. As shown in Figure 3-5, the IMON signal is fed to the ISYS pin of the VR14 controller and is converted to a voltage by dropping it across a resistor (R_{ISYS} or R_{IMON}) close to the VR14 controller to implement the PSYS™. The current monitoring circuit inside these three eFuses is designed to provide high bandwidth (> 500 kHz) and high accuracy (<± 1.5%) across load and ambient temperature conditions, irrespective of board layout and other system operating conditions. This helps in achieving the required response time (10 µs) and error specifications (± 2%) for PSYS™ implementation. The analog current monitoring response of these eFuses is depicted in Figure 3-6 to demonstrate the large signal bandwidth of IMON. There is no need to add any external components to implement the PSYS monitor in the design.

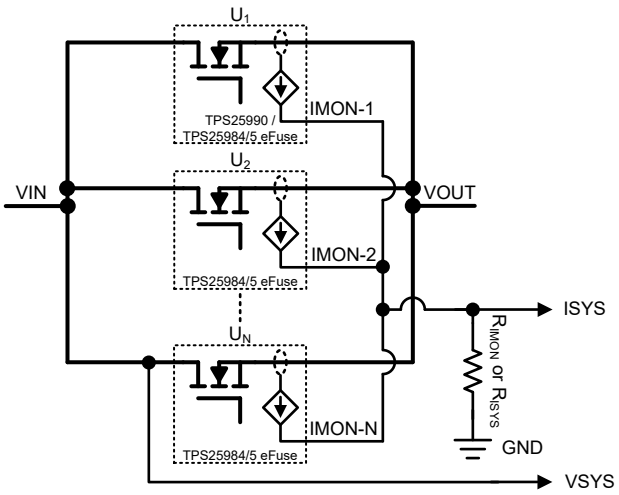

Figure 3-5. Parallel Connection: TPS25984, TPS25985, and TPS25990 eFuses

Note

The input power path protection design using TPS25984, TPS25985, or TPS25990 eFuses itself provides the functionality of the PSYS monitor by accomplishing the required large-signal bandwidth and accuracy criteria to implement PSYS™ functionality in the VR14 controllers.

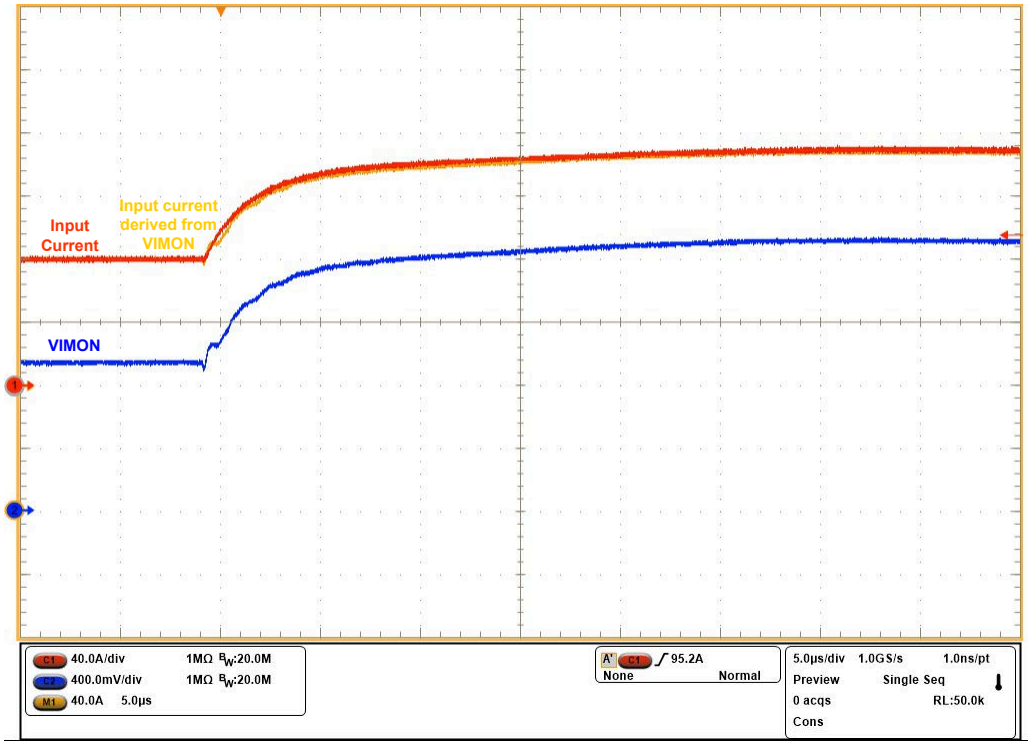

Figure 3-6. Large-Signal Current Monitoring Bandwidth of TPS25984, TPS25985, or TPS25990 eFuses

4 ISYS Resistor (R_{ISYS}) and Gain (ISYS_IN_GAIN) Selection in TPS536C9T VR14 Controller

The IMON pin in TPS25984, TPS25985, or TPS25990 eFuses serves two purposes:

- sets the over-current protection threshold and the scalable fast-trip threshold during steady-state.
- provides a fast and accurate analog output load current monitor signal during steady-state.

Therefore, the same resistance, either called R_{IMON} or R_{ISYS}, is determined by considering the required over-current protection threshold for the eFuses as well as the full-scale analog voltage range of the ISYS_IN pin in the VR14 controller.

The analog current monitoring output (I_{IMON}), sourced on the IMON pin in TPS25984, TPS25985, or TPS25990 eFuses, is defined as Equation 1.

$$I_{IMON} = I_{IN} \times G_{IMON} \quad (1)$$

G_{IMON} is the current monitor gain (I_{IMON} : I_{IN}) in TPS25984, TPS25985, or TPS25990 eFuses, whose typical value is 18.18 µA/A. I_{IN} is the total input current to the platform. The over-current condition is detected by comparing the voltage at the IMON pin (V_{IMON}) by dropping the I_{IMON} across the R_{IMON} resistance against a reference threshold of V_{IREF}. V_{IMON} is obtained using Equation 2.

$$V_{IMON} = I_{IMON} \times R_{IMON} = I_{IN} \times G_{IMON} \times R_{IMON} \quad (2)$$

The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 3. For more details, see the *Steady-State Over-current Protection (Circuit-Breaker)* section in TPS25984, TPS25985, or TPS25990 eFuses data sheets.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (3)$$

In TPS25990 eFuse, V_{IREF} is set through PMBus® using E0h register.

In TPS25984 and TPS25985 eFuses, V_{IREF} is specified by placing a resistor (R_{IREF}) at the IREF pin. Equation 4 is used to calculate the value of R_{IREF}.

$$R_{IREF} = \frac{V_{IREF}}{I_{IREF}} \quad (4)$$

I_{IREF} = 25 µA (typical).

The total platform input current drawn from the PSU, as sensed by the VR14 controller at the ISYS_IN pin, is given by Equation 5.

$$I_{SYS}(A) = I_{IN}(A) \times R_{ISYS}(\Omega) \times G_{ISYS}\left(\frac{\mu A}{A}\right) \times ISYS\_IN\_GAIN\left(\frac{A}{\mu A \times \Omega}\right) \quad (5)$$

I_{IN} is the platform current drawn from the PSU. Essentially, G_{ISYS} and G_{IMON} are the same parameter with identical values. R_{ISYS} and R_{IMON} are the same parameter with identical values.

ISYS_IN_GAIN: A scaling factor internal to the VR14 controller to account for the external gain factors G_{ISYS} and R_{ISYS}.

4.1 Steps to Calculate the Value of R_{IMON} or R_{ISYS} and ISYS_IN_GAIN

1. Find out the full-scale range of ISYS_IN pin in the VR14 controller.
2. Set the V_{IREF} to half of the maximum voltage range of the ISYS_IN input of the VR14 controller. This provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the scalable fast-trip threshold (2 × I_{OCP}).
3. Calculate the value of R_{IMON} or R_{ISYS} using Equation 3 to set the appropriate over-current protection or circuit-breaker threshold for eFuses.
4. Finally, select the internal scaling factor ISYS_IN_GAIN (set through the SVID_CONFIG) according to Equation 6.

$$ISYS\_IN\_GAIN = \frac{1}{G_{ISYS} \times R_{ISYS}} \quad (6)$$

4.2 Design Example

1. Maximum DC load current ($I_{OUT(max)}$) is considered as 200 A.
2. The circuit-breaker threshold during steady-state (I_{OCP}) is considered to be 1.1 times $I_{OUT(max)}$. Hence, I_{OCP} is set at 220 A.
3. The maximum voltage range of the ISYS_IN input of the TPS536C9T controller is 1.8 V.
4. As discussed in Section 4.1, V_{IREF} is set at half of 1.8 V, 0.9 V.
5. Using Equation 3, R_{IMON} or R_{ISYS} is calculated to be 225 Ω with G_{IMON} as 18.18 µA/A and V_{IREF} as 0.9 V. The nearest value of R_{IMON} or R_{ISYS} is 226 Ω with 0.1% tolerance and power rating of 100 mW. For noise reduction, place a 22 pF ceramic capacitor across the IMON pin and GND in the eFuses.
6. Using Equation 6, ISYS_IN_GAIN is calculated to be 245.

5 Functional Verification of PSYS and PSYS_CRIT# in TPS536C9T VR14 Controller Using TPS25984, TPS25985, or TPS25990 eFuses as PSYS Monitor

Figure 5-1 presents the basic interconnection block diagram for implementing PSYS™ and PSYS_CRIT#™ in TPS536C9T VR14 controller using TPS25984, TPS25985, or TPS25990 eFuses.

- ISYS_IN: ISYS input, full-scale range of 1.8 V,
- VSYS_IN: VSYS input, recommended range of 4.5 V to 17 V,
- PSYS_CRIT#: VR14 PSYS alert, open drain output, recommended range of - 0.1 V to 3.6 V,

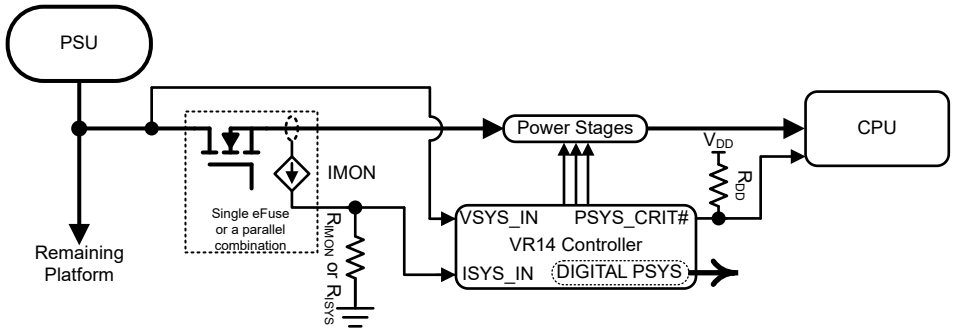

Figure 5-1. Interconnection Block Diagram Between eFuse and VR14 Controller in Implementing Digital PSYS™ and PSYS_CRIT#™

Figure 5-2 represents a snapshot of the digital PSYS output captured from the *Fusion Digital Power™ Graphical User Interface (GUI)* using TPS536C9T controller. ISYS and Digital PSYS are obtained to be 1.6% and 1.7% accurate, respectively, whereas the target specification is 2%.

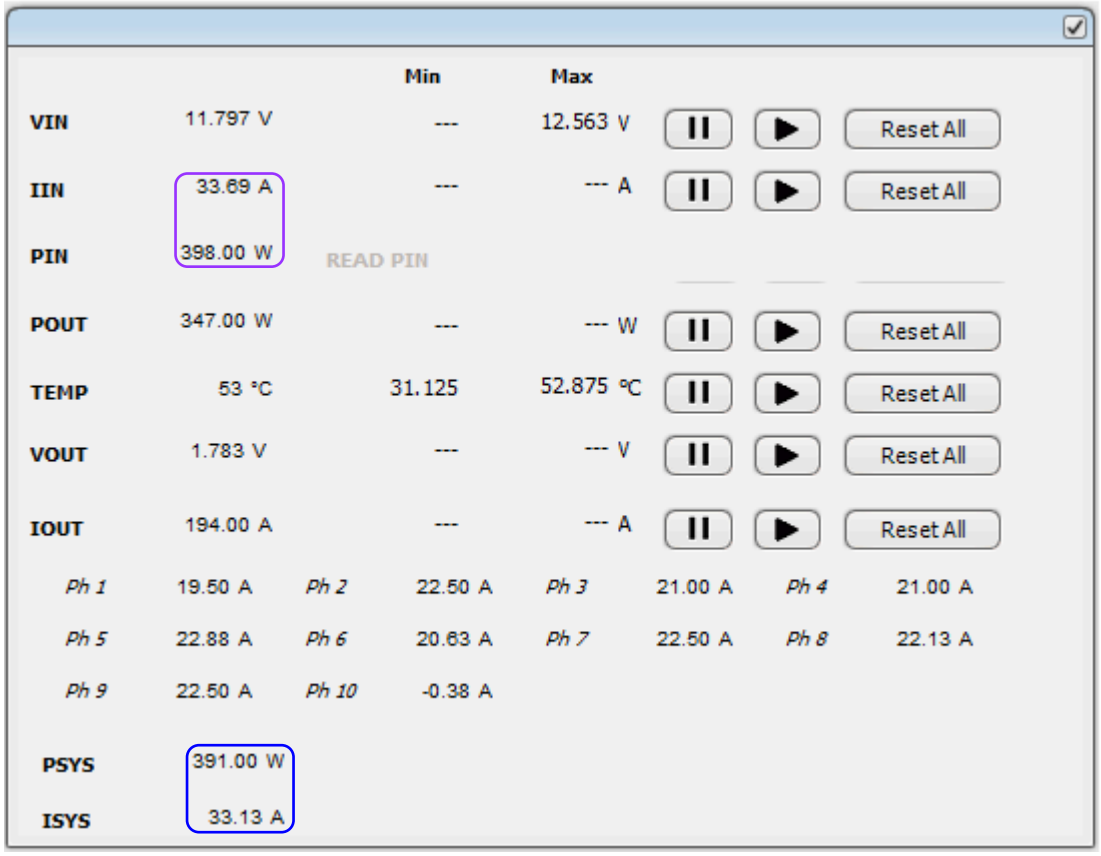

Figure 5-2. Digital PSYS

The PSYS_CRIT#™ threshold is set in the SVID register as a fraction of the maximum transient input current capability of the PSU. The threshold register contains a linear fraction of the corresponding to the telemetry input's full-scale value. The assertion of PSYS_CRIT#™ while the input current, in other words, the voltage at the ISYS pin in the TPS536C9T controller exceeds the pre-programmed threshold in SVID. The PSYS_CRIT#™ threshold in normal resolution telemetry is defined in Equation 7.

$$Digital\_PSYS\_CRIT\ \#\ \_Threshold\ (8\ bit,\ decimal) = Truncate\left[\frac{2^8 \times Analog\_PSYS\_CRIT\ \#\ \_Threshold(A)}{Full\_Scale(A)}\right];$$
$$Quantized\_Analog\_PSYS\_CRIT\ \#\ \_Threshold(A) = \left[\frac{Full\_Scale(A) \times Digital\_PSYS\_CRIT\ \#\ \_Threshold\ (8\ bit,\ decimal)}{2^8}\right] \quad (7)$$

The time delay in asserting the PSYS_CRIT#™ is depicted in fontoxml-text-placeholder text="Type the link text". The maximum delay contributed by the TPS25984, TPS25985, or TPS25990 eFuses in monitoring the PSU current (or platform current) is less than 500 ns, as shown in Figure 3-6. Therefore, the total delay between exceeding the PSU current beyond the pre-programmed threshold and the assertion of PSYS_CRIT# in the TPS536C9T controller is 5.5 µs, whereas the PSYS specifications require 10 µs.

Given *Analog_PSYS_CRIT#_Threshold as 73 A, Full_Scale as 252 A,* and using Equation 7, the *Digital_PSYS_CRIT#_Threshold (8 bit, decimal)* is calculated to be 74, in hexadecimal 4Ah. This hexadecimal data is written into a specified SVID resister to assert the PSYS_CRIT# when the input current to the power stages exceeds 73 A. Figure 5-4 illustrates the assertion and de-assertion of PSYS_CRIT#, implemented in the TPS536C9T VR14 controller using TPS25990 as the PSYS monitor.

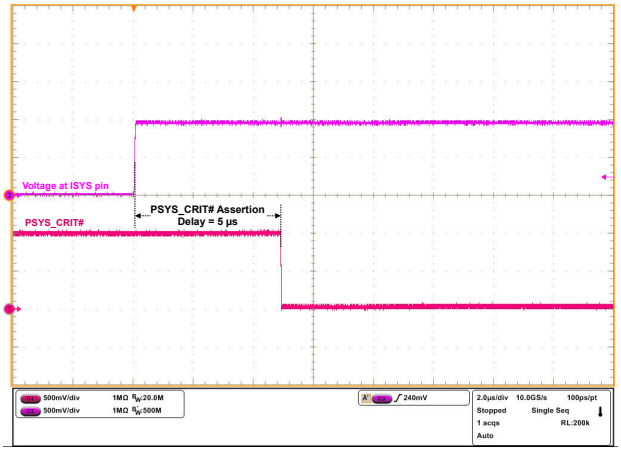

Figure 5-3. PSYS_CRIT# Assertion Delay in the TPS536C9T Controller

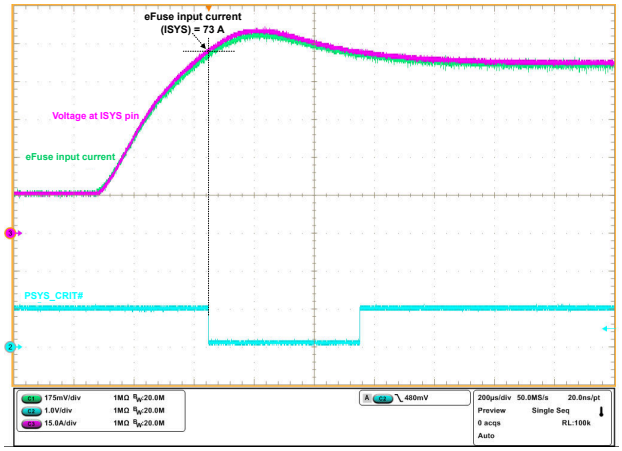

Figure 5-4. Assertion of the PSYS_CRIT# TPS536C9T Controller Using TPS25990 as the PSYS monitor

6 Extraction of Platform Current Information With Multiple PSYS Monitors Connected to the Same PSU

With the gradual increase in processor power consumption, the server power distribution boards (PDB) house multiple VR controllers and power stages to feed power into several CPUs. Each VR module is attached to the individual CPUs. In this architecture, only one VR14 controller attached to a CPU, suppose the CPU-1, is the recipient of PSYS data and associated connections to implement PSYS functionality as shown in Figure 6-1. All other VR14 controllers attached to the CPUs other than CPU-1 do not require PSYS functionality to be implemented. Only one VR14 per board requires PSYS considerations. This helps in moving from power monitoring at the individual CPU VR controller level to total platform power or current monitoring. The outputs of all the PSYS monitors need to be summed together to get the total platform input current.

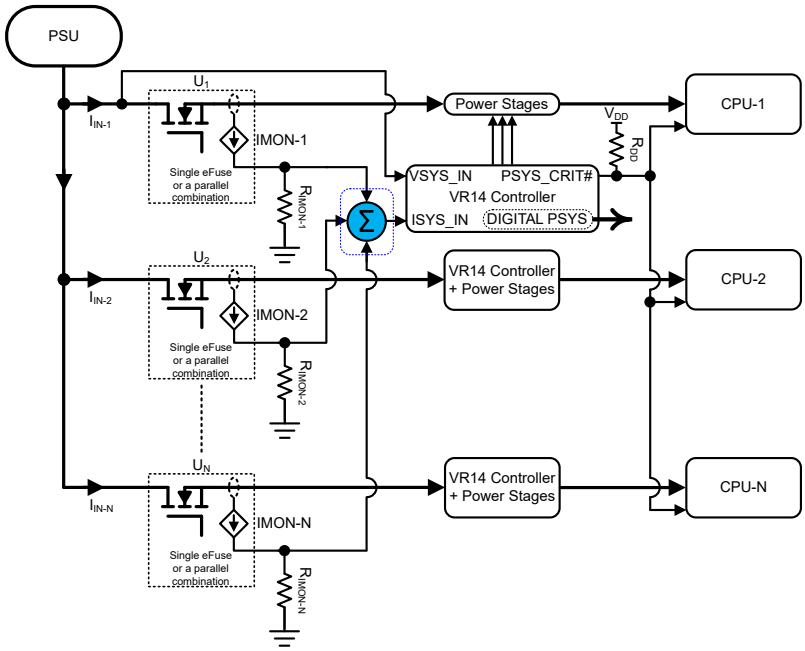

Figure 6-1. Protecting Individual VR Controller Power Paths Separately by Incorporating Multiple eFuse Modules Connected to the Same PSU

Multiple eFuse modules (either a single TPS25984, TPS25985 or TPS25990 eFuse or a parallel combination of TPS25990 and TPS25984/5 eFuses for higher current designs) are required to protect the different power paths (feeding to each VR14 modules) separately in a multiple CPU board. However, all these loads are fed by the same PSU. Therefore, it is essential to monitor the PSU current when implementing the PSYS functionality. These eFuse modules serve the purpose of multiple PSYS monitors connected to the input power supply of the platform. In this architecture, the current monitoring outputs from all these PSYS monitors need to be aggregated to determine the global platform power. However as discussed in Section 4, the IMON pin of the TPS25984, TPS25985 or TPS25990 eFuses serves two purposes: 1) setting up the over-current and scalable fast-trip thresholds; 2) monitoring the current flowing through it. Hence, the IMON outputs of the multiple eFuse modules cannot be directly tied together to get the total platform current. Otherwise, that might interfere with the over-current and short-circuit thresholds of the individual eFuses modules. The solution is here to use a non-inverting summing amplifier to sum up all the IMON voltage outputs (V_{IMON} = I_{IN} x G_{IMON} x R_{IMON}) from the individual eFuse modules.

6.1 Designing the Non-Inverting Summing Amplifier

A high bandwidth (>= 50 MHz) and low offset (<= 100 µV) precision op amp, for example, TLV365, is selected here to implement the non-inverting summing amplifier as shown in Figure 6-2.

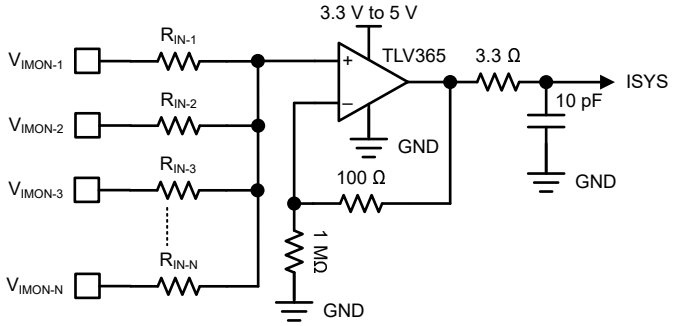

Figure 6-2. Non-Inverting Summing Amplifier to Aggregate the IMON Voltage Outputs From the Individual eFuse Modules

V_{IMON-1}, V_{IMON-2}, V_{IMON-3}, ... , and V_{IMON-N} are the IMON voltage outputs from the individual eFuse modules as defined in Equation 8.

$$V_{IMON-1}(V) = I_{IN-1}(A) \times R_{IMON-1}(\Omega) \times G_{IMON}(\mu A/A)$$
$$V_{IMON-2}(V) = I_{IN-2}(A) \times R_{IMON-2}(\Omega) \times G_{IMON}(\mu A/A)$$
$$V_{IMON-3}(V) = I_{IN-3}(A) \times R_{IMON-3}(\Omega) \times G_{IMON}(\mu A/A)$$
$$V_{IMON-N}(V) = I_{IN-N}(A) \times R_{IMON-N}(\Omega) \times G_{IMON}(\mu A/A) \quad (8)$$

N is the number of current monitoring outputs, summed up using the summing amplifier. The voltage output of the summing amplifier in Figure 6-2 is described in Equation 9.

$$V_{ISYS}(V) = \Sigma_{n=1}^{N}[V_{IMON-n}(V) \times m_n] \quad (9)$$

m_1, m_2, m_3, ... , and m_N are the different mathematical functions (f_1, f_2, f_3, ... , and f_N respectively) of R_{IN-1}, R_{IN-2}, R_{IN-3}, ... , and R_{IN-N} in Figure 6-2 as depicted in Equation 10.

$$m_{1,2,3,...,N} = f_{1,2,3,...,N}(R_{IN-1}, R_{IN-2}, R_{IN-3}, ..., R_{IN-N}) \quad (10)$$

m_1, m_2, m_3, ... , and m_N need to be selected in such a way that Equation 11 is satisfied.

$$m_1 \times R_{IMON-1} = m_2 \times R_{IMON-2} = m_3 \times R_{IMON-3} = ... = m_N \times R_{IMON-N} \quad (11)$$

Equation 11 simplifies Equation 9 to Equation 12.

$$V_{ISYS}(V) = m_1 \times R_{IMON-1}(\Omega) \times G_{IMON}(\mu A/A) \sum_{n=1}^{N} I_{IN-n}(A) \quad (12)$$

ISYS_IN_GAIN, which needs to be programmed in the VR14 controller firmware to get the total platform current from the voltage at the ISYS pin, is obtained using Equation 13 in this architecture.

$$ISYS\_IN\_GAIN = \frac{1}{m_1 \times R_{IMON-1} \times G_{IMON}} \quad (13)$$

The procedure to compute m_1, m_2, m_3, ... , and m_N are discussed in Section 6.2.

6.2 Design Guideline and Example

1. Find out the full-scale range of ISYS_IN pin in the VR14 controller.
2. Set the V_{IREF} of all the eFuse modules (U_1, U_2, U_3, ... , and U_N) (either a single TPS25984, TPS25985 or TPS25990 eFuse or a parallel combination of TPS25990 and TPS25984/5 eFuses for higher current designs) to half of the maximum voltage range of the ISYS_IN input of the VR14 controller. This provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the scalable fast-trip threshold (2 × I_{OCP}).

Note

The value of V_{IREF} must be same for U_1, U_2, U_3, ... , and U_N.

3. Select the required circuit-breaker thresholds during steady-state (I_{OCP-1}, I_{OCP-2}, I_{OCP-3}, ... , and I_{OCP-N}) for all the eFuse modules. TI recommends selecting the circuit-breaker thresholds during steady-state as 1.1 to 1.2 times the maximum steady-state current or the thermal design current (TDC).
4. Calculate the value of R_{IMON} resistors (R_{IMON-1}, R_{IMON-2}, R_{IMON-3}, ... , and R_{IMON-N}) for all the eFuse modules using Equation 3 to set the desired over-current protection or circuit-breaker threshold as selected in the above step.
5. Let assume a constant positive number, k_1 for the eFuse module-1 (U_1). The corresponding factors, k_2, k_3, ... , and k_N for the eFuse module-2, 3, ... , and N (U_2, U_3, ... , and U_N) are defined as Equation 14.

$$k_2 = k_1 \frac{R_{IMON-1}}{R_{IMON-2}},\ k_3 = k_1 \frac{R_{IMON-1}}{R_{IMON-3}},\ \dots \text{, and } k_N = k_1 \frac{R_{IMON-1}}{R_{IMON-N}} \quad (14)$$

6. Let consider the value of R_{IN-1} in Figure 6-2 as 50 kΩ. The values of the R_{IN-2}, R_{IN-3}, ... , and R_{IN-N} in Figure 6-2 need to be calculated using Equation 15.

$$R_{IN-2} = R_{IN-1} \frac{R_{IMON-2}}{R_{IMON-1}},\ R_{IN-3} = R_{IN-1} \frac{R_{IMON-3}}{R_{IMON-1}},\ \dots \text{, and } R_{IN-N} = R_{IN-1} \frac{R_{IMON-N}}{R_{IMON-1}} \quad (15)$$

Note

- Choose the value of R_{IN-1} in such a way that the values of R_{IN-2}, R_{IN-3}, ... , and R_{IN-N} including R_{IN-1} are in the range of 20 kΩ - 500 kΩ to maintain stability and adequate slew-rate of the operation amplifier.
- The selected values of R_{IN-1}, R_{IN-2}, R_{IN-3}, ... , R_{IN-N}, R_{IMON-1}, R_{IMON-2}, R_{IMON-3}, ... , and R_{IMON-N} must be as close as possible to the calculated ones to get better accuracy. These resistances must have a tolerance of less than 0.1% and a power rating of more than 100 mW. For noise immunity, place a 22 pF ceramic capacitor from the IMON pin to GND in each eFuse module.

7. The values of m_1, m_2, m_3, ... , m_N in Equation 11 can be obtained using Equation 16.

$$m_1 = k_1 / \sum_{n=1}^{N} k_n,\ m_2 = k_2 / \sum_{n=1}^{N} k_n,\ m_3 = k_3 / \sum_{n=1}^{N} k_n,\ \dots \text{, and } m_N = k_N / \sum_{n=1}^{N} k_n \quad (16)$$

8. Finally, select the internal scaling factor ISYS_IN_GAIN (set through the SVID_CONFIG) according to Equation 13.

A non-inverting summing amplifier design example is presented in Figure 6-3. The IMON outputs from six (6) eFuse modules or PSYS monitors are added together to retrieve the total system current, drawn from the PSU.

	Step-1 & 2	Step-3		Step-4	Step-5	Step-6	Step-7
eFuse Module (U_n)	V_{IREF} (V)	$I_{OUT(max)-n}$ (A)	I_{OCP-n} (A)	R_{IMON-n} (Ω)	k_n	R_{IN-n} (kΩ)	m_n
U_1	0.9	200	220	225	1.00	50.0	0.17
U_2	0.9	140	161	307	0.73	68.3	0.12
U_3	0.9	50	57	868	0.26	193.0	0.04
U_4	0.9	190	224	221	1.02	49.1	0.17
U_5	0.9	250	283	175	1.28	38.9	0.21
U_6	0.9	320	381	130	1.73	28.9	0.29
ISYS_IN_GAIN (A/V)				***1472.8***			

Step-8

Figure 6-3. Non-Inverting Summing Amplifier Design Example

7 Summary

This application note outlines the implementation of the PSYS monitor using either a single TPS25984, TPS25985 or TPS25990 eFuse or a parallel combination of TPS25990 and TPS25984/5 eFuses in higher current designs for incorporating the PSYS and PSYS_CRIT# functionalities in a VR14 controller powering CPUs or GPUs. TPS25984, TPS25985 or TPS25990 eFuses serve both the purposes of providing smart input power path protection features as well as accurate and high-bandwidth input current monitoring. This makes TPS25984, TPS25985 or TPS25990 eFuses well-designed for the PSYS monitors as per the requirements specified in the Intel® VR14 specifications. The system designers do not need to add any more extra active components for implementing the PSYS monitors.

8 References

- Texas Instruments, *TPS25984: 4.5-V to 16-V, 0.8-mΩ, 70-A stackable eFuse with accurate and fast current monitor* data sheet.
- Texas Instruments, *TPS25985: 4.5-V to 16-V, 0.59-mΩ, 80-A Stackable Compact eFuse with Accurate and Fast Current Monitor* data sheet.
- Texas Instruments, *TPS25990: 2.9-V to 16-V, 0.79-mΩ, 60-A eFuse With Digital Telemetry Controller* data sheet.
- Texas Instruments, *TLV365: 50-MHz Single-Supply Operational Amplifier With Rail-to-Rail Input and Output* data sheet.

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