*Application Brief*

# *Combined PLC Digital Input or Output Design*

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## Introduction

Digital input and digital output modules are the most common types of PLC modules. In some applications, the flexibility of configuring the channel to be either input or output is required. In DCS systems for example, the configuration can be done after wiring and sensor installation. Also, in high availability systems, few redundant channels can be used for many channels, and hence are required to be configured to one type when that channel type fails.

This application brief shares how to build an 8-channel configurable Digital Input/output (DIO) module using standard High Side Switch (HSS) output and standard digital input devices.

The module can be configured as digital input (DI) or digital output (DO) per channel independently. All channels are designed to withstand ESD, EFT, and surge events according to IEC6100-4-2 standard. The 8-ch DIO module works with 12V approximately 36V field supply.

The 8 DI channels can be configured as IEC 61131-2 Type 1 or 3 sinking digital inputs with inputs up to a 36V. There are two groups of input channels: the DI channels CH3, CH5, CH6, and CH7 can be individually disabled when DO is enabled. The DI channels CH1, CH2, CH4, and CH8 are always on even when the DO is enabled, those channels demonstrate how to use DIN for diagnostics of the DO path.

The DO channels are high-side. Both DI and DO are isolated from controller side.

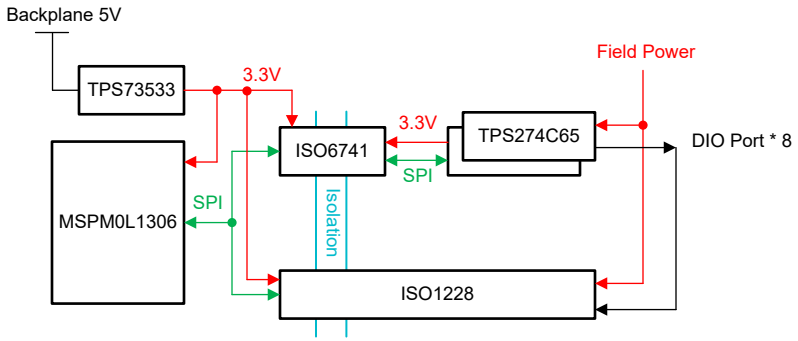


**Figure 1. Block Diagram**

The design block diagram shows how the DIO function is constructed. 8-ch DIO design uses MSPM0L1306 as a controller. ISO1228 for implementing DI and the isolation, TPS274C65 for implementing DO, and ISO6741 for isolating for DO function. Controller side is powered by 3.3V generated from 5V backplane power. The field side is powered by field supply that can go up to 38.5V. The TPS274C65 integrated regulator convert field power to 3.3V to supply ISO6741 isolator field side power.

Both TPS274C65 and ISO1228 have SPI. One MSPM0L1306 SPI channel is used to control both devices.

## System Implementation and Consideration

### Software Description

As the SPI modes differ between DO and DI devices, special consideration is required while initializing both devices and switching between DI/DO modes. A simple DIO basic software flow chart as shown. In the beginning, it resets ISO1228 and read RC (read to clear) type registers of TPS274C65 to clear data. For example, VDD_UVLO can be marked fault when power on, TPS274C65 default to latch fault bits and cleared only on read. So we read to clear the register at beginning, monitor faults occurrence when operating afterwords.

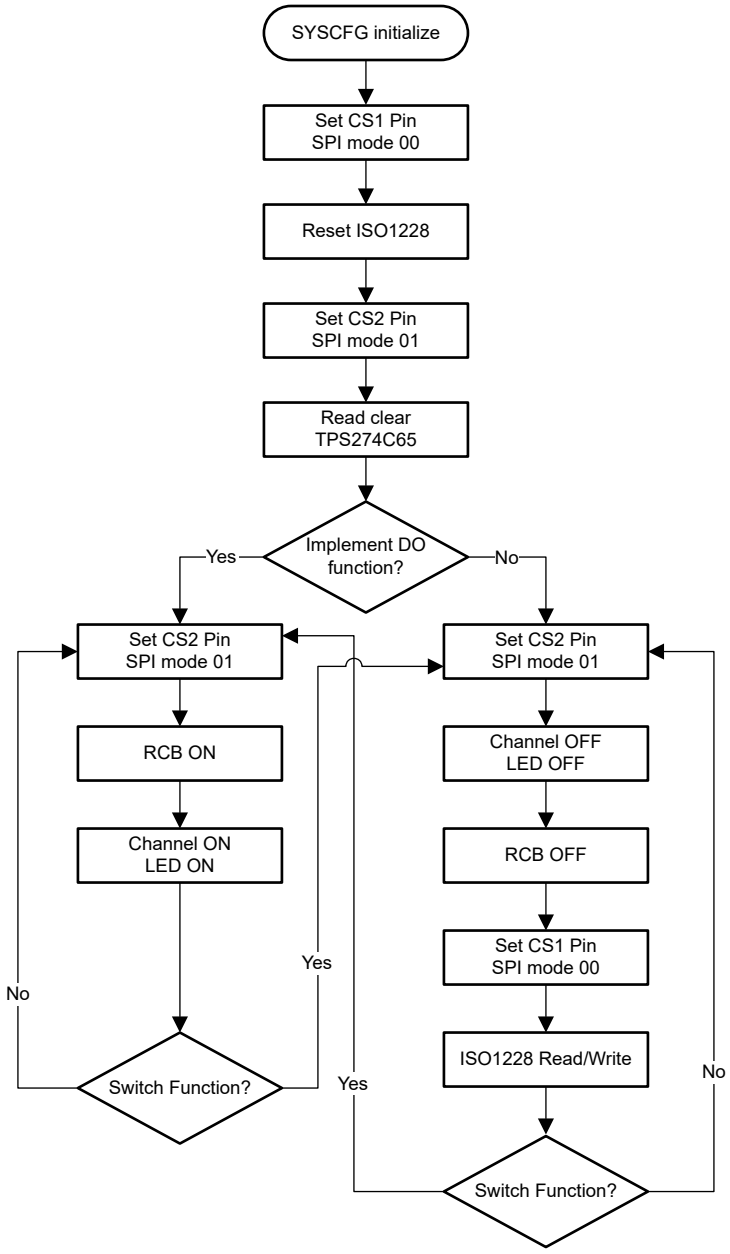


**Figure 2. Software Flow Chart**

### SPI Hardware Configuration

One controller M0 uses SPI to communicate with one ISO1228 and two TPS274C65 devices. ISO6741 device has three forward and one reverse-direction channels. SCLK SDI CS0 signal from M0 connect are connected to the three forward channels. SDO from TPS274C65 connect to the reverse-direction channel.

M0 connects directly to ISO6741 and ISO1228, for example, two devices to one controller. The SPI multiple peripherals configuration uses a separate CS signal for each device.

The controller M0 requires that only one CS is asserted when transmitting even if data for the other device is invalid. SDO can in high impedance when CS is cleared. Otherwise, SDO can be driven simultaneously by the two devices resulting in data corruption.

As the isolator drives the SPI signals, the chip select signal of ISO1228 (CS2) need to be connected to ISO6741 EN1 pin. This set OUTD of ISO6741 to high impedance when ISO1228 is transmitting. OUTD is for transmitting SDO signal of TPS274C65 to M0. ISO6741 OUTD is in high-Z state when EN1 is low. ISO1228 transmit SDO signal when CS2 pin is asserted.

For the DO side, SPI lines are connected to a pair of TPS274C65 through ISO6741. TPS274C65 can support addressable SPI configuration and Daisy chain configuration.

### SPI Mode Configuration

The SPI clock polarity and phase need to be adjusted individually for TPS274C65 and ISO1228 devices. One can adjust the microcontroller SPI peripheral clock polarity and clock phase, which are set by CTL0.SPO bit and CTL0.SPH bit.

Clock polarity (CTL0.SPO) is used to control the clock polarity when data is not being transferred and is only used in the Motorola SPI frame mode.

Value (0x0h) means controller produces a steady state LOW value on the CLKOUT pin when data is not being transferred, while value (0x1h) means controller produces a steady state HIGH value on the CLKOUT pin when data is not being transferred.

Clock phase (CTL0.SPH) bit selects the clock edge that captures data. This has the most impact on the first bit transmitted by either permitting or not permitting a clock transition before the first data capture edge. Please refer to Motorola SPI frame mode section to check the diagrams.

Value (0x0h) means data is captured on the first clock edge transition, while value (0x1h) means data is captured on the second clock edge transition.

For TPS274C65 clock signal needs to be low when data is not being transferred. The data is captured on the second clock edge. Thus, when controlling the TPS274C65, M0 need to set clock polarity (CTL0.SPO) bit to 0x0h, and set clock phase (CTL0.SPH) bit to 0x1h.

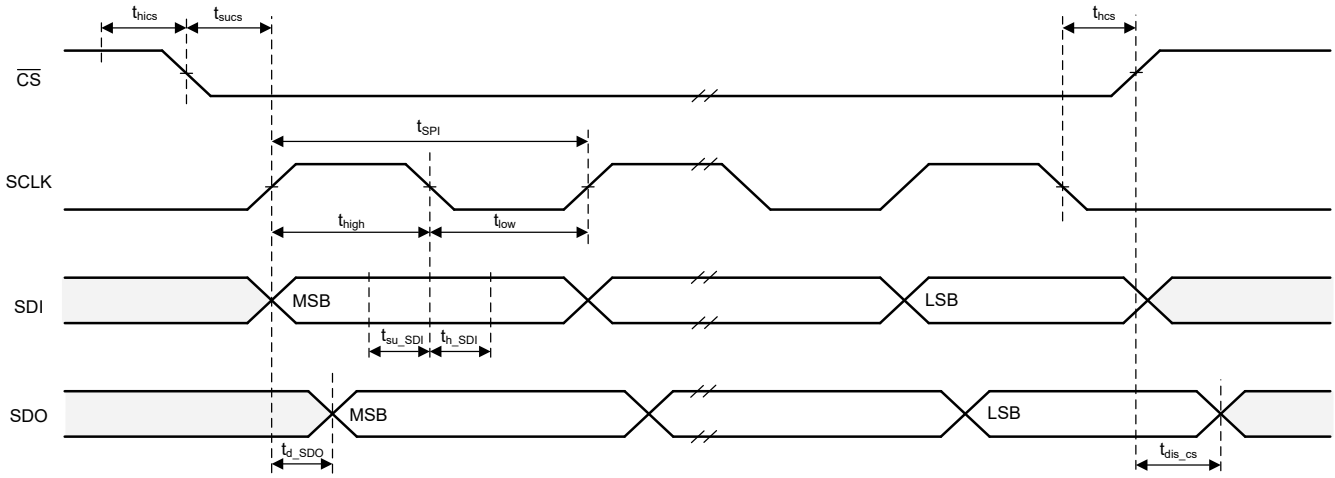


**Figure 3. SPI Timing of TPS274C65**

For ISO1228 clock signal also needs to be low when data is not being transferred. The data is captured on the first clock edge. Thus, when controlling the ISO1228, controller need to set clock polarity (CTL0.SPO) bit to 0x0h, and set clock phase (CTL0.SPH) bit to 0x0h.

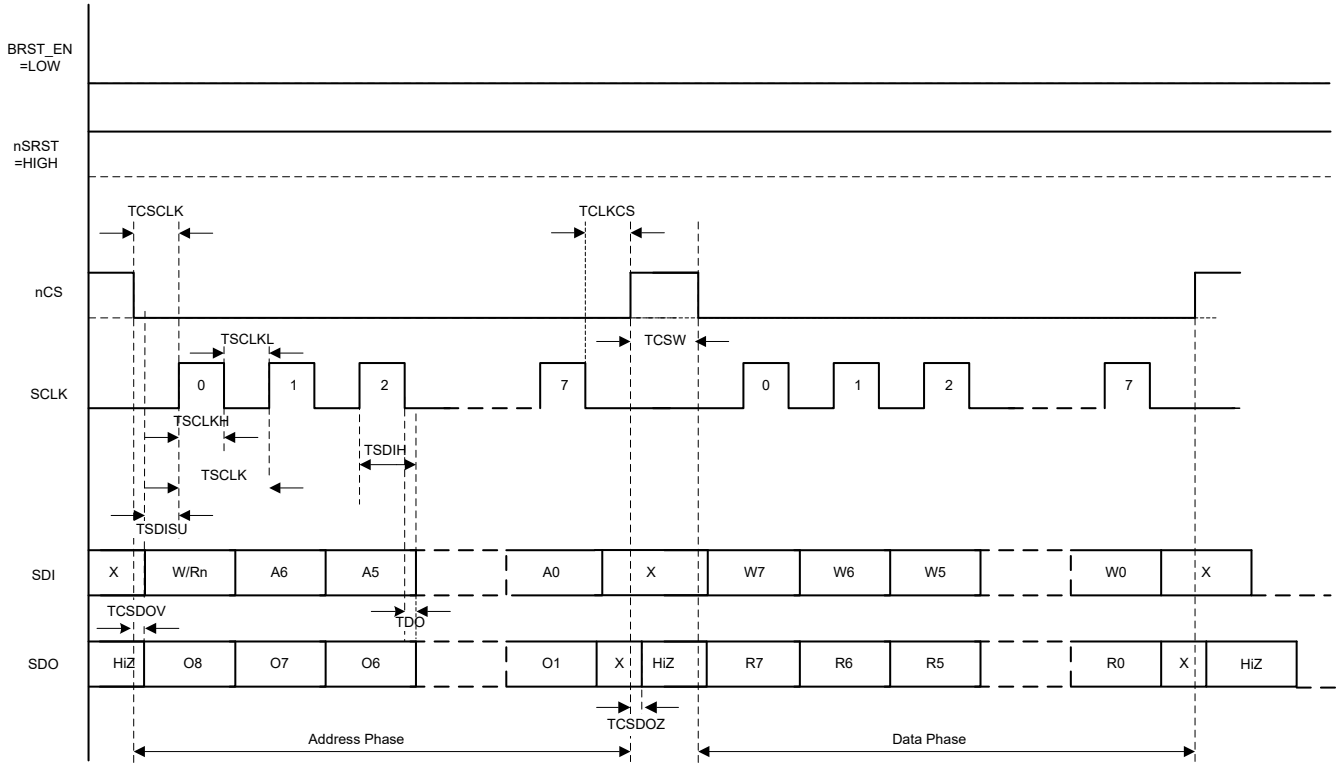


**Figure 4. SPI Timing of ISO1228**

As SPI modes of ISO1228 and TPS274C65 are different. SPI mode switching is needed when controlling the 2 devices. When the SPI configuration is set, the ENABLE bit in SPIx.PWREN register can be cleared to avoid unpredictable behavior during the updates or for the first data receive or transmitted afterward.

### Power Configuration

The digital supply of TPS274C65 is generated using the integrated regulator off the field supply. To enable integrated regulator, REG_EN pin is left floating.

If external DC/DC is used to achieve lower power dissipation, tie REG_EN to GND to disable internal regulator, power the external regulator from the same VS supply of TPS274C65.

TPS274C65 Vs must be powered before VDD. If VS is connected to ground while VDD is powered then substantial current can flow from VDD to VS and damage the internal protection diodes. If VS is floating while VDD is powered. Large current can flow to VOUT also damaging the protection diodes.

### Leakage Current of DO

The DO current path is from VS through TPS274C65 then to the external FET to DIO port to the load. Having the sink DI connected to the same output terminals can result in some leakage into DI.

For CH3, CH5, CH6, CH7, some current can leak through RTHR to ISO1228 input channel. For CH1, CH2, CH4, CH8 another current can leak through RTHR, RPAR, LED to ground. Because of 2 different configurations between the two groups of channels, the leakage current has 2 different paths. Leakage current test point between DIO port and RTHR.

CH3, CH5, CH6, CH7 as shown in Figure. Leakage current related to voltage on channel input as well as the load.

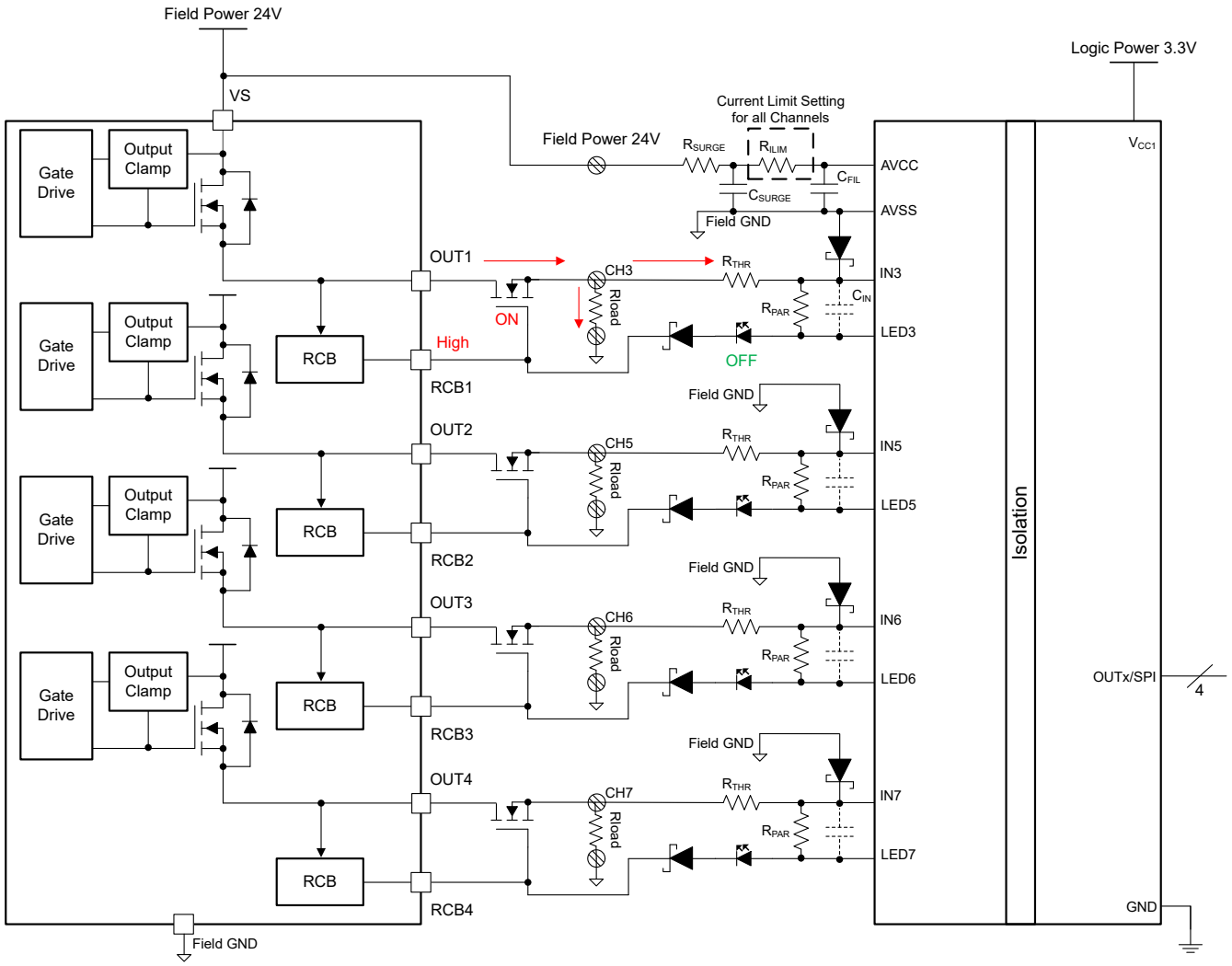


**Figure 5. Leakage Current of CH3, CH5, CH6, CH7**

The worst case is when CH3, CH5, CH6, CH7 are all at DO ON state and loaded with 50Ω resistance. Leakage current on one channel is 0.549mA. Total leakage current on this group is:

4×0.549 = 2.196mA

If 3 channels (CH5, CH6, CH7 in this example) at DO OFF state, and only CH3 at DO ON state and loaded with 50Ω resistance. Leakage current on CH3 is 1.049mA. Leakage current on CH5 or CH6 or CH7 is 0.004mA. Total leakage current on this group is:

1.049+0.004×3 = 1.061mA

More test results are shown in Table 1. A lighter load can reduce leakage current. The more channel at DO ON state, the less leakage current per channel, but the more total leakage current. Negative value means current source from DI, this is due to ISO1228 internal circuit connected to INx pin including wire break detection circuit. The wire break detection circuit tries to detect an input current of 245μA (specified as IWB in data sheet), if the input current is <245μA then the break detection circuit reports as a wire break. Current >245μA indicates no wire break.

**Table 1. Leakage Current Test Result on CH3, CH5, CH6, CH7**

| Load on CH3(Ω) | CH3 | CH5 | CH6 | CH7 | Leakage current on CH3 (mA) | Total Leakage current (mA) |
|---|---|---|---|---|---|---|
| 50 | ON | ON | ON | ON | 0.549 | 2.296 |
| 50 | ON | OFF | ON | ON | 0.633 | 1.903 |
| 50 | ON | OFF | OFF | ON | 0.770 | 1.548 |
| 50 | ON | OFF | OFF | OFF | 1.049 | 1.061 |
| 50 | OFF | OFF | OFF | OFF | -0.006 | 0.012 |
| float | ON | ON | ON | ON | 0.574 | 2.296 |
| float | ON | OFF | ON | ON | 0.658 | 1.978 |
| float | ON | OFF | OFF | ON | 0.795 | 1.598 |
| float | ON | OFF | OFF | OFF | 1.069 | 1.081 |
| float | OFF | OFF | OFF | OFF | 0.004 | 0.016 |

CH1, CH2, CH4, CH8 as show in Figure 6. Leakage current not relate to other channels' state. Test results shown in Table 2.

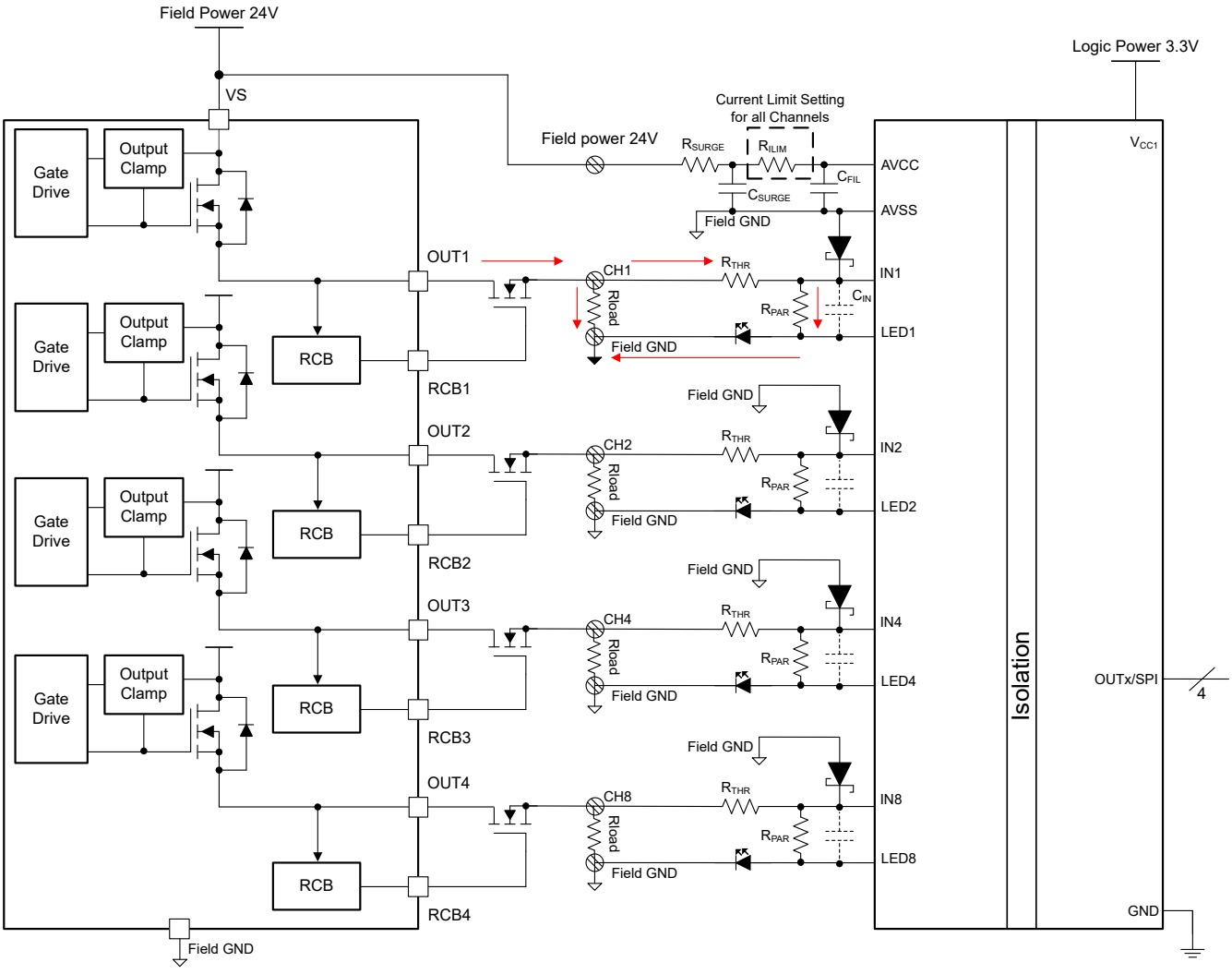


**Figure 6. Leakage Current of CH1, CH2, CH4, CH8**

**Table 2. Leakage Current Test Result on CH1, CH2, CH4, CH8**

| Load (Ω) | Current leak to CH1 (mA) | Current leak to CH2 (mA) | Current leak to CH4 (mA) | Current leak to CH8 (mA) |
|---|---|---|---|---|
| 50 | 2.670 | 2.703 | 2.644 | 2.667 |
| float | 2.667 | 2.700 | 2.640 | 2.663 |

When implement DI, there's nearly no current leak to TPS274C65 due to external FET in OFF state.

### Reference


- Texas Instruments, *TPS274C65xS 72mΩ, Quad-Channel Smart High-Side Switch With SPI Interface and Diagnostics,* data sheet.
- Texas Instruments, *ISO1228 Eight-Channel Isolated Digital Input with Current Limit and Diagnostics,* data sheet.
- Texas Instruments, *ISO674x General-Purpose Reinforced Quad-Channel Digital Isolators with Robust EMC,* data sheet.
- Texas Instruments, *MSPM0L130x Mixed-Signal Microcontrollers,* data sheet.
- Texas Instruments, *MSPM0 L-Series 32-MHz Microcontrollers,* technical reference manual.


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