HIGH VOLTAGE SEMINAR

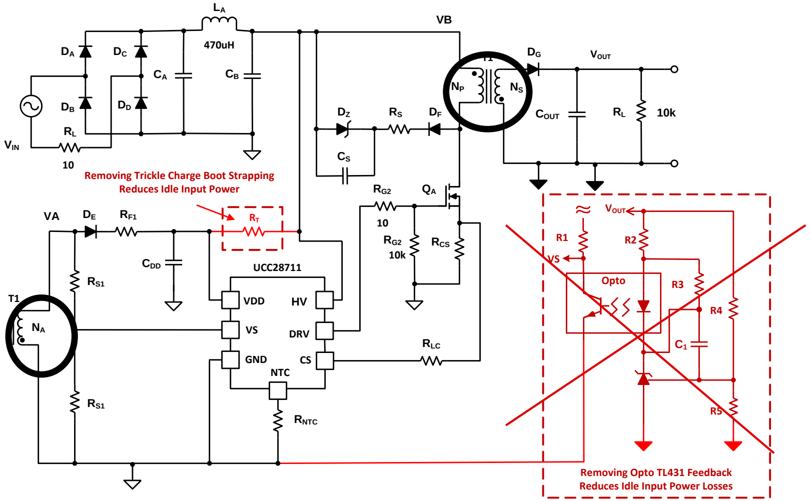
MIKE O'LOUGHLIN
HIGH VOLTAGE CONTROLLERS

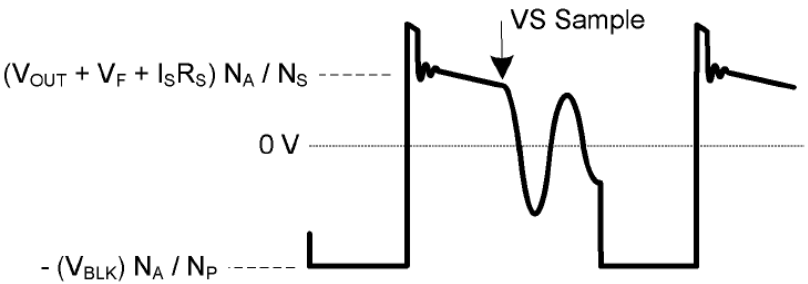
ACHIEVING HIGH POWER DENSITY AND ULTRA LOW STANDBY POWER IN FLYBACK CONVERTERS

Agenda

- Basic PSR flyback operation/problems and issues
- Wake-up monitoring (UCC24650) with PSR sampling initiation (UCC28730)
  - Speeds up transient response
  - Greatly reduces output capacitance ($\approx C_{OUT}/7$)
  - Can meet zero power (< 5 mw)
- Device feature set
- Design tips and tricks
- Questions

Typical Primary Side Regulation (PSR)

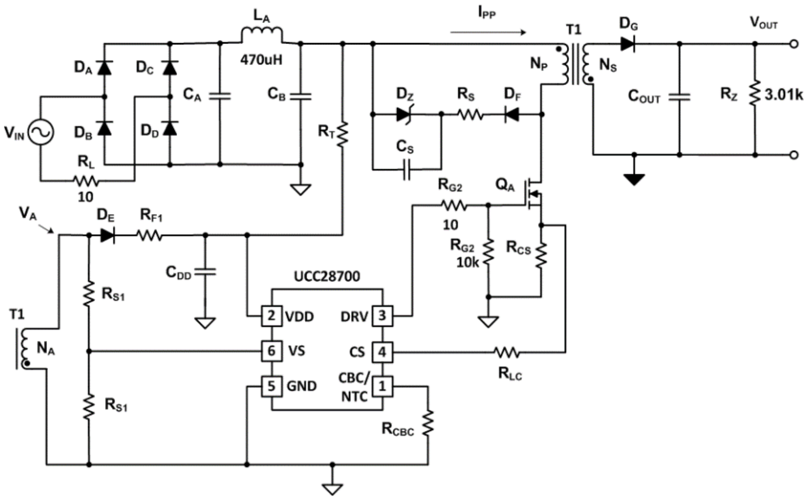




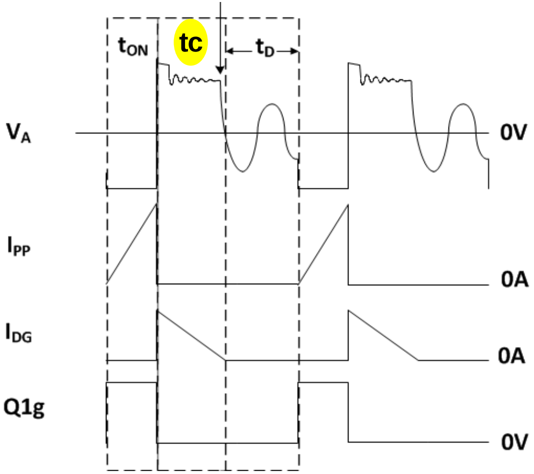
- Uses N_A/N_S Turns ratio to sample V_{OUT}
  - ✓Control Reflected Output Voltage (V_{OUT})
    - Sampled during rectifier diode conduction @ Knee
    - Removes the need of TL431 feedback
      - Saves $$$$ and reduces standby power

Uses FM, AM (I_{PP}), FM modulation to control duty cycle

- Controller Samples Auxiliary Winding (V_A) to Adjust Duty cycle
  - While Energy is being delivered to secondary (tc) when D_G is conducting
- Frequency Typically Varies from1 kHz to 100 kHz



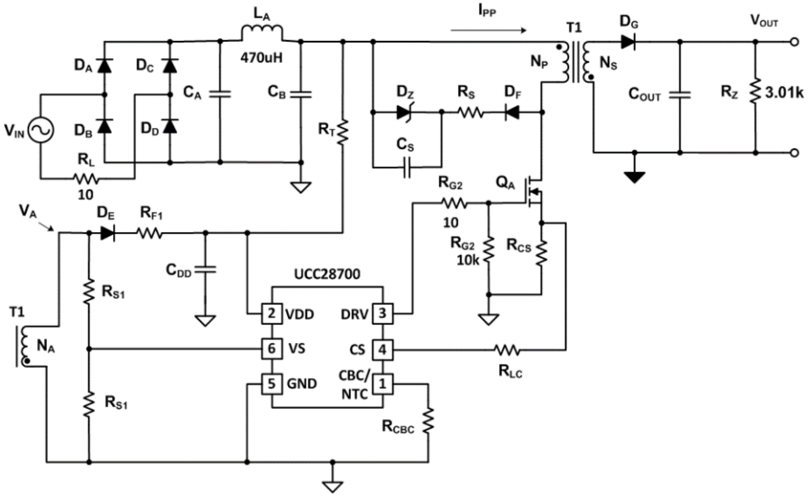
Feedback Sampling and t_D Adjustment



$$D = \frac{t_{ON}}{t_{ON} + t_C + t_D}$$

Negative side of PSR regulation

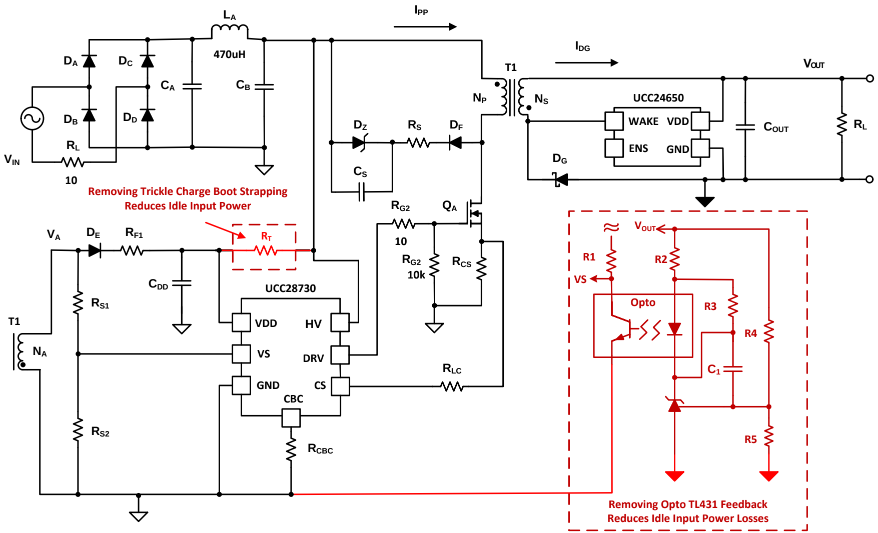
- This control scheme has a slow transient response
- When the Converter is Idle at f_{min} = 1kHz
  - ✓Output is sampled and the Duty cycle is adjusted once every 1 ms.
  - ✓The output capacitor (C_{OUT1})must be sized to handle load transients



$$C_{OUT1} \geq \frac{I_{MAX}}{dV \times f_{min}}$$

Improving the load transient response with the UCC28730

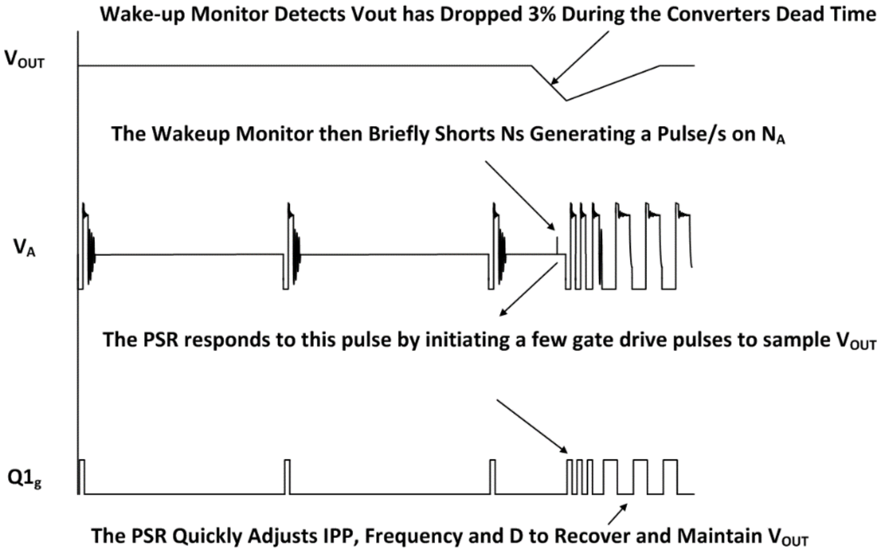
- Wake-up monitoring (UCC24650) with PSR sampling initiation (UCC28730) for fast transient response.
  - UCC28730 PSR with output sampling initiation
    - Has all the features of traditional PSR controller
    - Can operate down to 32 Hz to meet < 5 mW Standby power
  - UCC24650 Secondary side wake-up monitoring
    - Monitors V_{OUT} and will activate PSR sampling if V_{OUT} drops out of regulation.



UCC24650 performance advantage

- UCC24650 Monitors V_{OUT}
  - If $V_{OUT} < 0.97xV_{OUT1}$
    - The secondary winding is shorted
      - 1us every 30 us with a current-limited switch

- UCC28730
  - Monitors the auxiliary winding (VA) during the deadtime
    - If a + pulse is observed
      - It Triggers PSR Sampling
        - » Gate drive initiates a few sample pulses
          - » V_{OUT} is sampled
          - » The controller quickly responds
            - » Adjusts I_{PP}, frequency and Duty cycle
            - » Recovers and Maintains V_{OUT}



Faster transient response with wake-up

- Reduces the amount of C_{OUT}
- C_{OUT} needs to be sized for
  - Output transients (dV) and the V loop for stability

- $C_{OUT\_No\_Wakeup} \geq \frac{100 \times I_{MAX}}{V_{OUT} \times f_{max}}$
- $C_{OUT} \geq \frac{I_{MAX}}{dV \times \frac{f_{max}}{10}}$

How much is C_{OUT} reduced with wake-up?

- Typical design
  - f_{min} = 1 kHz
  - f_{max} = 80 kHz
- Using a design with Wake-up
  - C_{OUT} is reduce by a factor of 6.5
  - Output C with Wake-up (C_{OUT2})
  - Output C without Wake-up (C_{OUT1})

- $C_{OUT1} \geq \frac{I_{MAX}}{dV \times f_{min}}$
- $C_{OUT2} \geq \frac{I_{MAX}}{dV \times \frac{fmax}{10}}$
- $C_{OUT2} = 10 \times \frac{C_{OUT1} fmin}{fmax} = \frac{C_{OUT1}}{6.5}$

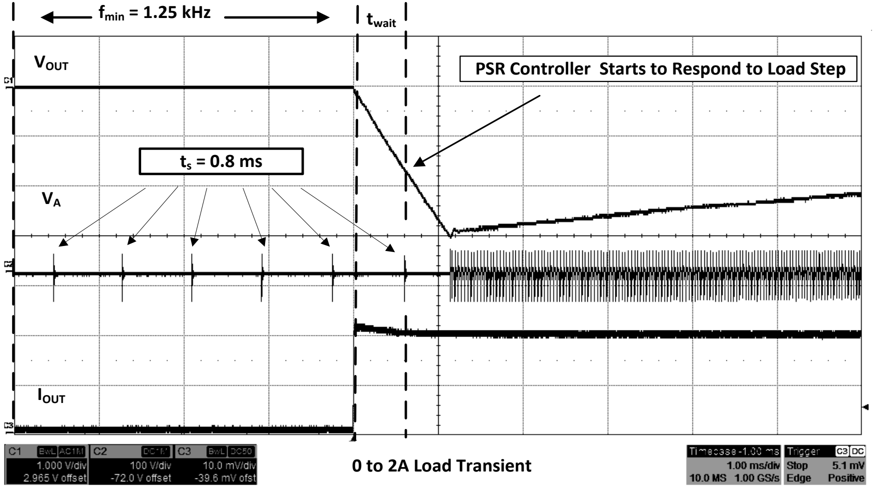
Reducing C_{OUT}

- Increases design's power density
- Reduces the cost of the design

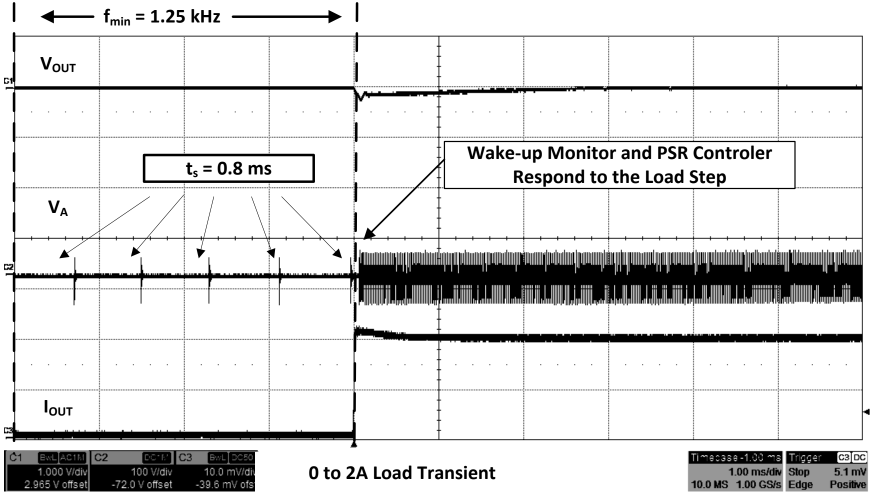
- $C_{OUT1} \geq \frac{I_{MAX}}{dV \times f_{min}}$
- $C_{OUT2} \geq \frac{I_{MAX}}{dV \times \frac{fmax}{10}}$
- $C_{OUT2} = 10 \times \frac{C_{OUT1} fmin}{fmax} = \frac{C_{OUT1}}{6.5}$

Transient response with and without wake-up

- 5 V/10 W Design was evaluated, f = 1.25 kHz to 80 kHz
- The design was tested with a full load transient step (0 to 2A)
- Without wake-up, controller could not sample (t_{wait}) V_{OUT} for 600us, V_{OUT} drooped 3V ☹
  - t_{wait} could have been as long 800 us
- With wake-up, controller responded quickly no waiting, V_{OUT} only drooped 0.4v ☺



0 to 2A Load Transient



0 to 2A Load Transient

UCC24650 200-V wake-up monitor for fast transient PSR

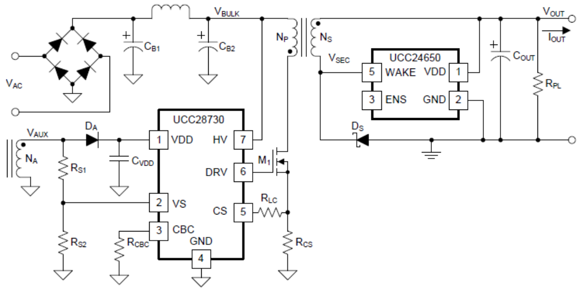
1 Features

- Enables Excellent Load Transient Performance and Zero Standby Power
- Enables Smallest Output Capacitor for Tight ΔV_{OUT}
- No External Components Required
- <50 µA Device Current Consumption (Typical)
- 5-V to 28-V Output Monitoring Capability
- 3% Voltage Droop Detection (Patent Pending)
- 200-V Wake-Up Switch
- Enables and Disables SR Controller, Relay Control, or Other Secondary Circuits
- SOT-23 5-Pin Package

2 Applications

- <5-mW *Zero-Power* Standby Applications
- Adapters and Chargers for Consumer Electronics
  - Smart Phones, Tablets, Set-Top Box
- TV and Monitor Power Supplies
- Home Appliance SMPS
  - Refrigerator, Washing Machine, Air Conditioners
- Industrial Power Supplies for Lighting and Home Automation

Simplified Application Schematic



Note: No opto feedback required

TEXAS INSTRUMENTS

UCC28730 *zero-power* standby PSR flyback controller with CVCC and *wake-up* monitoring

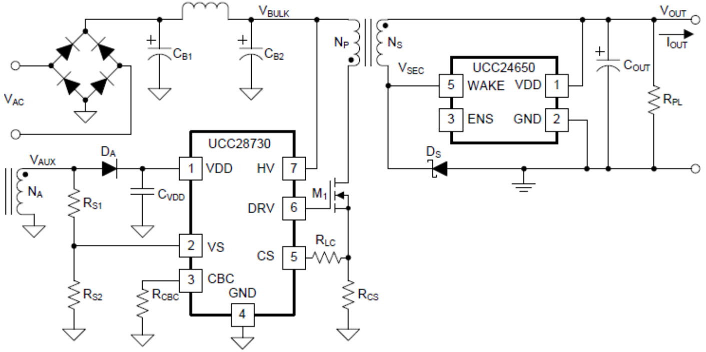
1 Features

- Enables *Zero-Power* (<5 mW) Standby Consumption
- Smart *Wake-Up* Detection Enables Smallest Output Capacitance
- Primary-Side Regulation (PSR) Eliminates Opto-coupler
- ±5% Voltage Regulation and Current Regulation Across Line and Load
- 700-V Start-up Switch
- 83-kHz Maximum Switching Frequency Enables Low Stand-by Power Charger Designs
- Resonant-Ring Valley-Switching Operation for Highest Overall Efficiency
- Frequency-Dither to Ease EMI Compliance
- Clamped Gate-Drive Output for MOSFET
- Over-Voltage, Low-Line, and Over-Current Protection Functions
- Programmable Cable Compensation
- SOIC-7 Package

2 Applications

- Adapters and Chargers for Smart Phones, Tablets, and Other Consumer Electronics
- TV and Monitor Power Supplies
- SMPS for Home Appliances and Industrial Automation
- Standby and Auxiliary Power Supplies

Simplified Application Schematic

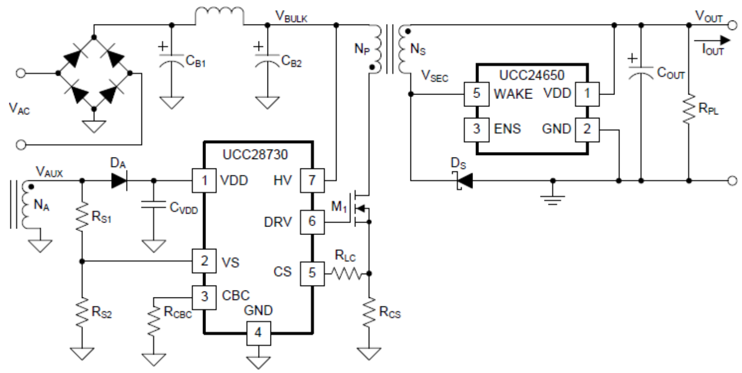


UCC28730 Protection/fault activation

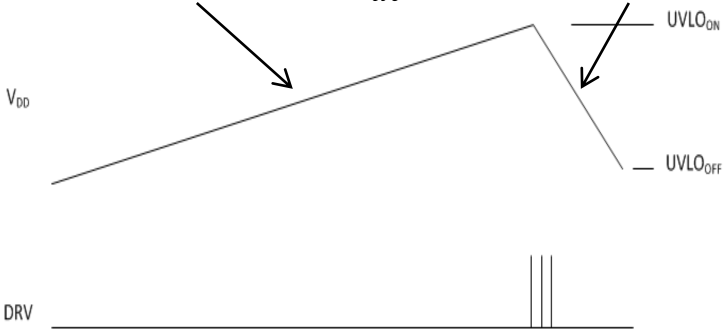
- Over Voltage Protection (OVP)
  - $(N_S/N_A)*(4.62V/R_{S2})*(R_{S1}+R_{S2})-V_D$
- Over Current Protection (I_{OCP}) V_{RCS} = 1.5V
  - $I_{OCP}=1.5V/R_{CS}$
    - Nominal Peak V_{RCS} = 0.74V
- Input Under Voltage Protection (UVLO)
  - $V_{IN} > (N_P/N_A)*(225uA*R_{S1})$ to startup
  - $V_{IN} < (N_P/N_A)*(80uA*R_{S1})$ to shutdown
- Thermal Shut Down (TSD = 165 C)
- All faults stop switching and reactivate soft start

Startup/fault

Simplified Application Schematic

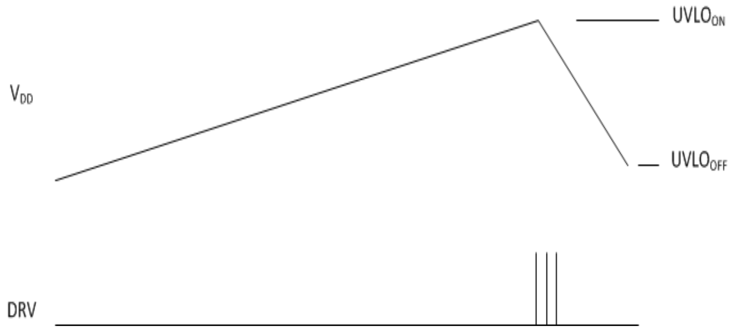


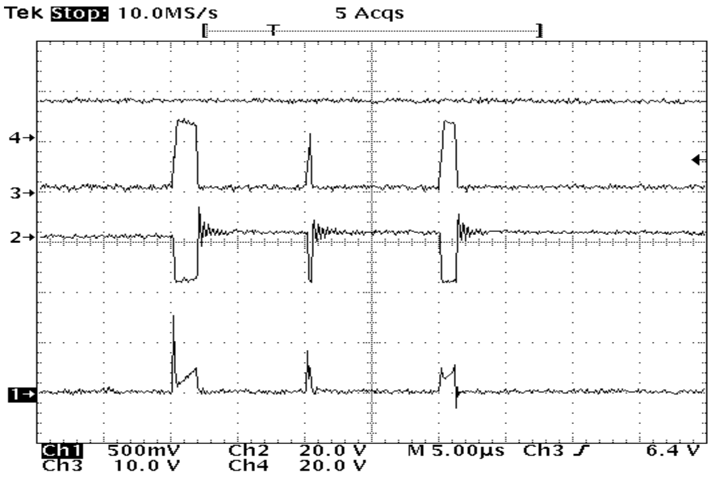
$$I_{HV} - I_{START} = C_{DD}\frac{dv_{DD}}{dt} \qquad I_{RUN} = C_{DD}\frac{dv_{DD}}{dt}$$



- ➢ VDD charged through HV Input:
  - 3 small gate driver pulses are initiated @ $UVLO_{ON}$
  - I_{PP} controlled to 1/3 max at startup
  - If fault is detected UVLO/soft start initiated
  - Will retry at $UVLO_{ON}$

Startup with input under voltage fault





- At UVLO$_{ON}$ three gate drive pulse are initiated:
  - CS peak is controlled to 1/3 max (245 mV)
  - Input UVLO detected UVLO restart is initiated

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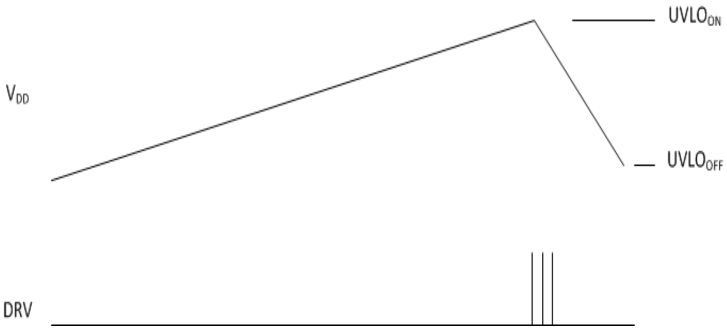
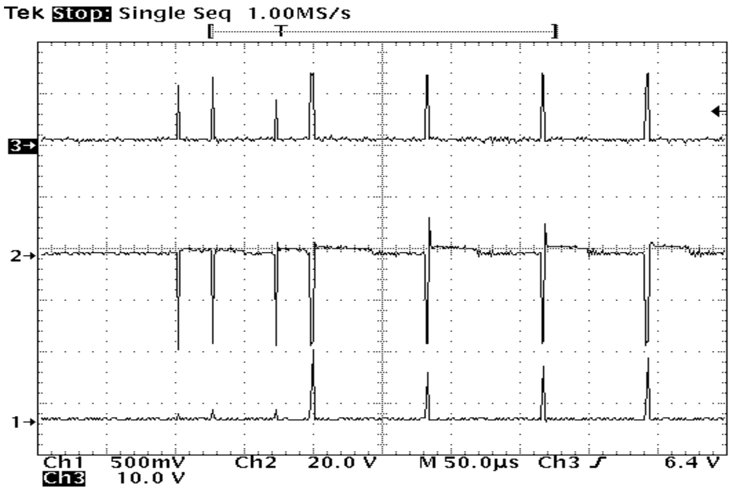
Startup with no faults





- At $UVLO_{ON}$ three gate drive pulse are initiated:
  - CS peak is controlled to 1/3 max (245 mV)
  - No Faults have been detected so supply starts switching
  - After 3rd initiated pulse I_{PP} is controlled to maximum threshold
    - (CS Controlled to 740mV)

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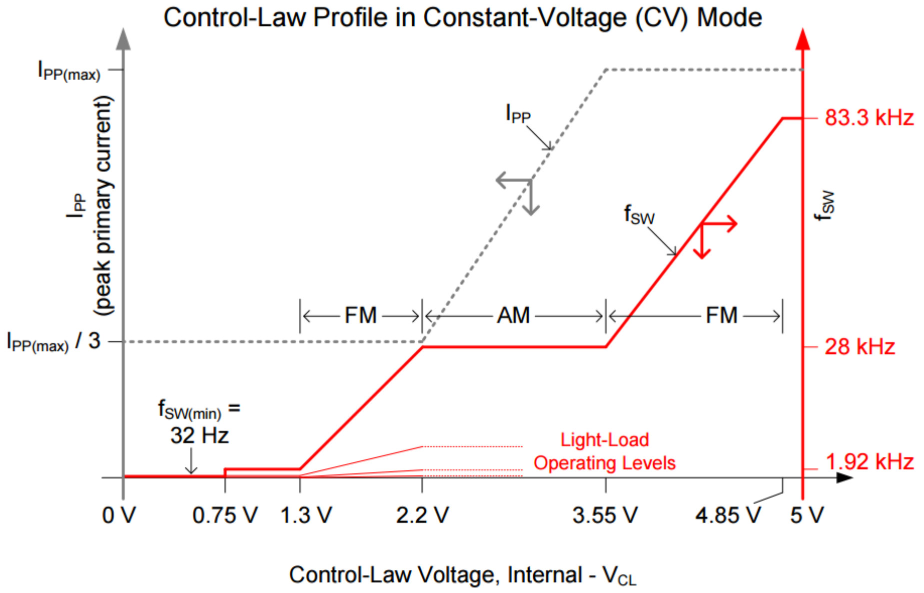
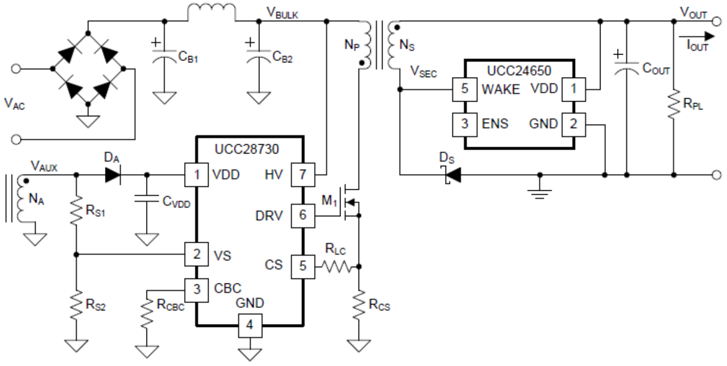
UCC28730 zero power: reducing f_{sw}

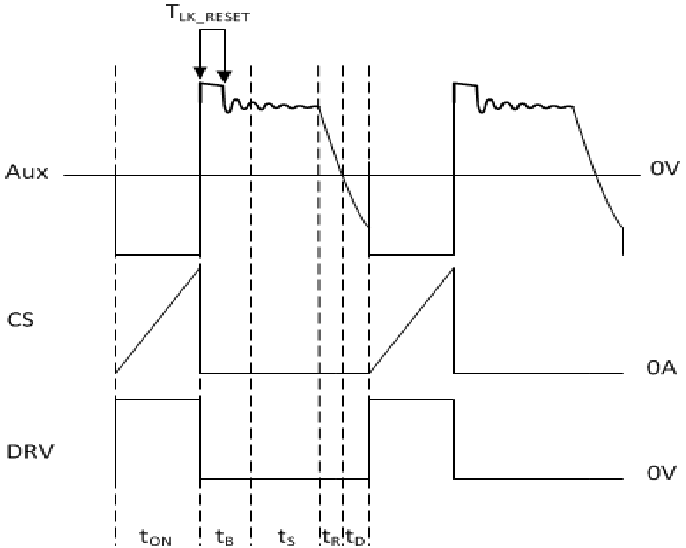
- Control Law
  - Reduces f_{SW} @ Standby (32 Hz minimum)
  - Enables
    - Low bias current (50uA)
    - P_{IN} < 5mW at Standby



Device timing/control

Simplified Application Schematic



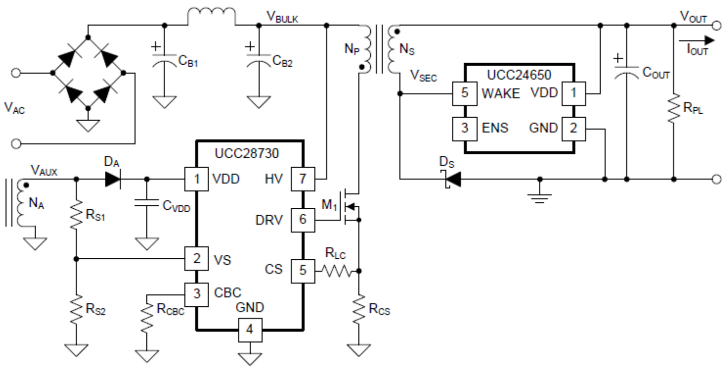


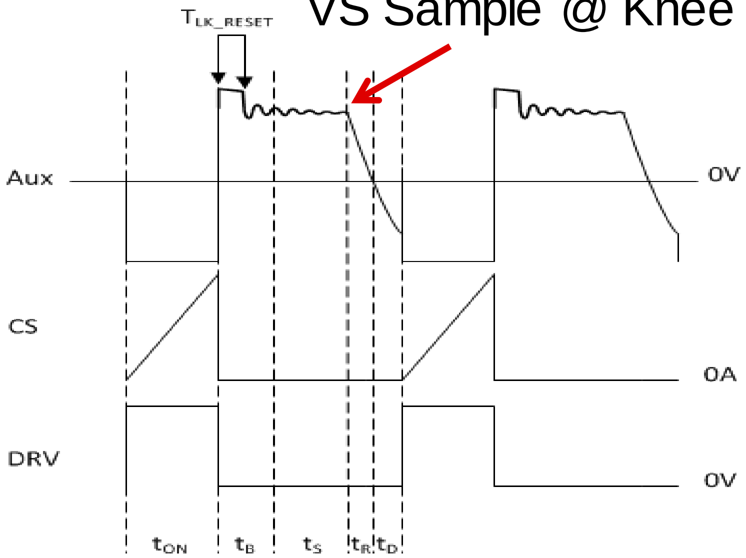
- ➢ At max frequency converter is close to critical conduction
- ➢ When DRV turns off OFF, VS looks for + transition and activates a VS blanking delay (t_B)
  - ▪ Prevents false OVP from leakage spike (T_{LK_RESET})
  - ▪ t_B adjusts with loading
    - • V_{CS} = 0.74V, t_B = 2.25 uS; V_{CS} = 0.245V, t_B = 750 nS

Device timing/sensing

VS Sample @ Knee

Simplified Application Schematic

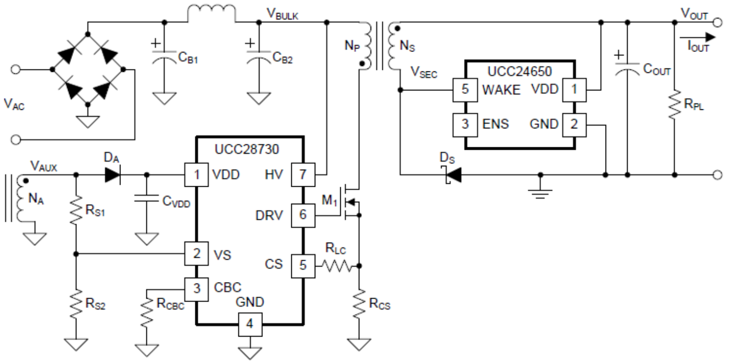


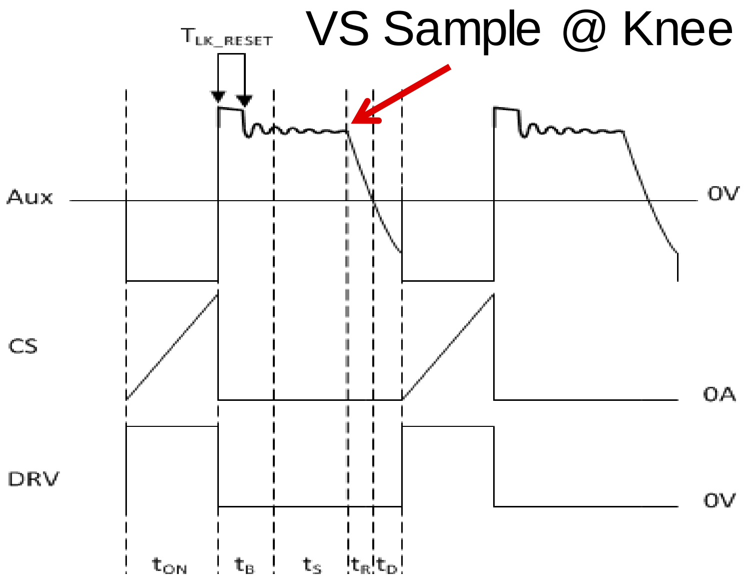


- ➢ After t_B times out
- ➢ VS sampling starts (t_S) detection for OVP and output control
- ➢ During t_S the VS pin is continuously sampled
  - Will hold the last VS value sampled before LC tank (t_R) of switch node (M1 drain)
    - This VS value is used to control the output
      - Helps remove errors caused by aux ringing
      - Ringing after delay needs to be < 100mV p-p

Device timing/sensing

Simplified Application Schematic

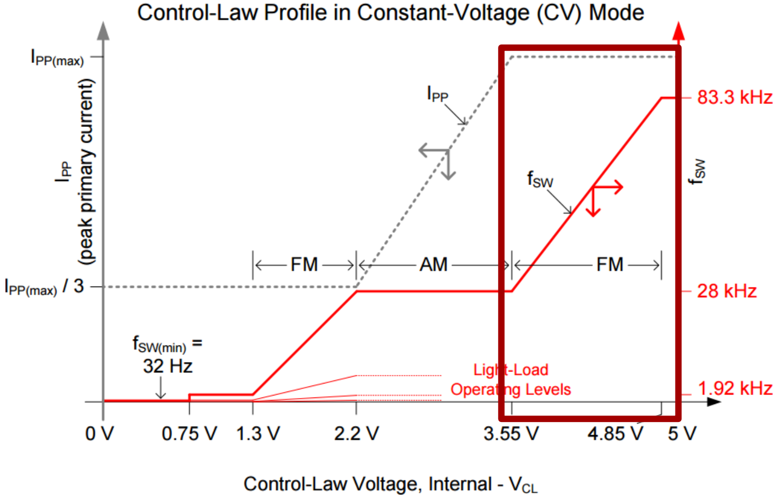


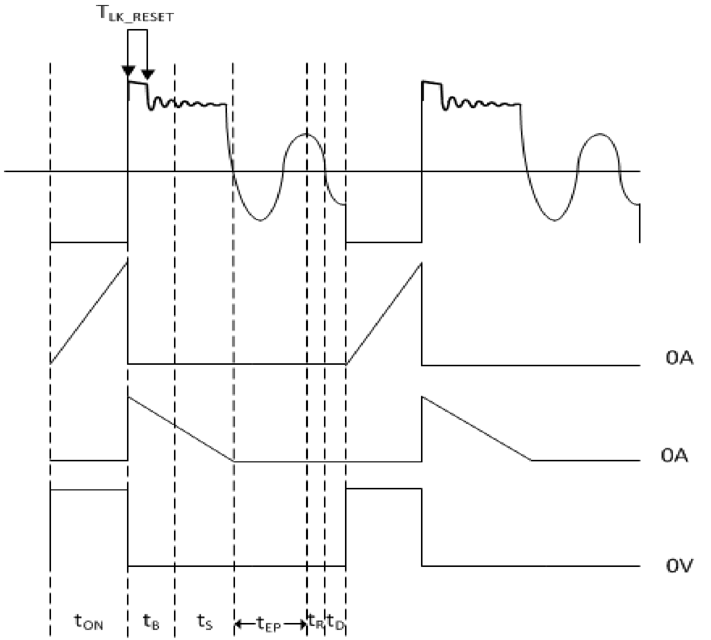


- ➢ After the controller has sampled the output at VS
  - ✓The switch node and aux winding will LC ring (t_R)
  - ✓The controller is looking for 0V transition of the Aux winding
    - When this occurs an internal timer/delay is triggered (t_D)
    - Once t_D has timed out DRV will turn back on
      - This added delay allows valley switching

Device timing/control (FM)

$$D = \frac{t_{ON}}{t_{ON} + t_B + t_S + t_{EP} + t_R + t_D}$$

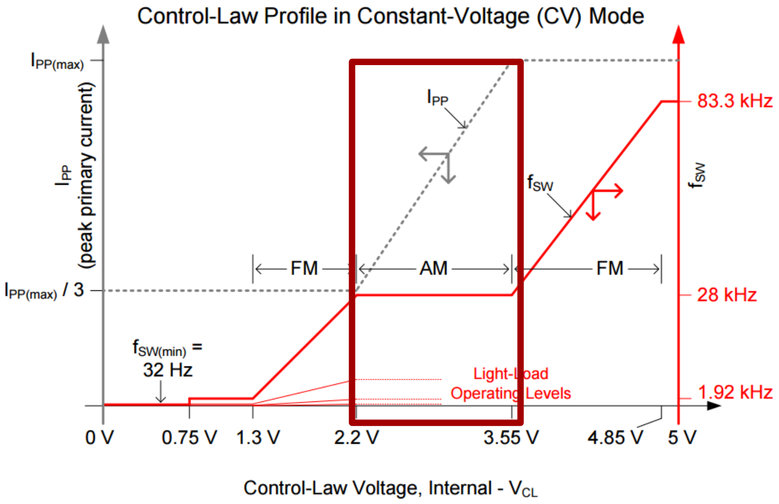


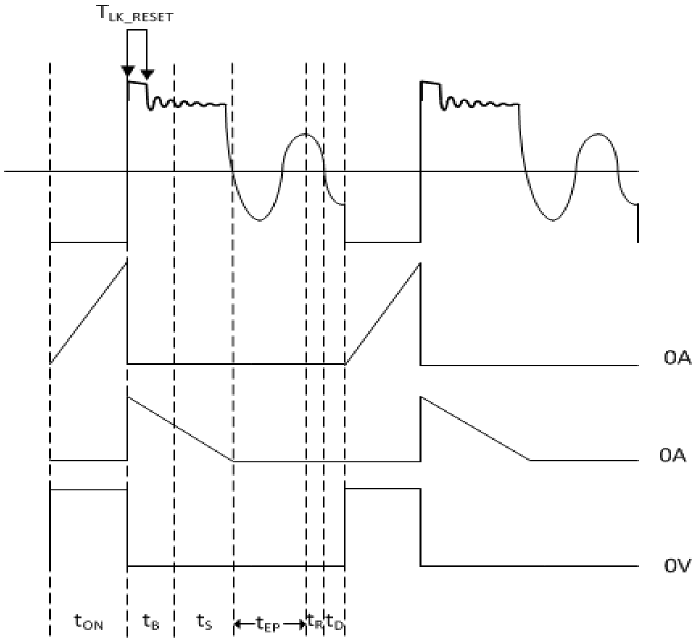


- $V_{E/A}$ 3.55V to 5V, V_{CS} = 0.74V
  - Fixed I_{PP} set at Max
  - A delay is added/adjusted (t_{EP}) to adjust D/frequency (28 kHz < 83 kHz)
  - Controller will not turn on M1 until VS zero is detected and t_D has timed out (150ns)
    - This achieves valley switching deep into DCM

Device timing/control (AM)

$$D = \frac{t_{ON}}{t_{ON} + t_B + t_S + t_{EP} + t_R + t_D}$$

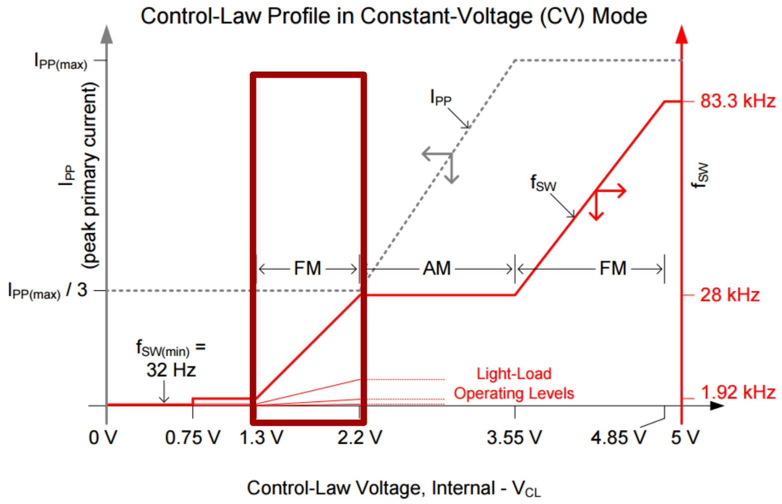


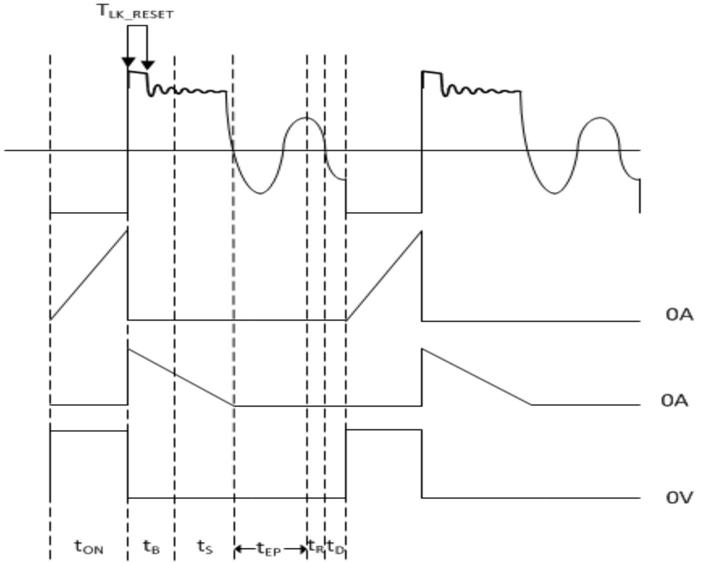


- $V_{E/A}$ 2.2V to 3.35V, V_{CS} = 0.74V to 0.245V
  - Converter is operating deeper into DCM
  - Frequency is Fixed 28 kHz (Excluding Dither)
  - Duty Cycle is Controlled by Adjusting CS amplitude (AM) from I_{PP} to 1/3 I_{PP}
    - Was done to remove audible noise as load and f decrease

Device timing/sensing (FM)

$$D = \frac{t_{ON}}{t_{ON} + t_B + t_S + t_{EP} + t_R + t_D}$$

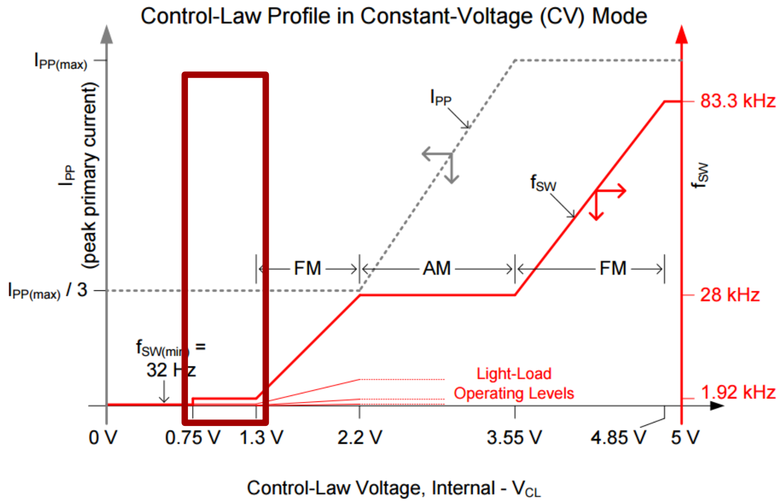


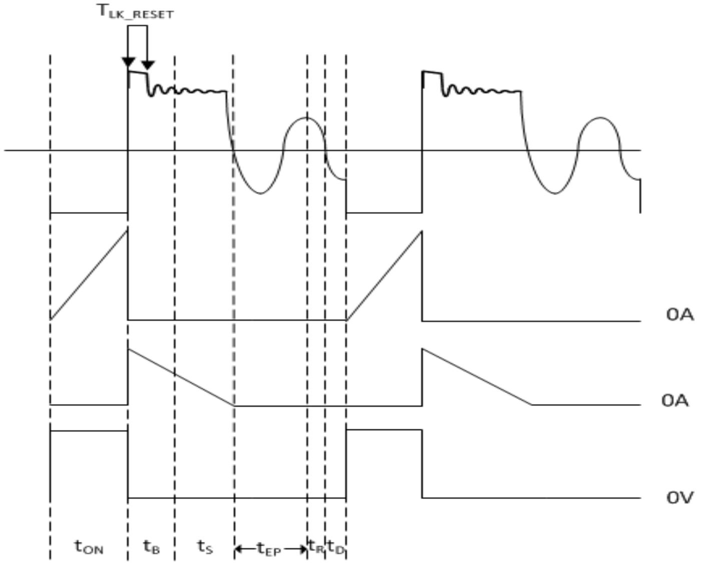


- $V_{E/A}$ 1.3V to 2.2V, V_{CS} = 0.245 V
  - Duty cycle is controlled by adjusting t_{EP} (VCO/fixed peak current again)
  - Frequency is adjusted from 28 kHz down to 1.92 kHz depending on E/A out
  - I_{PP} is fixed to 1/3 I_{PP} MAX

Device timing/sensing (FM)

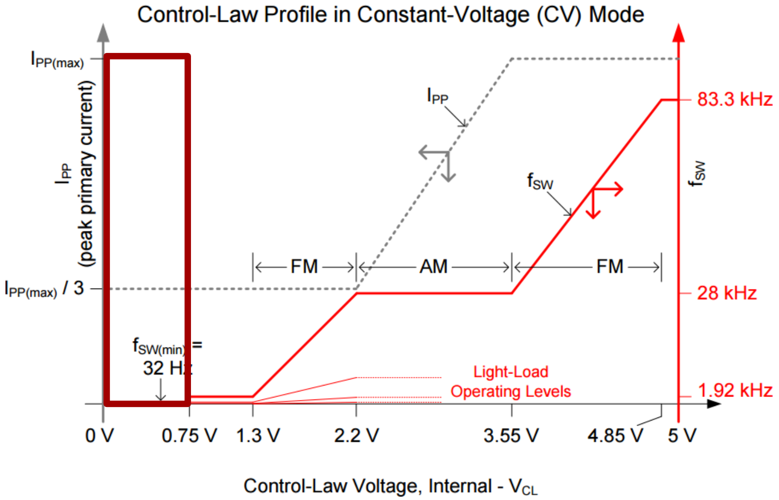
$$D = \frac{t_{ON}}{t_{ON} + t_B + t_S + t_{EP} + t_R + t_D}$$



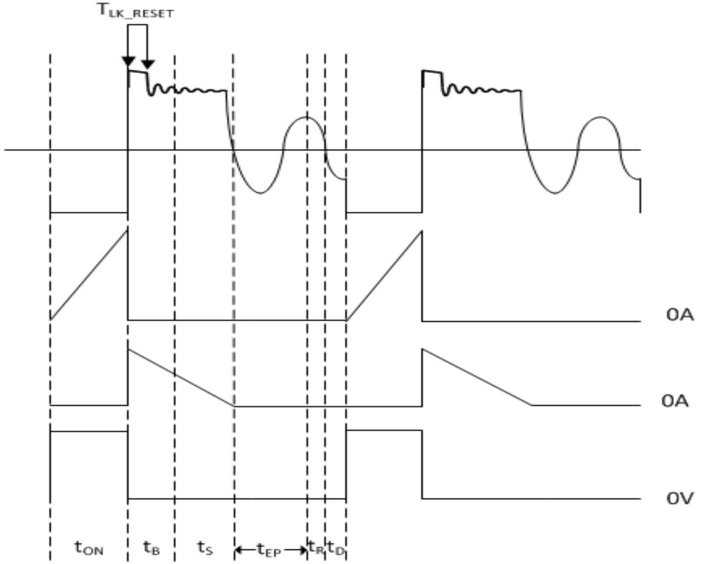


- VE/A 0.75 V to 1.3 V, V_{RCS} = 0.245 V
  - Frequency shifts to lower operating level as load gets lighter

Device timing/sensing (FM)



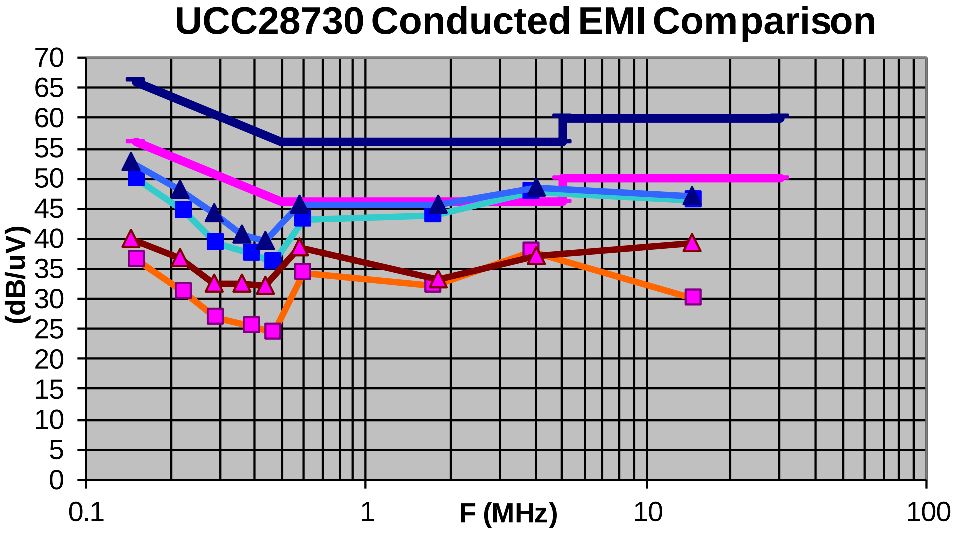
$$D = \frac{t_{ON}}{t_{ON} + t_B + t_S + t_{EP} + t_R + t_D}$$



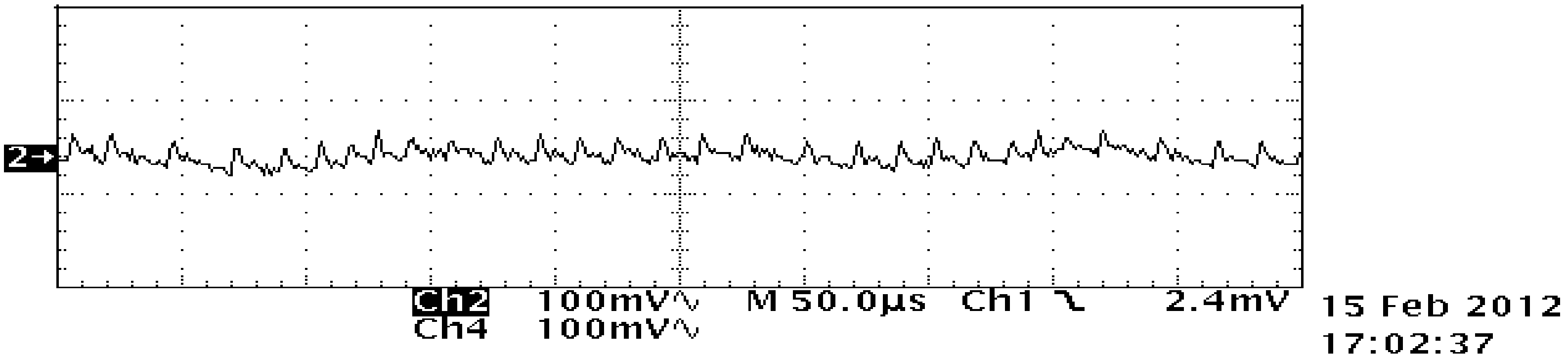
- VE/A 0 V to 0.75 V, V_{RCS} = 0.245 V
  - Frequency bottoms out at 32 Hz

System EMI reduction evaluation

- EMI comparison with and without dithering
  - ✓ Charger at 5V/1A: Vout return connected to earth
    - ✓ 2-5 dB reduction with EMI jittering scheme



Frequency dithering affects output ripple

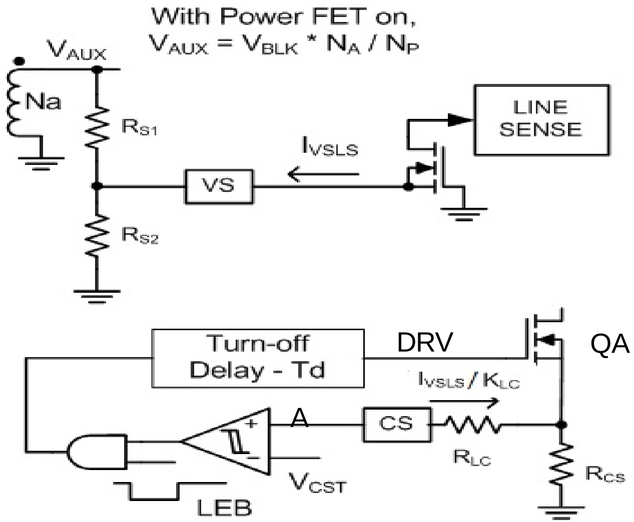


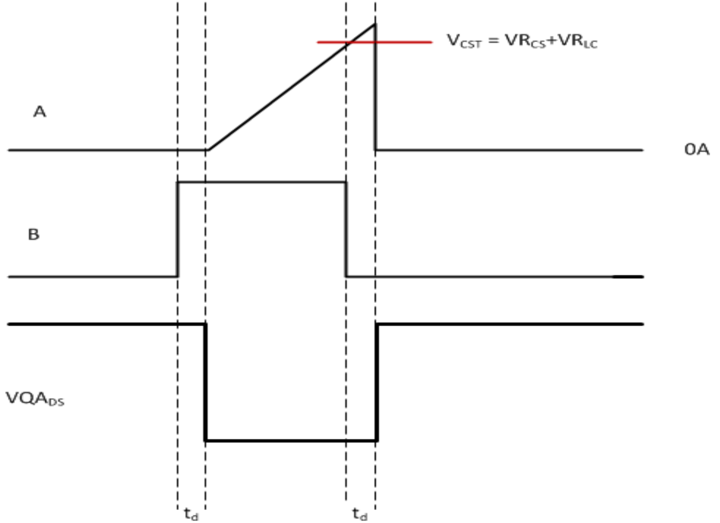
- Frequency jitter does cause a small amount of low frequency output ripple
  - Still meets USB specifications
  - CH2 = V_{OUT}

R_{LC} offset CS adjustment

$$R_{LC} = \frac{K_{LC} \times R_{S1} \times R_{CS} \times t_d \times N_{PA}}{L_P}$$

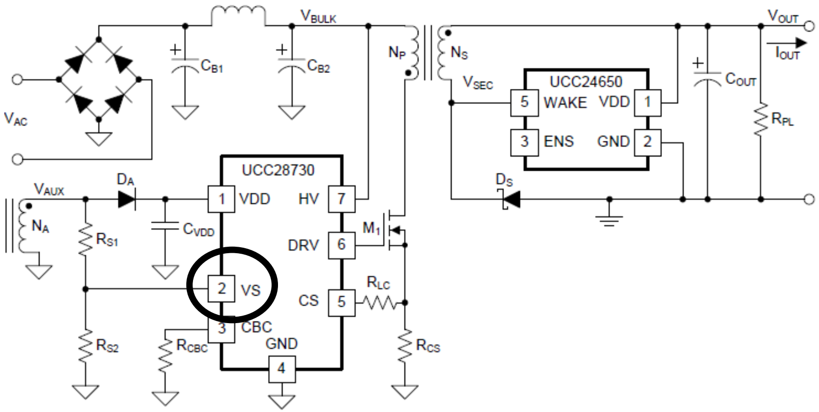
- Adds offset to the CS signal
  - Provides Some VFF
  - Provides an adjustment to reduce I_{PP} over shoot
    - Caused by FET turnoff delays





Design tips and recommendations

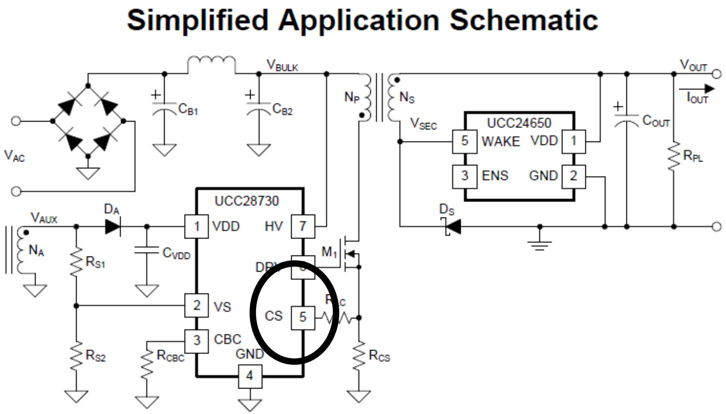
Simplified Application Schematic



➢VS Pin Recommendations

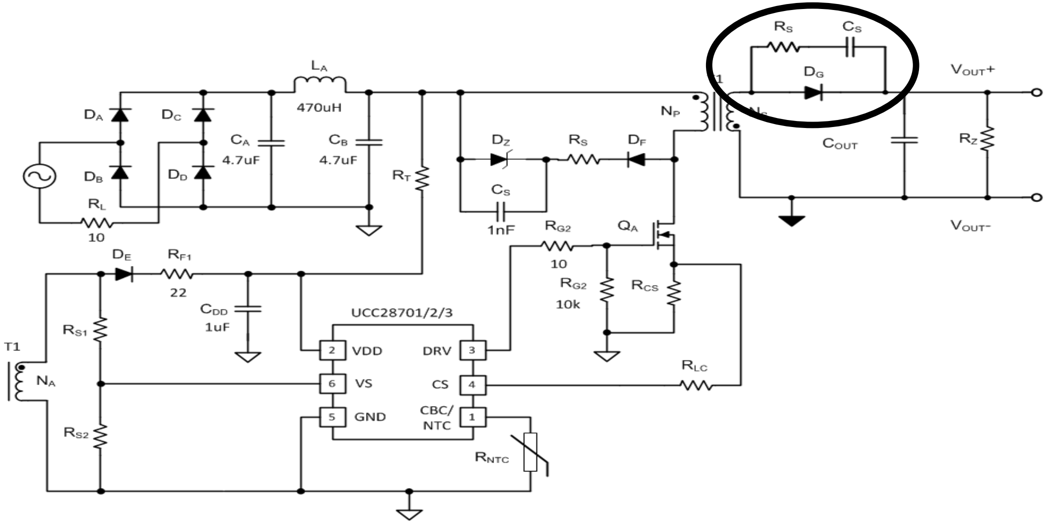
- No filtering/high impedance pin/noise sensitive
- Don’t probe the VS pin directly with a scope probe
  - Can estimate behavior at this pin from D_E

Design tips and recommendations



- CS pin recommendations
  - Device has 225 ns of leading edge blanking
  - Filtering should not be needed on the CS pin
    - -If cap is added to CS input, RC delay will affect value of R_{LC}

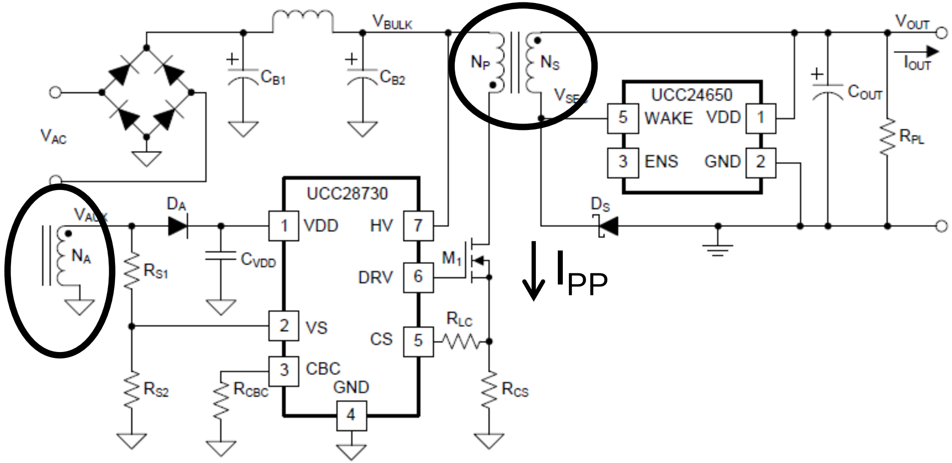
Design tips and recommendations



- Leave place for a snubber on the output
  - You may or may not need it
  - Excessive ringing on VS pin could cause misbehavior

Transformer calculations

Simplified Application Schematic



$$\frac{N_P}{N_S} = \sqrt{\frac{L_{PM}}{L_{SM}}}$$

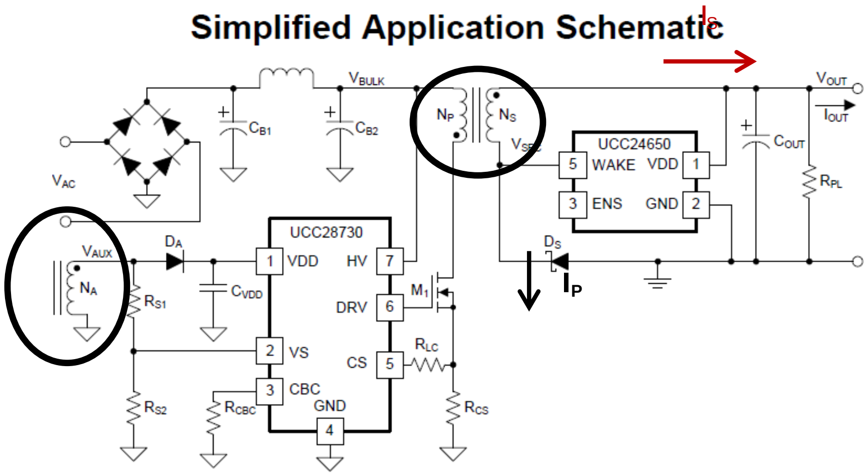
I_{PP} = Peak T1 Primary I_P

$$L_{PM} = \frac{\frac{2 \times P_{OUT}}{\eta}}{{I_{PP}}^2 \times f_{max}}$$

- T1 primary inductance (L_{PM}) set by f_{max}
  - f_{max} target 38 kHz to 76 kHz

Transformer turns ratio (N_P/N_S)

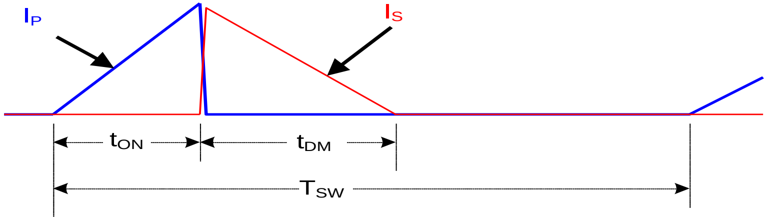
$$D_{MAX} = \frac{t_{ON}}{T_{SW}}$$



$$D_{MAG} = \frac{t_{DM}}{T_{SW}} \qquad D_{MAG} = 0.432$$

$$D_{MAX} = 1 - D_{MAG} - \frac{t_r \times f_{MAX}}{2}$$

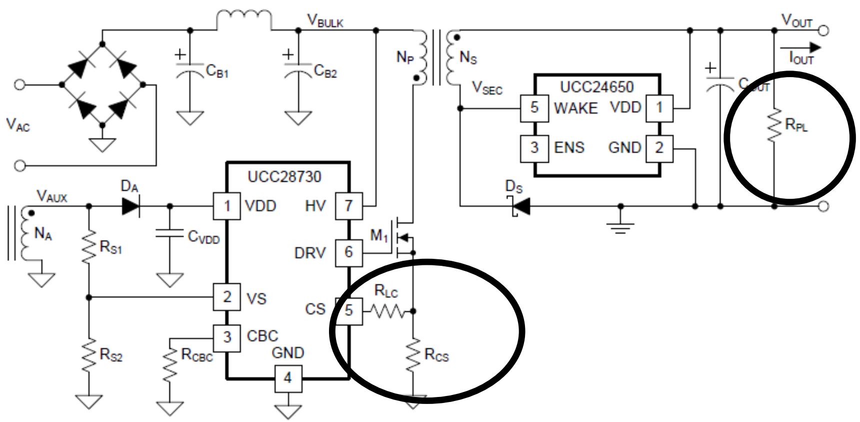
$$\frac{N_P}{N_S} = \frac{D_{MAX}\left(V1 - I_{PP}\left(R_{dson(QA)} + R_{CS}\right)\right)}{D_{MAG}\left(V_{OUT} + V_{DG} + V_{CBC}\right)}$$

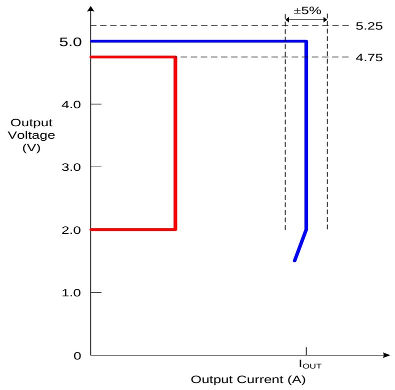


- L_{PM} selected based on f_{max}
  - UCC28730 requires D_{MAG} of 0.432 by design
  - Calculate D_{MAX} based on D_{MAG} and ½ of LC tank (t_r)
  - Use volt second balance to calculate N_P/N_S

Design tips and recommendations

Simplified Application Schematic





Typical Output V-I Characteristic

- R_{CS} and R_{LC} adjusted to fine tune circuit for maximum current (I_{OCC})
- Preloading (R_{PL}) is added/adjusted
  - Keeps output in Reg. at no Load
    - f_{MIN} is 32 Hz
    - f_{MIN} is generally higher for other PSR controllers

Device features: UCC28730

Low Standby Power Integrated 700-V Start-up Primary Side Regulated Flyback Controller

Features

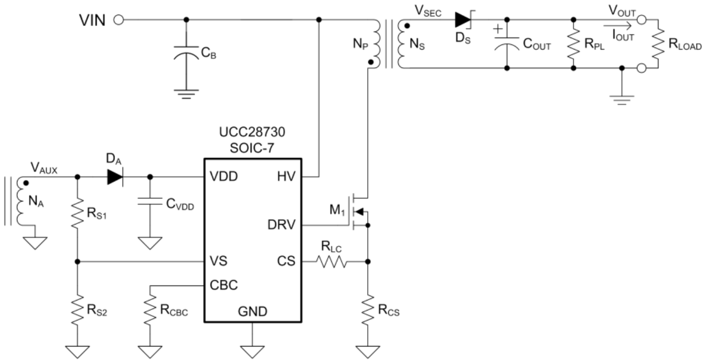
- **Less than 5mW standby power**
- AM-FM modulation scheme, operates at low frequency at light loads (no burst mode)
- Internal 700-V startup switch with X-Cap Discharge
- DCM operation with FET valley switching
- Frequency jitter scheme to reduce generated EMI/EMC
- Protection Functions: Over Voltage, Low Line & Over Current

Benefits

- **Exceeds energy star, coc tier 2, DOE level VI standards**
- Maintains regulation across load range with minimal audible noise
- Simplified fast start, lower standby power, and no leakage for bleed resistors
- Minimized switching losses to improve efficiency
- Minimal external filtering to pass EMI
- Intelligent protection with minimal external components

Applications

- Adapters and chargers for consumer electronics
- Home appliances
- Industrial automation
- Standby and auxiliary power supplies



Device features: UCC24650

200V Wake-Up Monitor for Fast Transient Primary Side Regulation (PSR) Controllers

Features

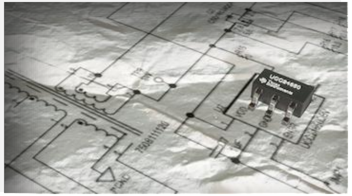
- **Less than 50µA I_Q**
- Fast wake-up
- No external components
- Enables secondary circuitry like synchronous rectifier
- 5-V to 28-V output monitoring

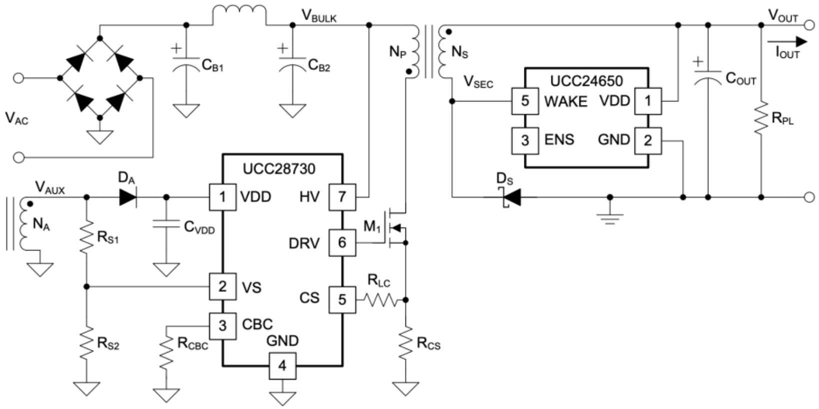
Benefits

- **Less than 0.6mW of power consumption**
- Can help to reduce output capacitances to save cost and space
- Small solution size
- No need to control across isolation barrier
- Supports a wide range of output voltages

Applications

- Adapters and chargers for consumer electronics
- Home appliances
- Industrial automation
- Standby and auxiliary power supplies





Summary: UCC28730 and UCC24650

- Fast transient response (C_{OUT}/7)
  - High power density
  - Save $$
- Industry's first PSR controller that help enables zero-standby (< 5 mW)
- Please use design tips to simplify your design process