Designing a modern power supply for RF sampling converters

By Thomas Neu
System Engineer, High-Speed Products

Introduction

Recently introduced high-performance converters for direct-radio-frequency (RF) sampling can operate without one entire RF down-conversion stage. This results in a simpler signal chain that uses a printed-circuit board (PCB) with a much smaller footprint. While RF sampling converters can help designers create a truly modern receiver, other system components such as the analog-to-digital (ADC) power supply need upgrading as well.

Using low-dropout regulators (LDOs) for post-regulation to reduce power-supply noise seem to be a quick, low-risk design implementation, but at the expense of 15 to 50% additional power consumption. Instead, system designers could spend time optimizing the design of the RF ADC power supply by using a high-efficiency switch-mode DC/DC regulator to achieve receiver noise performance similar to when using a low-noise LDO.

Understanding the ADC PSRR

The ADC power-supply rejection ratio (PSRR) gives information about the attenuation of noise on the power-supply inputs before the noise finds its way into the output spectrum. Power-supply noise from the DC/DC regulator is typically illustrated as voltage ripple riding on top of a DC voltage. It can be quantified as an AC signal with amplitude (voltage ripple) and frequency (the switching frequency of the regulator, $f_{DC/DC}$).

There are two different paths inside the ADC where noise on the power rail couples into the converter as illustrated in Figure 1:

- **Direct coupling into the analog input path.** The switching regulator spur shows up at $f_{DC/DC}$ in the spectrum.
- **Mixing products when the spurs couple into the clock path.** Two spurs in the spectrum are input-frequency dependent and located at $f_{IN} \pm f_{DC/DC}$. These spurs can be problematic in applications that have unwanted in-band interferers, such as radar systems. Because of the mixing operation, unwanted spurs from the power-supply noise can directly overlap with weak wanted signals and thus significantly impact receiver-sensitivity performance. Furthermore, the mixing spurs scale in amplitude with 20 log(f_{IN}/f_S); they increase in amplitude as the input frequency increases.

Figure 1. Power-rail noise coupling inside the high-speed ADC

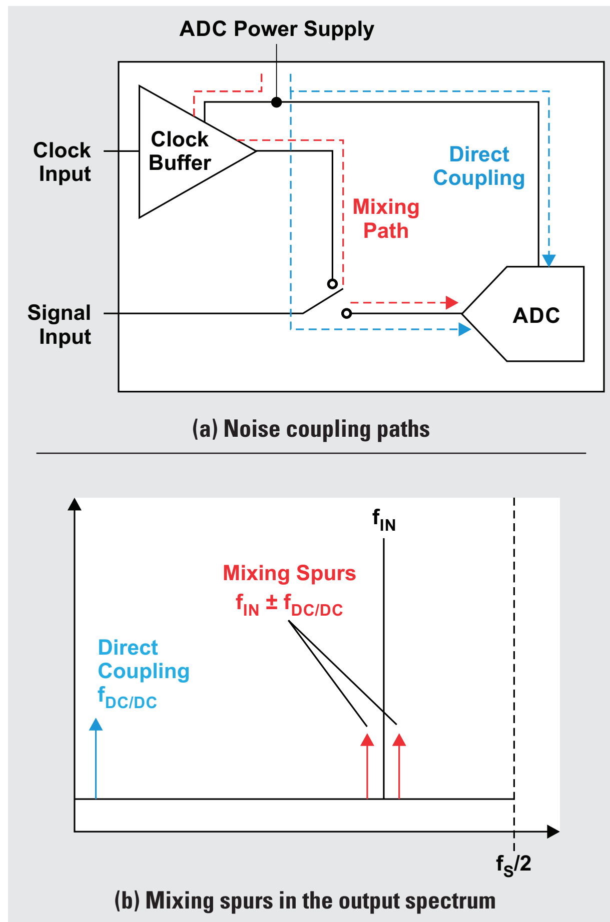
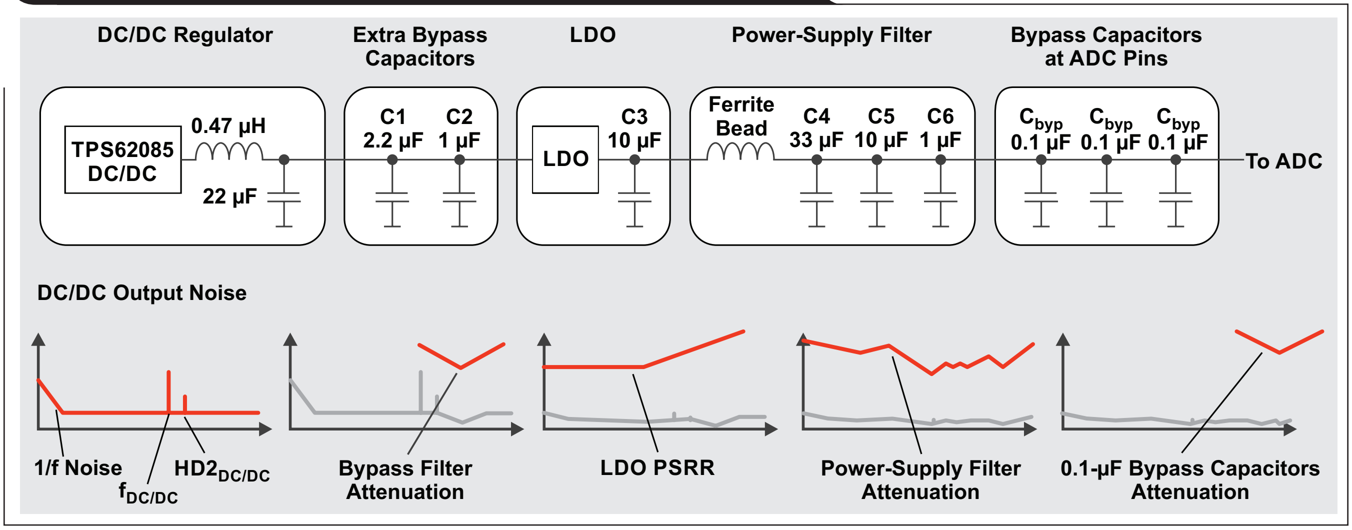


Figure 2. Power-supply chain in a traditional low-noise design



A conventional power-supply design for a high-speed data converter with low noise performance may contain up to five sections and look similar to Figure 2 (also implemented on the ADC32RF45 evaluation module).

The LDO reduces the noise contribution of the DC/DC regulator, which consists of the switching spurs and the flicker noise. Low-noise LDOs provide very good PSRR at low frequencies, but their PSRR decreases for higher frequencies. Certain applications require optimal flicker-noise performance and the LDO may be indispensable.

Bypass or decoupling capacitors provide a local path to ground for noise created by a circuit, decoupling one component or electrical circuit from another. Figure 2 shows bypass capacitors close to the switching regulator as well as the high-speed ADC. The 0.1-µF bypass capacitors located close to the data-converter pins have a resonant frequency beyond 10 MHz. They are not intended for filtering power-supply noise and spurs, but provide localized high-frequency bypassing for switching currents generated from the ADC.

Modern DC/DC regulators use switching frequencies beyond 1 MHz to reduce inductor size. At these frequencies, the LDO PSRR may only be 20 to 30 dB. Designers can attain a similar level of attenuation with an optimized power-supply filter design that eliminates the need for the LDO.

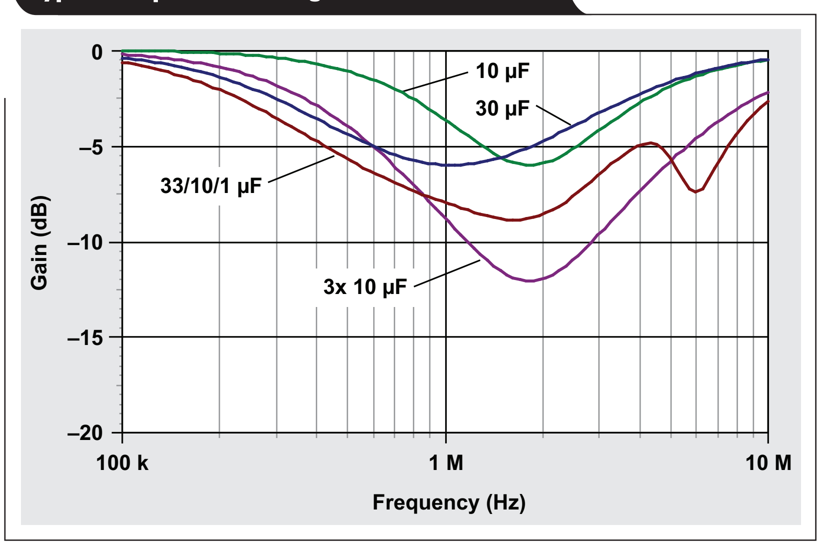
Optimizing the power-supply chain

The shotgun approach is a popular design method for a passive power-supply filter. This is where a ferrite bead is followed by a capacitor array with a wide range of different values (for example, from 33 µF to 0.1 µF) in an attempt to cover any possible spur frequencies.

With a basic understanding of the bypass capacitor and some design effort, filter performance can be optimized to the DC/DC converter switching frequency (~1.8 to 2.6 MHz for the TPS62085, depending on load current) while reducing capacitor count.

The capacitor array (33/10/1-µF) exhibits better broadband rejection compared to a single 10-µF capacitor. When taking package parasitics into consideration, however, simulation results in Figure 3 show that three parallel 10-µF capacitors show a 6-dB deeper notch around 2 MHz, instead of a shallow notch around 1 MHz from a single 30-µF capacitor. Depending on the amount of rejection needed, additional bypass capacitors can be added in parallel.

Figure 3. Frequency response of different bypass-capacitor configurations



When selecting actual components for the filter design, there are three important considerations:

- **Physical size:** Physically smaller capacitors save space (1206 vs. 0805); they also have less parasitics such as series resistance and inductance, which reduce the effectiveness of the notch filter.
- **The ferrite bead:** To be effective against switching noise, the ferrite bead needs to have a high impedance at very low frequencies (~1 MHz). Most ferrite beads have high impedance around 100 MHz but very little impedance at low frequencies. Thus, many ferrite beads are little help in attenuating switching spurs. A much more effective component is an electromagnetic interference (EMI) filter such as the NFM31PC276B0J3. It is inherently designed to have a notch filter around 2 MHz for use with modern switching regulators and can provide approximately 15 to 25 dB of rejection.
- **Capacitor material:** The material (X7R, X5R, Y5V) impacts capacitor performance in regards to aging (capacitance vs. time), DC voltage rating, temperature and tolerance.

Filter performance and spur improvement

When removing the low-noise LDO from the power-supply chain, the power-supply filter needs to provide about 20 to 30 dB of rejection at the switching frequency in order to make up for the missing LDO PSRR. As Figure 4 shows, the power-supply filter was tuned for that goal so that the overall spur performance would be comparable to using a low-noise LDO.

The switching regulator typically requires an inductor-capacitor (LC) filter at its output that is tuned with the internal compensation; however, some optimization is possible with this filter as well. In the TPS62085 data sheet, TI recommends the 0.47-µH inductor for an optimal transient response. During normal operation, the high-speed data converter presents a constant load and the transient response is not a factor. A larger inductor reduces output ripple (a 1-µH versus a 0.47-µH inductor cuts the ripple in half), which reduces the spurs at the expense of a (possibly) slightly bigger PCB footprint. Changing the output inductor is an option for further spur improvement.

The amplitude of the mixing spurs can be estimated with the following equations and component parameters:

- $A_{Mixing\_Spurs} = A_{DC/DC} + PSRR_{LDO} + PSRR_{Filter} + PSRR_{ADC}$ + Frequency_Adjust
- ADC32RF45 with f_S = 3 GSPS and f_{IN} = 1 GHz, clock amplitude = 1.5 V_{PP}.
- TPS62085 DC/DC regulator with 10-mV_{PP} ripple.
- The spur amplitude of the DC/DC regulator calculates to $A_{DC/DC} = 20 \log(A_{Spur}/A_{Clk}) \approx -43$ dBc.
- TPS74201 LDO with PSRR ≈ 25 dB at 2 MHz.

The estimated and measured results for various supply configurations are shown in Table 1.

Table 1. Estimated vs. measured spur amplitude for different configurations of the power-supply chain

Configuration	With LDO	No LDO	Optimized filter design without LDO	Comment
Spur amplitude $A_{DC/DC}$	–43 dBc	–43 dBc	–43 dBc	
PSRR LDO at 2 MHz	~–25 dB	—	—	
Power-supply filter at 2 MHz	~–15 dB	~–15 dB	~–35 dB	EMI filter + 3 x 10 µF
PSRR ADC	~–25 dB	~–25 dB	~–25 dB	
Input signal = 1 GHz, –1 dBFS	–9 dB	–9 dB	–9 dB	20 log (1G/3G)
Estimated spur amplitude	–117 dBc	–92 dBc	–112 dBc	
Measured spur amplitude	Noise (<–105 dBc)	~–97 dBc	Noise (<–105 dBc)	

This guideline is to get an estimate for the power-supply spur. There may be additional coupling paths—both inside the ADC as well as on the PCB itself—that can degrade rejection performance.

Figure 4. Optimized power-supply network with low-noise LDO removed

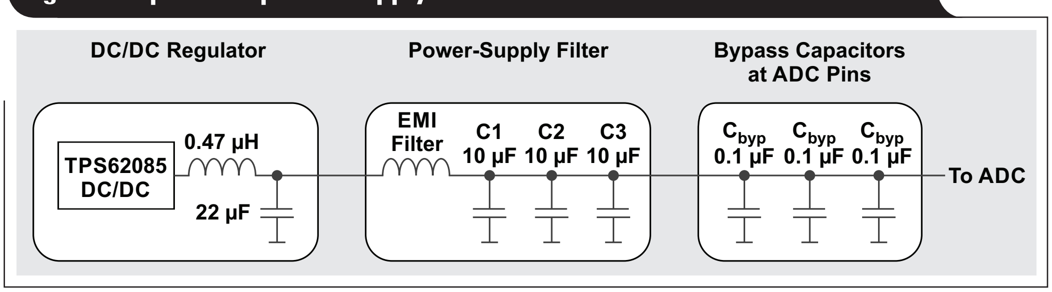
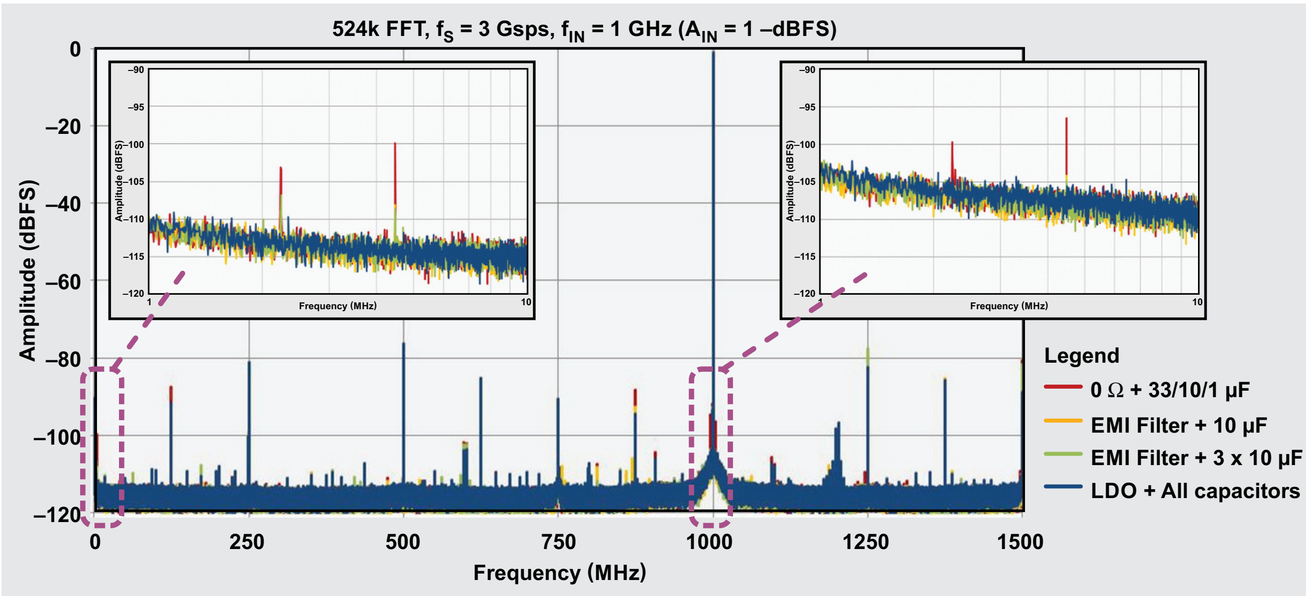


Figure 5. FFT comparison showing power-supply spurs close to DC and around the input signal



Even with a 524,000-point fast Fourier transform (FFT) and 20× averaging, the power-supply spurs are difficult to detect when employing the LDO or a tuned filter network, as shown in Figure 5. The switching regulator operates at $f_{DC/DC} \approx 2.3$ MHz; thus the spurs are located at $f_{Spur} \approx 2.3$ MHz and $f_{IN} \pm f_{DC/DC}$ = 1 GHz ±2.3 MHz. The spurs are in noise well below –100 dBFS, which attests to the effectiveness of the tuned filter network.

Conclusion

To address system power consumption, designers of modern high-bandwidth receivers have adopted a new architecture for direct-RF sampling that simplifies the receiver signal chain and results in reduced system power. Also, it is possible to save a lot of additional power consumption by optimizing the power supply for the data converter itself. Rather than using a low-noise LDO to improve power-supply noise, an optimized passive power filter can achieve similar noise rejection without the 15 to 35% additional power expense.

Related Web sites

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ADC32R45 evaluation module

Product information;
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