A comparative analysis of topologies for a bridgeless-boost PFC circuit

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Introduction

The need for miniaturization is driving increased power densities of switching power supplies used in network, server, computing, telecom and other industrial applications. Because high power density makes thermal management a big challenge if the efficiency isn't good enough, high efficiency becomes a prerequisite for high power density.

High efficiency is also an important concern in the design of any power supply for energy savings and environmental protection. Voluntary certifications like the 80-Plus initiative (especially its Platinum and Titanium derivatives) force power-supply designers to create innovative solutions to improve the overall efficiency of a switching power supply. These certifications also require a higher power factor. However, adding a circuit for power-factor correction (PFC) increases power losses.

One of the components contributing to power loss in switching power supplies is the front-end bridge rectifier, which converts the AC input to the high-voltage DC necessary for the operation of a conventional boost-PFC circuit. The bridge rectifier can easily consume 2% to 3% of the output power at low line voltages and at full load. Therefore, a bridgeless boost-PFC topology attracts interest for its ability to reduce conduction losses, since there is no input rectifier bridge.

This article provides an evaluation of common bridgeless-boost PFC topologies, including an assessment of their advantages and a review of design considerations in current application areas.

The classic bridgeless-boost PFC

Figure 1 is a schematic of a classic bridgeless-boost PFC. This topology can be derived from the basic diode bridge by moving the boost inductor to the AC input and replacing the bottom diodes with active switches. During each half-line cycle, a separate switching cell performs boost-PFC operation.[1]

Each operating cell consists of a power metal-oxide semiconductor field-effect transistor (MOSFET) and a diode. Q1 and D1 operate in boost switching mode for the half-line cycle when terminal L is high, and the body diode of Q2 functions as the current return path. On the other half-line cycle, Q2 and D2 operate in boost switching mode when terminal N is high, and the body diode of Q1 functions as the current return path.

Compared to a conventional-boost PFC, a bridgeless-boost PFC eliminates the losses caused by the bridge rectifier. However, the body diode of the inactive MOSFET conducts and effectively acts as a slow diode for the

Figure 1. Classic bridgeless-boost PFC
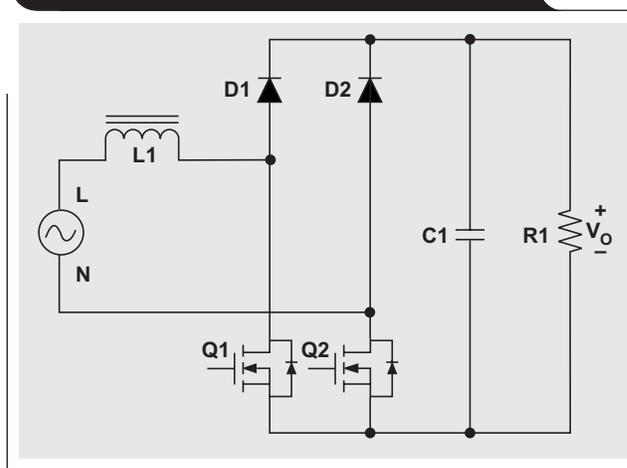
corresponding half-line cycle. The one-diode conduction loss for a bridgeless-boost PFC compared to the conduction loss from two diodes in a conventional-boost PFC can improve efficiency by eliminating the voltage drop of one diode in the line-current path.

The main advantage of a bridgeless-boost PFC is that Q1 and Q2 can be driven by the same pulse-width modulation (PWM) signal, greatly simplifying the control circuit.

In spite of the advantages of a bridgeless-boost PFC, there are certain concerns that need attention before arriving at a practical solution.

Because the input is floating with respect to the PFC-stage ground, the input voltage cannot be directly sensed. An isolated sensing method is required, like a low-frequency transformer, an optocoupler or an isolation amplifier.

For a conventional boost PFC, current sensing is as easy as placing a shunt resistor in the return path of the inductor current. However, for a bridgeless-boost PFC, the current path does not have the same ground at each half-line cycle, which means that current sensing for the bridgeless-boost PFC can be complicated.

Common-mode electromagnetic interference (EMI) is a problem with this bridgeless-boost PFC, as the output-voltage ground is always floating relative to the AC line input. Therefore, all parasitic capacitances—including the MOSFET drain to earth and output terminals to earth—contribute to common-mode noise. At the same time, the switching node for MOSFET Q2 and diode D2 are directly connected to the input line terminal. The high dV/dt of this node leads to increased common-mode noise that can be difficult to filter.

The dual-boost semi-bridgeless PFC

The dual-boost semi-bridgeless PFC shown in Figure 2 is a practical implementation that can address the EMI and voltage-sensing issues.

In Figure 2, the typical PFC inductor is split into L1 and L2 and connected from each input-line terminal to the corresponding switching node. Using two inductors removes the direct application of the switching node's high dV/dt to the input terminals; thus, the line potentials become more stable with respect to the board ground. Two diodes (Da and Db) link the PFC output ground to the input line and offer a return path linking the input terminals to board ground. These two modifications eliminate the common-mode noise problem of the bridgeless-boost PFC.

The addition of diodes Da and Db also helps resolve the input-voltage sensing issue. Now that the input is referenced to ground, isolated sensing is no longer necessary. Simple resistor dividers can be placed from both the inputs to ground to sense the input voltage.

During startup, diodes Dc and De peak-charge the PFC boost capacitor (C1), thereby avoiding the in-rush current going through D1 and D2 during this period. After C1 is charged, current does not flow through Dc and De. When analyzing the operation of the dual-boost semi-bridgeless PFC, the effects of Dc and De can be ignored.

Like the bridgeless-boost PFC, both Q1 and Q2 can be driven with the same PWM signal. Also, the two inductors compared to a single inductor helps improve thermal performance. However, because each inductor only works during one half of the input line cycle, the inductor utilization is low, and the total cost can increase.

Current sensing is still an issue with this topology. However, sensing both the switch currents and using a controller that has internal current synthesis to fill in for the diode current part of the current waveform (like TI's UCC28070) can help mitigate the issue.[2]

The bridgeless-boost PFC with a bidirectional switch

The limitations of a bridgeless-boost PFC make it impractical to implement. Figure 3 shows how it can be modified by adding diodes D3 and D4 and disconnecting the common-source node of switches from the output ground.[3]

In Figure 3, diodes D1 and D3 are fast-recovery diodes, whereas diodes D2 and D4 are slow-recovery diodes.

Figure 2. Dual-boost semi-bridgeless PFC
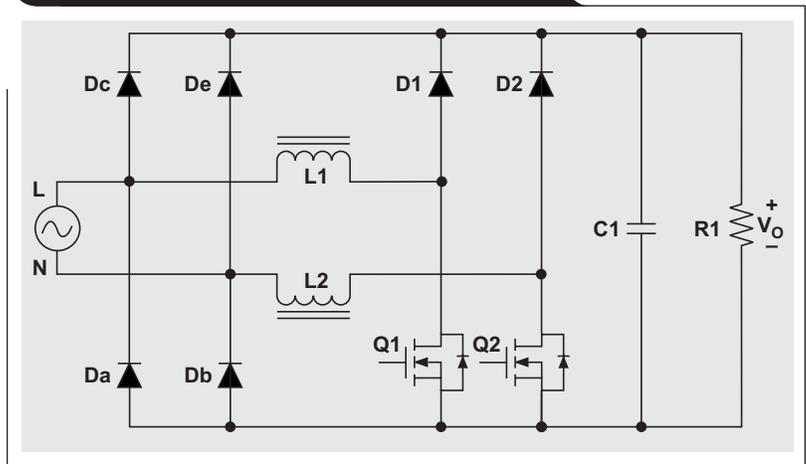
Figure 3. Bridgeless-boost PFC with a bidirectional switch
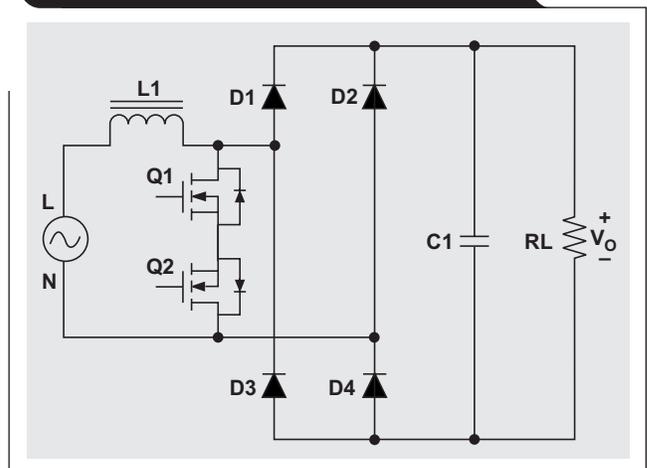
During the positive half-line cycle, the AC source connects to the output ground through slow-recovery diode D4. During the negative half-line cycle, the AC source connects to the positive terminal of the output through slow-recovery diode D2. This solves the problem of floating inputs, reducing common-mode EMI and easing input-voltage sensing.

Although both switches use the same PWM, driving them will be complicated because an isolated drive is needed. Current sensing still remains complex. Also, device utilization is still not very good, and thus can increase cost.

A totem-pole bridgeless-boost PFC topology

The totem-pole bridgeless-boost PFC topology shown in Figure 4 is a modification of the basic bridgeless-boost PFC topology shown in Figure 1 in that the positions of D1 and Q2 are exchanged. Because the two switches are one on top the other, the topology obtained is called the totem-pole bridgeless-boost PFC.

Both of the diodes in the totem-pole bridgeless-boost PFC can be slow-recovery type. During the positive half-line cycle, the AC input connects to the output ground through D1 and during the negative half-line cycle, the AC input connects to the positive terminal of the output ground through D2. Because the output is never floating with respect to the input, the common-mode EMI is better and input-voltage measurement is easier. The circuit has low conduction losses because only two semiconductor devices conduct during each half cycle of input voltage. It has the advantage of simple circuitry and high device utilization.

With silicon MOSFETs, the totem-pole arrangement allows operating in only discontinuous-conduction mode (DCM) or critical-conduction mode (CrM) because if continuous-conduction mode (CCM) is allowed, the reverse recovery of the MOSFET body diodes can cause excessive losses. The reverse recovery time of the body diode in silicon MOSFETs is much more than that of standard fast-recovery diodes. So the reverse recovery losses will be very high and the efficiency will be low.

The totem-pole bridgeless-boost PFC will need isolated or complex sensing for the inductor current. The gate drive can also be comparatively more complex, requiring a high-side/low-side or isolated drive.

Although the totem-pole bridgeless-boost PFC is limited in its use with silicon MOSFETs, the advent of silicon carbide (SiC) and gallium nitride (GaN) switching devices with zero-recovery reverse conduction has made it a preferred choice even in CCM operation. Although CCM operation is practical with these devices, when operating the circuit in zero-voltage switching, operating in CrM is much more beneficial because the output capacitance-related losses are removed in this mode. The advantages of low EMI, a simple circuit structure, high device utilization and low losses make it the preferred choice for SiC and GaN devices.

Figure 4. Totem-pole bridgeless-boost PFC
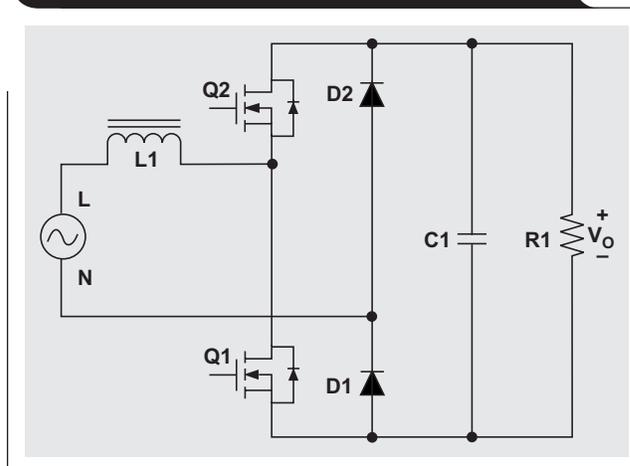
Conclusion

Given the limitations of silicon MOSFETs, the dual-boost semi-bridgeless topology was always the most popular choice for a bridgeless PFC. However, out of the topologies examined in this article, the totem-pole bridgeless-boost topology seems to be the most promising now that SiC and GaN switching devices are available.

References

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