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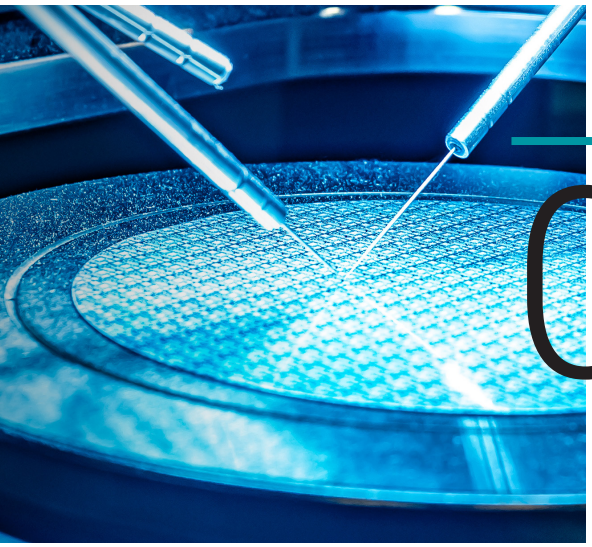

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How the ADC noise figure impacts RF receiver designs

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Introduction

In an effort to build smaller digital receivers, the aerospace and defense industry is embracing modern direct radio-frequency (RF) sampling analog-to-digital converters (ADCs). These ADCs eliminate RF mixing stages and are closer to the antenna, simplifying digital receiver designs while also saving cost and printed circuit board (PCB) area.

One critical (and often misunderstood) parameter is the ADC noise figure, which sets the amount of RF gain to detect very small signals. This article explains how to calculate the noise figure of an RF-sampling ADC, and illustrate how the ADC noise figure affects RF signal-chain designs.

Why the noise figure matters in digital receiver designs

The digital receiver operates in one of two distinct scenarios as illustrated in **Figure 1**. In the blocking condition, an interferer or jammer is present and the receiver has to operate with reduced RF gain in order not to saturate the ADC. In this setup, the ADC is driven close to full scale by the interferer; thus, the large-signal signal-to-noise ratio (SNR) of the ADC determines how weak a signal can be detected. There are additional degrading mechanisms such as phase noise and spurious free dynamic range.

In the second scenario, there is no interferer present. Detecting the weakest signal possible is solely dependent on the inherent noise floor of the receiver, a condition typically measured as receiver sensitivity. The noise figure measures the SNR degradation caused by components in the receiver signal chain.

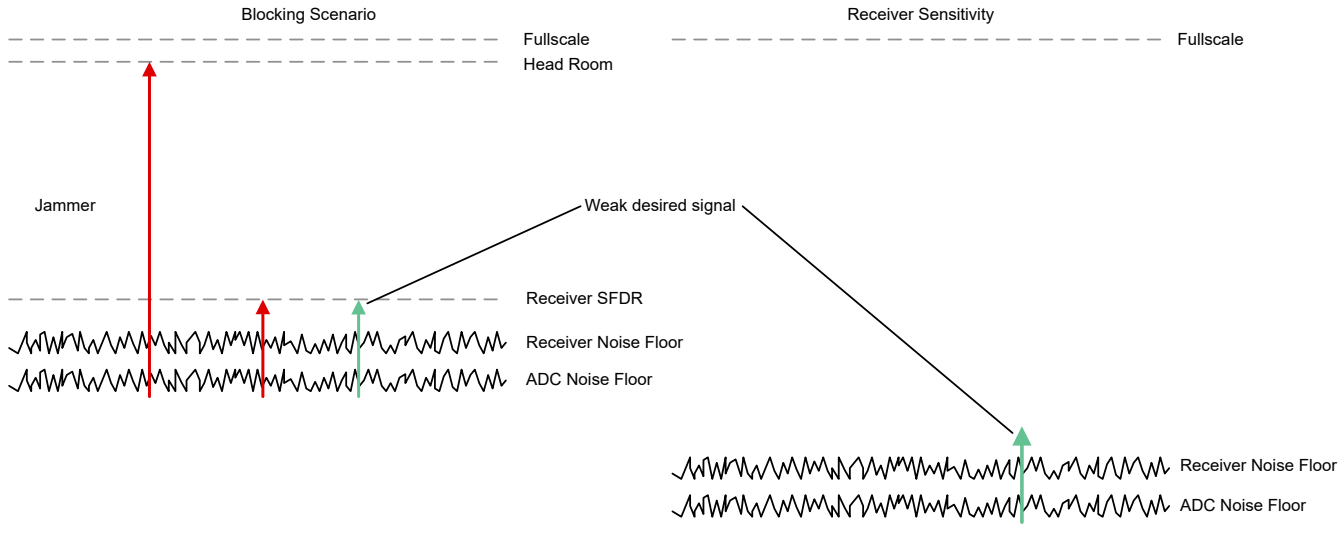

Figure 1. *Comparison between blocking or jamming and receiver sensitivity scenarios.*

The noise figure of the ADC is typically the weakest link of the receiver (approximately 25 to 30 dB), while low-noise amplifiers (LNAs) have noise figures as low as <1 dB. It is possible, however, to improve the ADC noise figure by adding gain to the analog RF front end (close to the antenna) using LNAs. The difference between a 1-dB receiver system noise figure and a 2-dB receiver system noise figure translates to approximately 20%. This difference means that a receiver with a 1-dB noise figure can detect signals with approximately 20% weaker amplitude. In a software-defined radio (SDR), that translates to radios with reduced output power – saving battery life – while in radar, that makes it possible to cover a longer distance.

Modern receiver designs in SDRs or digital radars use direct RF-sampling ADCs in order to reduce size, weight and power. This architecture simplifies receiver designs by eliminating the RF downconversion mixing stage. The better the ADC noise figure, the less gain required, which results in additional savings. Furthermore, using less additional RF gain means that when a jammer is present, there is less gain to reduce, with a higher dynamic range maintained in the receiver.

Calculating a system's noise figure

You can use the Friis equation to calculate a receiver system's noise figure. Assuming a simplified, ideal receiver with two amplifiers and one ADC, as shown in **Figure 2**, **Equation 1** calculates the cascaded system noise factor as:

$$F_{System} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 \cdot G_2} + \ldots + \frac{F_n - 1}{G_1 \cdot G_2 \ldots \cdot G_n - 1} \quad (1)$$

where F_x are the noise factors and G_x are the power gains.

The system noise figure in decibels is:

$$NF_{System} = 10 \log\left(F_{System}\right) \quad (2)$$

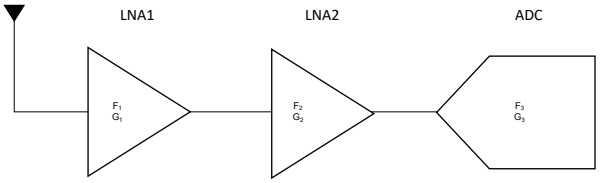

Figure 2. *Typical receive signal chain.*

There are two important things to highlight: the system noise figure is primarily dominated by the noise figure F_1 of the first element, as long as gain G_1 and G_2 are large enough to where the ADC noise figure F_3 is negligible.

Comparing two different ADCs with 20-dB vs. 25-dB noise figures in a system with two cascaded LNAs shows a drastic difference in system noise figures (see **Table 1**).

	LNA1	LNA2	ADC1	ADC2
Noise figure	1 dB	3 dB	20 dB	25 dB
Gain	12 dB	15 dB	0 dB	0 dB
Resulting system noise figure			1.8 dB	2.9 dB

Table 1. *System noise figure with two LNA stages.*

Getting the system listed in the ADC2 column (with a 5-dB worse noise figure) to a system noise figure below 2 dB would require an additional 10 dB of gain using a third LNA (noise figure = 3 dB), as shown in **Table 2**.

Table 2 highlights the impact of the ADC noise figure on the overall system noise figure. Adding a third LNA increases cost, board area (matching components, routing and power supply) and system power consumption, and further reduces the full-scale headroom.

	LNA1	LNA2	LNA3	ADC2
Noise figure	1 dB	3 dB	3 dB	25 dB
Gain	12 dB	15 dB	10 dB	0 dB
Resulting system noise figure				1.4 dB

Table 2. *System noise figure using ADC2 with three LNA stages.*

Assuming a target receiver sensitivity of –172 dBm, or very weak signals just 2 dB above the absolute noise floor (–174 dBm + 2 dB = –172 dBm), this receiver requires an noise figure better than 2 dB. Let's use the above example with ADC1 (with a 20-dB noise figure, as

listed in **Table 1**) and a cascaded system noise figure of 1.8 dB.

As shown in **Figure 3** and **Table 3**, LNA1 with a gain of 12 dB raises both the input signal and noise by 12 dB while degrading the noise figure by 1 dB (noise figure$_{LNA1}$ = 1 dB). LNA2 raises both signal and noise by 15 dB. Even though LNA2 has a higher inherent noise **Figure 3** dB, its impact is reduced to just 0.2 dB because of the 12-dB gain of LNA1.

Finally, the noise contribution of ADC1 (noise figure = 20 dB) reduces to just 0.6 dB, as it gets reduced by the 27-dB gain of both LNAs. Therefore, you end up with a system noise figure of 1.8 dB, which leaves approximately 0.2 dB of headroom to detect weak input signals.

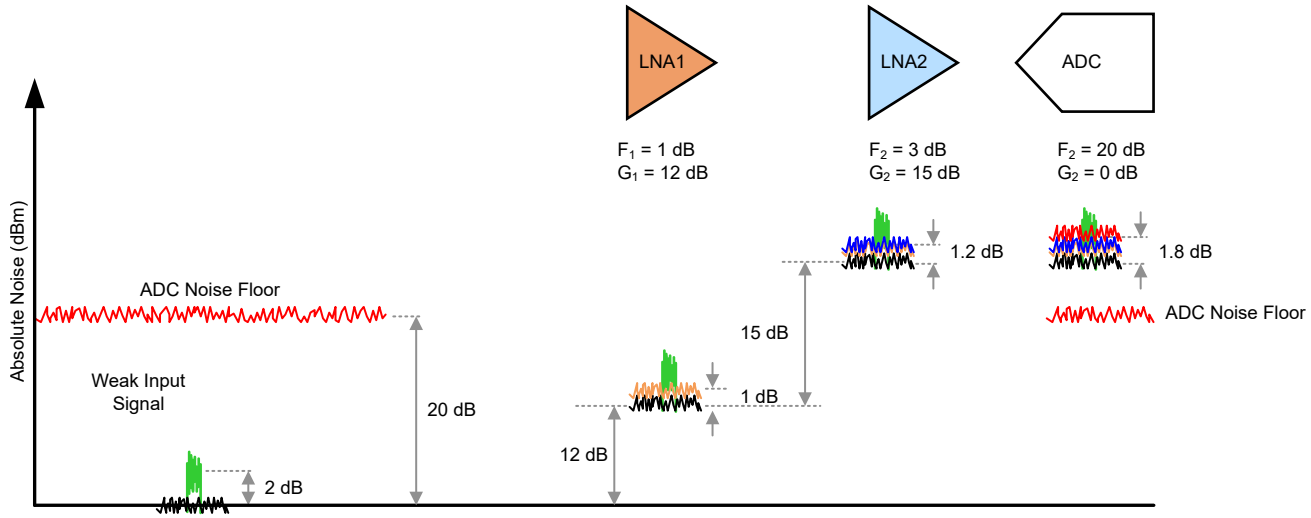

Figure 3. *Graphical illustration of the individual noise figure contributions in a receive signal chain.*

	LNA1	LNA2	ADC
Noise figure (dB)	1	3	20
Gain (dB)	12	15	0
Noise power (linear) 10^(noise figure/10)	1.26 $10^{1/10}$	2 $10^{3/10}$	100 $10^{100/10}$
Power gain (linear) 10^(gain/10)	15.85 $10^{12/10}$	31.62 $10^{15/10}$	1 $10^{0/10}$
Noise figure of LNA1 only (dB)	1	–	–
Noise figure of LNA1 + LNA2 only (dB)	1.2 10log[1.26+(2-1)/15.85]		–
Noise figure of LNA1 + LNA2 + ADC (dB)	1.8 10log[1.26 + (2-1)/15.85 + (100-1)/15.85/31.62]		
Additional impact on system noise figure (dB)	1	0.2	0.6

Table 3. *Calculations for individual noise figure contributions.*

High-speed data converters rarely list noise figure in the device-specific data sheet. The noise figure for an ADC can be calculated using **Equation 3** using the common data-sheet parameters (see **Table 4**) for the **ADC32RF54** RF-sampling ADC.

Parameter	Description	ADC32RF54 (1 times AVG)	ADC32RF54 (2 times AVG)
V	Input full-scale voltage peak to peak (V_{pp})	1.1	1.35
R_{IN}	Input termination impedance (Ω)	100 Ω	
FS	ADC sampling rate	2.6 GSPS	
SNR	ADC SNR for small-input signals (dBFS), typically –20 dBFS	64.4	67.1

Table 4. *Data sheet parameters of the ADC32RF54.*

$$\text{ADC Noise figure (dB)} = P_{SIG,dBm} + 174\ dBm - SNR\ (dBFS) - \text{bandwidth (Hz)}$$

$$\mathrm{NF_{ADC}\,(dB)} = 10\log\left(\frac{\left(\frac{V}{2\times\sqrt{2}}\right)^2}{R_{IN}}\times 1000\right) + 174 - \mathrm{SNR} \quad (3)$$

$$- 10\log\left(\frac{FS}{2}\right)$$

For the **ADC32RF54**, the noise figure calculates to:

Noise figure (1x AVG) = 20.3 dB

10log[(1.1/2/sqrt(2))^2/100 x 1000] +174 – 64.4 – 10log[2.6e9/2]

Noise figure (2x AVG) = 19.3 dB

10log[(1.35/2/sqrt(2))^2/100 x 1000] +174 – 67.1 – 10log[2.6e9/2]

Conclusion

The receiver noise figure is an important system design parameter because it determines the weakest detectable signal. In addition to a very low inherent noise figure, the **ADC32RF54** also provides a high SNR, which allows the system to maintain its noise figure even with a larger-input power signal. An ADC with same noise figure but a lower SNR would require a reduction in the input gain to prevent saturation, in which case the ADC noise figure starts adding more to the overall noise.

Comparing dual-supply discrete and integrated instrumentation amplifiers

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Introduction

The advantages and disadvantages of designing a discrete instrumentation amplifier (IA) versus an integrated IA are numerous and often debated. Some of the variables to consider include printed circuit board (PCB) area, gain range, performance (over temperature) and cost. The purpose of this article is to compare three dual-supply IA circuits: a discrete IA using a quad operational amplifier (op amp), a general-purpose IA with an integrated gain-setting resistor (R_G) and a precision IA with an external R_G.

Dual-supply circuits

Figure 1 is a simplified schematic of a discrete, dual-supply IA using the Texas Instruments (TI) TLV9064 quad op-amp circuit. In this circuit, three of the four amplifier channels (A, B and C) are connected as a traditional three-op-amp IA. The reference voltage (V_{REF}) connects to ground. With no use for the fourth channel, D, it is therefore connected as a buffer to mid-supply (ground) through a resistor for transient robustness. All resistors labeled "R" have a value of 10 kΩ; R_G sets the differential gain. The differential input voltage is $V_{IN+} - V_{IN-}$ and the output voltage is V_{OUT}. Some components, such as the load resistor (10 kΩ) and decoupling capacitors, are not shown. Drawing all circuits from a package perspective illustrates the number of external discrete components.

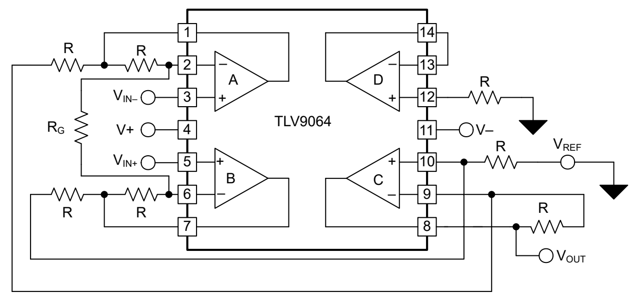

Figure 1. A discrete dual-supply IA using a quad op amp.

Equation 1 gives the transfer function for this circuit:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left[1 + \frac{20\ k\Omega}{R_G}\right] \qquad (1)$$

Designers will typically select a discrete IA when PCB area and performance are secondary to cost and gain range. TI's TLV9064IRUCR op amp was selected for this comparison because it is a rail-to-rail input/output device (RRIO) with a wide bandwidth (10 MHz) and a low typical initial input offset voltage ($V_{OS(typ)}$ = 300 µV), and comes in a small package (RUC = X2QFN = 4 mm^2). While there are less expensive RRIO quad op amps in RUC/X2QFN packages, they come at the expense of bandwidth and typical offset voltage.

To be consistent with the design priorities of discrete IAs, inexpensive ±1% tolerance, ±100-ppm/°C drift resistors were installed. Not only do these resistors differ in initial value, they will likely drift significantly over temperature. Since R_G is external, the gain for this configuration is primarily limited by the input offset voltage of the op amps.

Figure 2 is a simplified schematic of the TI **INA350ABS**, a general-purpose dual-supply IA with an integrated R_G. V_{REF} connects to ground. This circuit integrates all resistors in the IA. The differential input voltage is $V_{IN+} – V_{IN–}$ and the output voltage is V_{OUT}. Some components, such as the load resistor (10 kΩ) and decoupling capacitors, are not shown. The gain of the IA is set based on the switch connected to pin 1 (open = 20 V/V, closed = 10 V/V). In an actual application, the switch would not be present. To enable the device, connect pin 8 ($\overline{SHDN}$) to V+ or leave it floating.

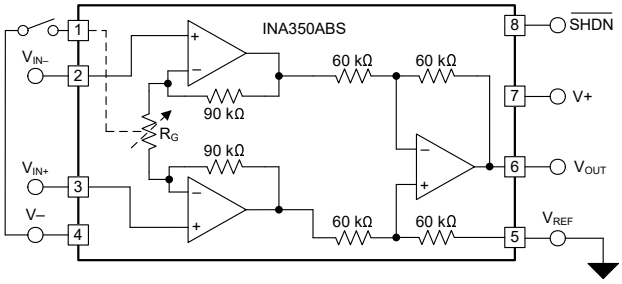

Figure 2. *General-purpose dual-supply IA with an integrated R_G.*

Equation 2 gives the transfer function for this circuit:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left[10\frac{V}{V} \text{ or } 20\frac{V}{V}\right] \quad (2)$$

Designers will typically select this IA when their requirements necessitate a balance of cost, performance and PCB area. The **INA350ABSIDSGR** IA was chosen for this comparison because of its affordability, performance, small package (lead DSG = WSON = 4 mm^2), selectable gain (10 V/V or 20 V/V) and low typical input offset voltage ($V_{OS(typ)}$ = 200 µV). This implementation needs no external components. For designs that require higher gains, the **INA350CDS** has gains of 30 V/V or 50 V/V.

Figure 3 is a simplified schematic of the TI **INA333** precision dual-supply IA with an external R_G. V_{REF} connects to ground. In this circuit, the IA integrates all resistors except R_G. The differential input voltage is $V_{IN+} – V_{IN–}$ and the output voltage is V_{OUT}. Some components, such as the load resistor (10 kΩ) and decoupling capacitors, are not shown.

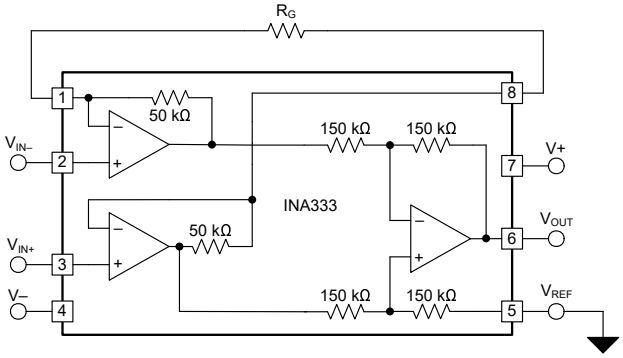

Figure 3. *Precision dual-supply IA with an external R_G.*

Equation 3 gives the transfer function for this circuit:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \times \left[1 + \frac{100\ k\Omega}{R_G}\right] \quad (3)$$

Designers typically use a precision IA when performance is the highest priority. The **INA333AIDRGR** precision IA was selected for this comparison because it is low voltage (5 V), has excellent precision (G = 1 V/V, $V_{OS(typ)}$ = 35 µV) and comes in a small package (DRG = WSON = 9 mm^2). The performance over temperature depends on the selection of the external R_G. Therefore, to be consistent with the primary design priority – performance – we used a precision R_G for a gain of 10 V/V (±0.05%, ±10 ppm/°C). Because the precision op amps are integrated, this implementation has excellent gain range (1 V/V to 1,000 V/V). The overall cost is usually greater than the other two solutions, however, given the integrated precision op amps and required precision R_G.

PCB layout

A PCB specifically designed for this comparison, containing the three circuits outlined above in a circular region, upon which the nozzle of a temperature forcing unit would fit. Care was taken to present the same input signal to each circuit, alleviating any concern for "leakage." Each output was routed separately to ensure isolation.

Figure 4 shows a simplified layout of each IA circuit to compare the relative sizes of each solution, including decoupling capacitors. For comparison purposes, the smallest device packages were used, along with resistors and capacitors in the 0402 package.

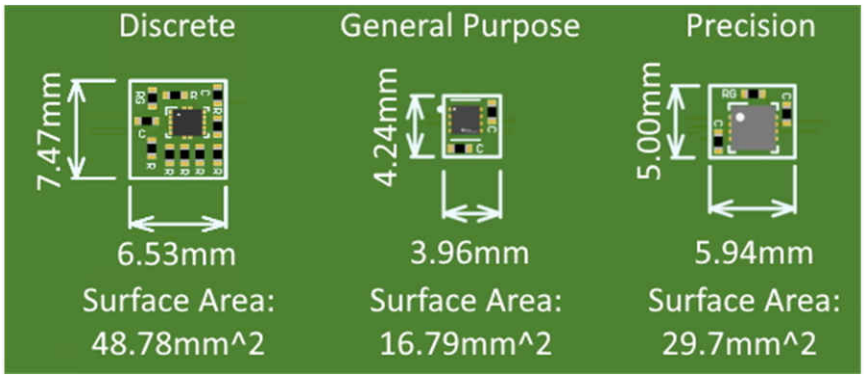

Figure 4. *Simplified PCB layout comparison for dual-supply IA circuits.*

As you can see, the discrete IA implementation is significantly larger than the two integrated solutions. And with the integrated R_G and overall smaller die size, the general-purpose IA layout is almost half the size of the precision IA layout.

Measurement results

Gain and offset errors were used as a measure of the relative performance of each circuit across temperature. As a baseline measurement, the precision dual-supply IA was put in a gain of 1 V/V (R_G = open). For each sweep, the input signals were scaled such that the output voltage ranged from –2 V to +2 V.

Table 1 depicts the baseline gain and offset errors for the precision IA, G = 1 V/V across temperature. The table includes the data sheet's typical gain and offset error values at 25°C, to validate the measurement system.

Temperature	–40°C		0°C		25°C		100°C		125°C	
Error Type	Gain	Offset	Gain	Offset	Gain	Offset	Gain	Offset	Gain	Offset
Measured (data sheet typical)	0.00270%	10.1 µV	0.00019%	9.1 µV	–0.00281% (±0.01%)	7.5 µV (±35 µV)	–0.00523%	23.5 µV	–0.00572%	31.2 µV

Table 1. *Precision IA gain and offset error vs. temperature (G = 1 V/V).*

Table 2 depicts the gain and offset error (referred-to-output [RTO]) for all IAs in a gain of 10 V/V and across temperature. The green shading indicates the highest-performing implementation at each temperature.

Temperature	–40°C		0°C		25°C		100°C		125°C	
Error Type	Gain	Offset	Gain	Offset	Gain	Offset	Gain	Offset	Gain	Offset
Discrete IA	–0.60853%	–4.09 mV	–0.70079%	–3.67 mV	–0.73929%	–4.07 mV	–0.90846%	–4.07 mV	–0.95486%	–3.69 mV
General-purpose IA	–0.02532%	2.07 mV	–0.03182%	2.05 mV	–0.00250%	2.04 mV	0.00876%	2.12 mV	–0.00970%	2.21 mV
Precision IA	0.17320%	–58.8 µV	0.08103%	–43.2 µV	0.02941%	–35.2 µV	–0.06125%	–2.2 µV	–0.07883%	33.8 µV

Table 2. *Gain and offset error (RTO) vs. temperature (Gain = 10 V/V).*

From a performance perspective, **Table 1** and **Table 2** show that without an external R_G, the precision dual-supply IA is superior to all other solutions. From a gain error perspective, the general-purpose and precision IA solutions are comparable. This is primarily because of the external R_G required for the G = 10 V/V precision IA implementation, whereas the general-purpose solution integrates R_G. When looking at the offset error, the precision IA solution is clearly the most accurate, while the general-purpose offset error is about half that of the discrete solution. Overall, the discrete IA has significantly worse performance when compared to both integrated solutions.

Conclusion

While many designers typically implement a discrete solution in low-cost applications, new general-purpose IAs (TI's **INA350**, for example) will likely yield lower overall cost and better performance. Depending on the gain, precision IAs such as the **INA333** can offer superior performance and gain range, although the external R_G is an important factor in performance, especially over temperature.

Table 3 summarizes the comparison.

	PCB Area	Gain Range	Performance	Cost
Discrete IA	48.78 mm^2	1 V/V to @100 V/V	Good	$$
General-purpose IA	16.79 mm^2	10, 20, 30, 50 V/V	Better	$
Precision IA	29.7 mm^2	1 V/V to 1,000 V/V	Best	$$$$

Table 3. *Comparison of dual-supply IA circuit solutions.*

The next time you are designing a dual-supply IA, weigh the trade-offs outlined in this article. For applications that require the greatest accuracy, precision IAs are the obvious choice. For applications that require cost-effective performance, the choice is no longer as easy as building a discrete IA. New general-purpose IAs can provide significantly better performance than discrete solutions, while taking up less PCB area and lowering system costs at the same time.

Optimize your application with a power path battery charger

Charles Harthan
Product Marketing Engineer

Introduction

With so many options for batteries and differing system requirements, it can be challenging to design the best battery charging integrated circuit (IC) to maximize battery lifetime and enable optimum system performance. The decision to choose a power path or non-power path battery charger can have a big impact on the functionality of your charging IC.

Figure 1 shows non-power path devices have one path for charging, in which the system and battery connect to the same node. This makes non-power path charging an effective option when you do not need to use the system and charge the battery at the same time, since you cannot control how much current is devoted to powering the system vs. charging the battery. Applications such as shavers or electric bikes are a good fit for non-power path chargers.

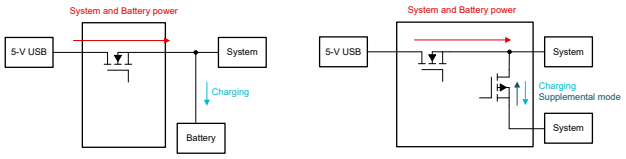

Figure 1. *Non-power path and power path block diagrams.*

Power path charging is a better option for products when both charging and use can occur simultaneously, since the integrated Q2 metal-oxide semiconductor field-effect transistor (MOSFET) in the battery allows you to customize the amount of current devoted to powering the system vs. charging the battery. This customization is also useful when a battery is deeply discharged. Because deeply discharged batteries are often charged with small currents, a power path device can independently regulate the system and battery current from the adapter to provide small current into the battery, ensuring that the system is still getting the required power to turn on.

When there is high demand for system current while charging the battery, the Q2 MOSFET can also turn on to combine power from the input and the battery to support the system load. This feature is known as supplement mode, where the device will pull current from the battery to supplement the current from the input in case the system is pulling more current than what the input can provide. A typical application that would benefit from power path charger features would be a smartphone.

The following sections show how power path topology improves system performance and battery life.

Maximizing shelf life

A product can be in transit and on the shelf for months before its purchase by a consumer, who typically prefers to use the product right out of the box. With some countries adopting new shipping restrictions that restrict batteries to only a certain amount of charge before they're shipped, it is crucial to conserve every bit of battery capacity.

In a non-power path topology, the system has to go into a low-power mode, as the system connects directly to the battery. Low-power mode often imposes requirements for a load switch or some other way to isolate the battery from the system.

In the power path topology, the battery FET can disconnect the battery from the system in ship mode – that is the state in which the product is consuming the lowest battery current. Ship mode also prevents the battery from powering the system by shutting off the battery FET. Designing your charging IC with power path

and ship mode can enable instant turnon right out of the box when the consumer plugs in the adapter or presses the power button.

Performing a watchdog reset

In some scenarios, when the system processor or host is nonresponsive, a forced hardware reset or a power cycle might be necessary; you can accomplish this with a watchdog reset. For instance, on TI's BQ25180 charger device, a hardware reset is possible when meeting conditions such as:

- No I2C communication for 15 s or more after plugging in the adapter.
- The user pressed the reset button for an extended period of time.
- A duration >40 s from the last I2C communication.

During a hardware reset sequence, the charger IC disconnects the system from the battery and adapter (if present), waits for a configurable duration, and then turns the system back on, enabling system startup and initialization. Because the battery is physically connected to the system, an external load switch might be necessary in a non-power path charger device to perform a hardware reset.

Employing the full battery capacity

Getting the most battery capacity is a primary goal when designing a charger IC, since it translates to more time between charging for users. Inaccurate termination current (I_{TERM}) monitoring can lead to charge termination at values higher than the desired I_{TERM} value and prevent use of the full battery capacity, as shown in **Figure 2**.

Power path enables the most battery capacity with a higher-accuracy I_{TERM}. In a lithium-ion (Li-ion) charging profile, the charge current tapers down during the constant voltage phase until it reaches I_{TERM} and then shuts off. In order to maximize the battery capacity, it is important to have a low I_{TERM} and the ability to accurately measure low I_{TERM} values to precisely terminate charging. Power path enables accurate current monitoring at low values by measuring the current passing through the Q2 battery FET.

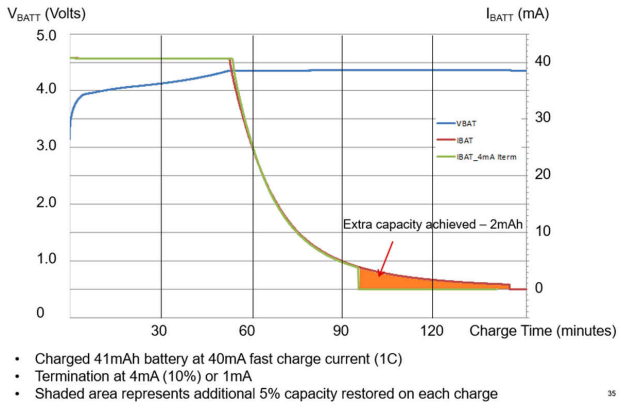

Figure 2. *Extra capacity from a lower I_{TERM}.*

Figure 2 also highlights how inaccurate I_{TERM} monitoring can lead to termination at 4 mA instead of 1 mA, which means that the user would lose 5% of the available 41-mAhr battery capacity. Because a power path charger regulates charging and system currents separately, any variations in system current will have no effect on the charging current. Charge termination can thus occur at a consistent pre-determined value, maximizing the battery's state of charge.

Using power path to enable accurate, low I_{TERM} is analogous to filling up a cup of water from a faucet. In the analogy, the cup is the battery, the water in the cup is the charge in the battery, and the water coming from the faucet is the charge current. The goal is to fill up the cup as much as possible without the water overflowing. It is much easier to do so by slowly decreasing the flow of water coming from the faucet as the water gets closer to the top, so that you can easily control the water level. Allowing the fastest flow from the faucet at all times will likely cause the water to overflow, or you will pull the cup away from the faucet before you've used all of the cup's capacity. Translating back into battery charger terminology, reducing the charge current (water from the faucet) to a controlled, measurable I_{TERM} allows the charger to fill the battery (the cup) with as much charge (water in the cup) as possible, without overcharging or undercharging the battery.

Minimizing battery fatigue

When a rechargeable battery is exposed to multiple charge and discharge cycles, its ability to power the system degrades, which can negatively affect its performance and run time. In order to maximize the lifetime of both the battery and the system, it is important to design the IC to limit the overall cycle count of the battery.

Figure 3 shows that the cell capacity of a Li-ion battery decreases as the number of recharge cycles increases. Designing a power path battery-charging IC enables you to maximize its lifetime by shutting off the battery FET – powering the system directly from the adapter and preventing the system from using the battery for power eliminates the need to discharge and recharge the battery. With power path, you can choose to power the system with only the adapter if the adapter is present, which reduces the number of recharge cycles on the battery and maximizes its lifetime.

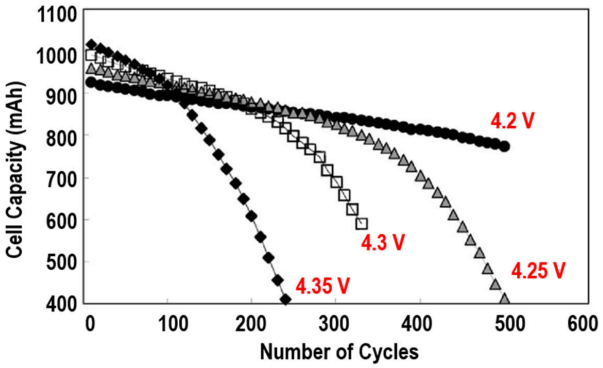

Figure 3. *Li-ion cell capacity vs. number of recharge cycles.*

Note

Factors that affect cycle-life and possible degradation mechanisms of a Li-Ion cell based on LiCoO2," Journal of Power Sources 111 (2002) 130-136 .

TI power path battery chargers

Linear chargers such as the **BQ25180** are useful in charge current applications <1 A. The BQ25180 comes equipped with ship mode to provide a low-power mode to conserve the battery. In ship mode, the battery quiescent current is only 15 nA, which is significantly lower than the 3-µA battery quiescent current in the BQ25180's normal operation. It is possible to program the BQ25180 to have an extremely low I_{TERM} of 0.5 mA, which helps charge the battery to its full capacity. Adjusting the I_{TERM} is simple, as it is a fixed 10% of the programmed fast charge current, and easily changeable through I^2C communication. This charger also prioritizes system power with supplement mode.

The **BQ25620** is a switching buck charger that comes equipped with power path. Switching chargers are useful in applications that need a charge current >1 A, since switching chargers are better for higher-power applications. The BQ25620 can support up to 3.5 A of charge current. It also has ship mode for battery conservation, with 150 nA of battery quiescent current, while supplement mode optimizes system performance. In order to maximize battery capacity, the BQ25620 has an I_{TERM} as low as 10 mA and can be easily customized with I^2C communication.

Conclusion

There are trade-offs between a power path or a non-power path battery-charger IC. Battery-charger ICs with power path provide additional functionality with the integrated battery FET: additional power modes such as ship mode to conserve the battery, full system reset capability to recover unresponsive hosts, and the ability to maximize both the battery capacity for longer run times and minimize battery fatigue. These types of charger ICs will help increase battery and system performance in applications that need simultaneous charging and system use.

Related Websites

- For an overview of the differences between linear and switching chargers, watch the video **Introduction to Battery Charger Topologies and Their Applications**.
- The video **Fast-Charging Trends and Challenges for Single-Cell Batteries** has more details on charger battery safety features.
- To learn more about ship mode, read the technical article, **Pull the Tab: How to Implement Ship Mode in Your Lithium-Ion Battery Design**.

Powering precision ADCs: Average versus transient current

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Introduction

Understanding the analog-to-digital converter (ADC) data-sheet power-supply parameters can help you design more reliable precision data acquisition (DAQ) systems. Specifically, it is important to understand that current consumption in an ADC data sheet is an average value specified at steady-state operating conditions. These measured current values therefore do not characterize transient current demand, even though ADC transient currents can be orders of magnitude larger than the specified ADC current. Transient currents can occur when transitioning between different ADC modes of operation and are most significant when initially powering the device. Moreover, the circuitry and components surrounding the ADC can cause additional transient current demand.

This article delves into the topic of ADC transient current demand by first introducing how a typical ADC data sheet specifies current, and then sharing the results of several tests that quantify transient current demand under different operating conditions. Multiple power-supply configurations that can source both average and transient currents are discussed, and finally the effects of various power-down methods are compared.

Power-supply specifications

Current consumption in an ADC data sheet is an average value specified at steady-state operating conditions. An ADC with many different operating conditions requires the specification of several current values. These conditions can include an average ADC supply current that scales relative to the data rate or increased current demand when enabling internal features such as programmable gain amplifiers (PGAs) or voltage references (VREFs). As an example, **Table 1** shows the data-sheet power-supply specifications at different operating conditions for TI's **ADS1261**, a 24-bit, 40-kSPS, 11-channel delta-sigma ADC with an integrated PGA and VREF.

Power Supply						
Parameter		Test Conditions	MIN	TYP	MAX	Unit
I_{AVDD}, I_{AVSS}	Analog supply current	PGA Bypass		2.7	4.5	mA
		PGA mode, gain = 1 to 32		3.8	6	
		PGA mode, gain = 64 or 128		4.3	6.5	
		Power-down mode		2	8	µA
I_{AVDD}, I_{AVSS}	Analog supply current (by function)	Voltage reference		0.2		mA
		40-kSPS mode		0.5		
		Current sources		As programmed		
I_{DVDD}	Digital supply current	20 SPS		0.4	0.65	mA
		40 kSPS		0.6	0.85	
		Power-down mode		30	50	µA
P_D	Power dissipation	PGA mode		20	32	mW
		Power-down mode		0.1	0.2	

Table 1. *The data-sheet power-supply specifications for the ADS1261.*

The highlighted PGA Bypass section in **Table 1** shows that the average analog current drawn by the **ADS1261** during normal operation with the PGA bypassed is 2.7 mA (typical) or 4.5 mA (maximum). The highlighted "by function" section indicates how much the current increases when enabling each function. All of these supply-current specifications are characterized by measuring the average current drawn by the device after the current settles.

Data-sheet power-supply specifications therefore average out any transient current demand that the device or supporting circuitry requires during normal operation. This is important because transient currents during startup and switching can be significantly larger than the values specified in the data sheet. A reliable system design must be able to account for both average and transient current demand.

Transient currents

One challenge with transient currents is that their magnitude and duration can vary significantly as a result of the ADC operating conditions and surrounding circuitry. ADC data sheets therefore rarely specify transient currents. However, it is possible to measure transient currents for a given system configuration by probing with an oscilloscope across a small-value resistor placed in series with the power-supply trace. You can then use Ohm's law to determine the resulting current.

The **ADS1261** has an evaluation module (EVM) that incorporates such a resistor between the power-supply output and the ADC AVDD pin. **Figure 1** shows the relevant portion of the EVM schematic that includes a 10-Ω measurement resistor (R33). Measuring the average or transient voltage drop across this resistor and then dividing by 10 Ω calculates the average or transient current drawn by the **ADS1261**, respectively. I performed multiple tests under a variety of conditions to better understand the transient current behavior of this ADC.

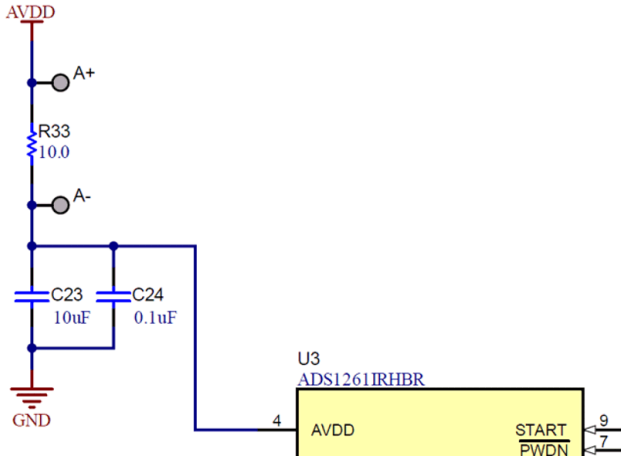

Figure 1. *Transient current test circuit using the ADS1261 EVM.*

The first transient current test was a power-up test with the recommended 10-µF (C23) and 0.1-µF (C24) decoupling capacitors from AVDD to ground installed. **Figure 2** shows the **ADS1261** transient current under these conditions.

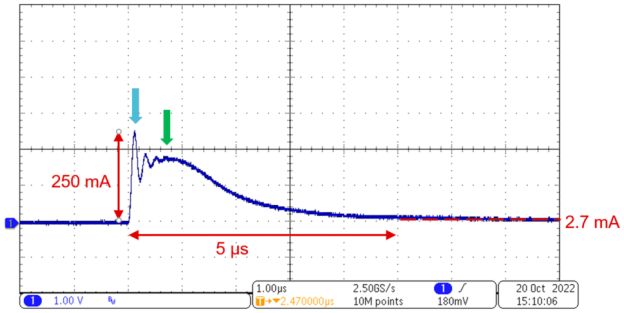

Figure 2. *Measured transient current at power up with decoupling capacitors installed.*

Recall from the **ADS1261** power-supply specifications in **Table 1** that the average current with the PGA disabled is 2.7 mA (typical) or 4.5 mA (maximum). However, the blue arrow in **Figure 2** points to a 250-mA transient spike that occurs when the **ADS1261** is initially powered. This transient is >90 times the typical current and >55 times the maximum current specified in the data sheet. Similar current spikes can occur when the ADC undergoes any change in state.

The green arrow in **Figure 2** identifies a second transient current required to charge up the decoupling capacitors. Under normal operating conditions, the decoupling capacitors store supplemental charge to provide extra current when transients occur. This extra charge helps maintain a steady supply voltage such that ADC operation remains unaffected. The capacitors must be charged up to the supply voltage from an uncharged state when the system is powered, however. Unpowered capacitors behave like a short at the instant the system powers up, resulting in a large inrush current. The magnitude of the inrush current increases as the value of the decoupling capacitor increases.

To measure only the transient current that the ADC requires, the second transient current test removed the recommended 10- and 0.1-µF decoupling capacitors from AVDD to ground in **Figure 1**. **Figure 3** shows the **ADS1261** transient current under these conditions.

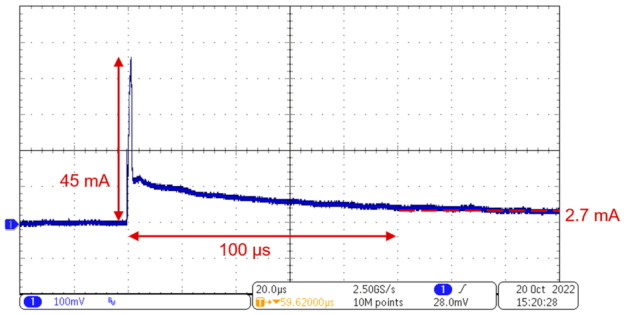

Figure 3. *Measured transient current at power up with decoupling capacitors removed.*

The 45-mA transient spike in **Figure 1** represents only the power-up current required by the ADC attributable to switching. As expected, the ADC-only transient is smaller compared to the 250-mA spike that occurred when the decoupling capacitors were installed. However, this reduced transient magnitude comes at the cost of a significantly longer time for the ADC to reach the steady-state current because the capacitors no longer provide any supplemental charge. Additionally, this 45-mA transient is still 10 times the maximum ADC current specification of 4.5 mA listed in **Table 1**.

I performed a third set of tests to verify that different functions can also cause transient current spikes. Enabling the **ADS1261** VREF was one such function that produced a spike. **Figure 4** shows the observed behavior of this transient current.

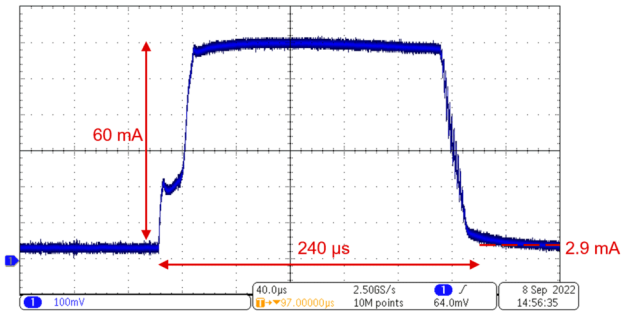

Figure 4. *Measured transient current with the ADS1261 VREF enabled.*

Recall from **Table 1** that the typical **ADS1261** VREF current is 0.2 mA. Operating the ADC with the PGA disabled (2.7 mA) and the internal VREF enabled should yield 2.9 mA of total current. However, the 60-mA measured transient current in **Figure 4** is >20 times the expected value. This transient largely results from the inrush current required to charge a filtering capacitor placed between the VREF output pin and ground.

One interesting characteristic of **Figure 4** is that the current demand remains constant at 60 mA for essentially the entire transient pulse. This behavior results from an inherent current limit designed into the **ADS1261** internal VREF, which helps protect the ADC in case the REFOUT pin shorts to ground.

I performed some additional function tests that did not show any measurable transient current, although I did not test all operating conditions. Also, I should note that this behavior is not limited to the **ADS1261**; it is possible to observe the transient currents documented in this article with all precision ADCs.

Power-supply circuit options

Transient currents can cause issues such as voltage droop that may lead to unstable ADC operation. Therefore, it is important to design power supplies to accommodate both average and transient current demand. Review the benefits and challenges of three different power-supply options:

- Low dropout regulators (LDOs). TI recommends using LDOs to power precision ADCs. LDOs offer many benefits, such as excellent noise performance; low voltage ripple; and a small, simple implementation. The most important benefit of an LDO is its ability to reliably maintain the output voltage during transients while also providing low quiescent current. For more information on how to select the best LDO for any application, see **Related Website** section below.
- Linear regulators. Linear regulators with standard dropout voltages can also be a good option if selecting an LDO is cost-prohibitive. Linear regulators can reliably maintain the output voltage during transients while also providing low quiescent current similar to LDOs. The challenge with linear regulators is that the dropout voltage is significantly larger, which can require specific voltage rails just to power these devices. Linear regulators also tend to come in larger packages because they are less efficient and must dissipate more heat. Additional heat can raise the temperature of a closed system, which can contribute to drift errors in precision systems.
- Shunt regulators. One of the most cost-effective power-supply options is a shunt regulator. The cost savings come at the expense of the additional complexity required to design a reliable power-supply circuit. As an example, a precision ADC requiring bipolar supply operation might use the **TLV431** – a low-voltage, adjustable shunt regulator – to generate ±2.5-V rails. You can use the **TLV431** for this purpose because it has a low VREF. However, one challenge with this regulator is that it can supply only a limited amount of current. The **TLV431** data sheet also requires a cathode current of ≥1 mA. These two restrictions limit the output-current capabilities of the standard setup shown in **Figure 5** and **Figure 6**.

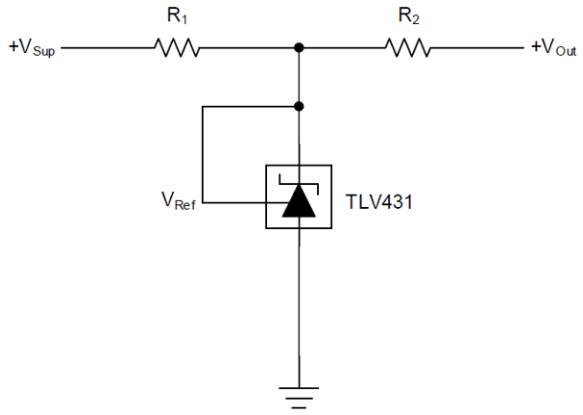

Figure 5. *Current-limited shunt regulator circuit with positive output.*

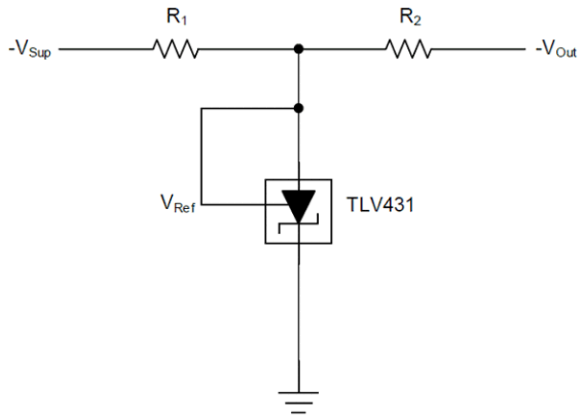

Figure 6. *Current-limited shunt regulator circuit with negative output.*

Figure 5 and **Figure 6** show that both the cathode current and the current supplied to the ADC must flow through resistor R1. This configuration limits the supply current to (VSUP – VREF) / R1, resulting in two design challenges. First, current flowing continuously through R1 consumes power even with no applied load. Attempting to reduce R1 to increase the available supply current also proportionally increases the static power dissipation. Second, the maximum current set by R1 generally cannot support the hundreds of milliamperes of transient current that the ADC requires. An inability to provide the necessary current causes the supply voltage to droop, and can lead to unstable ADC operation.

Mitigate these issues by adding two components to the circuit in **Figure 5** and **Figure 6**. **Figure 7** and **Figure 8** show a modified shunt regulator circuit that includes a transistor and a bias resistor, Rb.

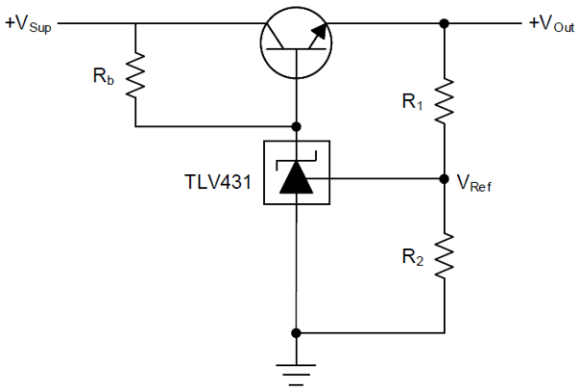

Figure 7. *Improved shunt regulator circuit with positive output.*

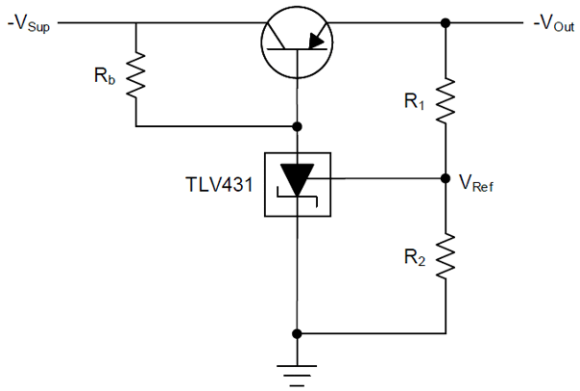

Figure 8. *Improved shunt regulator circuit with negative output.*

The power-supply circuit in **Figure 7** and **Figure 8** can provide more current compared to the system in **Figure 5** and **Figure 6** because the transistor eliminates any resistance between the supply input (VSUP) and output (VOUT). This new circuit can also maintain a cathode current of ≥1 mA by installing Rb instead of relying on R1. Resistors R1 and R2 therefore are only required to set the output voltage as per **Equation 1**.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) \times V_{ref} \quad (1)$$

For more information on how to use a voltage reference as a shunt regulator, see **Related Website** section below.

Low-power systems: Power down or power off?

Low-power DAQ systems often conserve energy by using different power-down methods. Some ADCs offer a power-down mode that helps reduce system power consumption by putting the device in a low-power state when it is not in use. The ADC data sheet then specifies the current consumption in this mode. Another popular power-saving technique is to simply turn off the power supply when the ADC is not in use and turn the power supply back on when needed. This method should result in no power consumption while the system is off.

The latter method is subject to the transient currents discussed in this article, however, because any capacitors must recharge every time the supply cycles. You can estimate how much current the system consumes when the supply is turned off by using the standard equations for charge (Q) and current (I), and then compare this value to the ADC data-sheet value in power-down mode.

For example, the **ADS1261** data sheet recommends 10- and 0.1-µF decoupling capacitors in parallel from AVDD to AVSS. The data sheet also specifies that AVDD must be 5 V. **Equation 2** and **Equation 3** calculate that the average current is 50.5 µA if the power supply cycles once per second:

$$Q = C \times V = 10.1\ \mu F \times 5\ V = 50.5\ \mu C \quad (2)$$

$$I = \frac{Q}{t} = \frac{50.5\ \mu C}{1\ s} = 50.5\ \mu A \quad (3)$$

where, C = 10.1 µF (10 µF + 0.1 µF), V = 5 V and t = 1 s.

Recall from the green highlighted section in **Table 1** that the **ADS1261** power-down current in power-down mode is only 8 µA (maximum). Comparing both options reveals that using the ADC power-down mode conserves >6 times more power relative to turning off the supplies. Therefore, it is important to consider the effect that transient currents can have on overall power consumption. Choosing to put the ADC in a power-down state can often be the more energy-efficient solution.

Related Website

- Download these e-books:
  - Texas Instruments: ***LDO Basics***
  - Texas Instruments: ***Tips and Tricks for Designing with Voltage References***
- Check out these TI E2E™ design support forums technical articles:
  - **How to Choose an LDO or Switching Regulator**
  - **How to Use a Voltage Reference as a Voltage Regulator**
- Texas Instruments: ***Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheets***
- Find an LDO for your next precision ADC design using the **LDO parametric search**

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