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How to use an ideal diode controller as a scalable input bypass switch in solar applications

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Introduction

In solar photovoltaic (PV) systems, module-level power electronics (MLPE) improve power-yield performance under certain conditions, especially in shade. Once considered a costly specialty category, MLPE is now one of the fastest-growing market segments in the solar industry. A solar power optimizer is one type of MLPE that optimizes the power output of the PV panel and increases efficiency.

Conventional solar power optimizers use a P-N junction diode or a Schottky diode for the bypass circuit. When high current flows through the diode, the high-power dissipation can cause severe thermal issues because of the diode's relatively high forward voltage drop. An improved method uses a metal-oxide semiconductor field-effect transistor (MOSFET) with a lower voltage drop than diodes to overcome the high-power loss.

Additionally, solar optimizers can now support higher input voltages – up to 150V transient with two PV panels in series – thanks to the efficiency improvements gained by lower conduction losses for a given power level, and lower system costs. In this article, we'll discuss a scalable bypass circuit solution using a floating-gate ideal diode controller. This circuit addresses challenges related to bypass switches with wide voltage support in solar power applications such as solar power optimizers, rapid shutdown and PV junction boxes.

What is a solar power optimizer?

Figure 1 illustrates a PV system with a solar power optimizer installed on an individual PV panel.

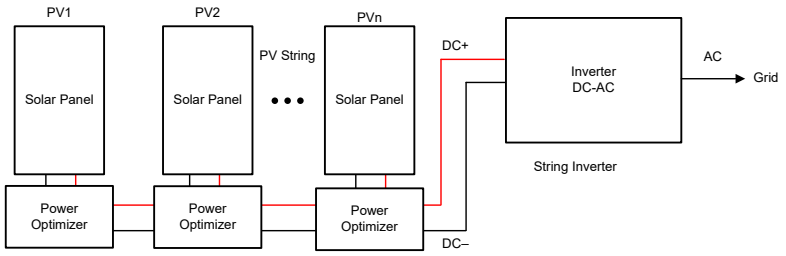

Figure 1. *PV system with a solar power optimizer.*

Think of a power optimizer as a compromise between a microinverter and a string inverter. It is installed on individual solar panels like a microinverter, but its function has nothing to do with converting DC to AC electricity. A power optimizer tracks the maximum power of each solar panel in real time and regulates the output voltage before sending it to the inverter. Therefore, the inverter can process much more electricity. The result is optimized power-yield performance for every single

solar panel, regardless of orientation to the sun, shade or even damage to one or more panels. Solar systems with power optimizers installed at each PV panel can be 20% to 30% higher in efficiency compared to one without an individual panel-level optimizer.

Output bypass function of a solar power optimizer

For high-power solar inverters, connecting multiple PV panels in series achieves a high DC input voltage going into the inverter input. Deploying the optimizers to the corresponding PV panels obtains the highest efficiency, as shown in **Figure 2**. The PV string is actually connected by the outputs of the optimizer. If any one of the solar panels fails, then the PV string voltage can collapse, as all of the PV panels are connected in series. An output bypass circuit provides a parallel path to the string current around the damaged optimizer. **Figure 2** shows how the bypass function works when one of the PV panels breaks.

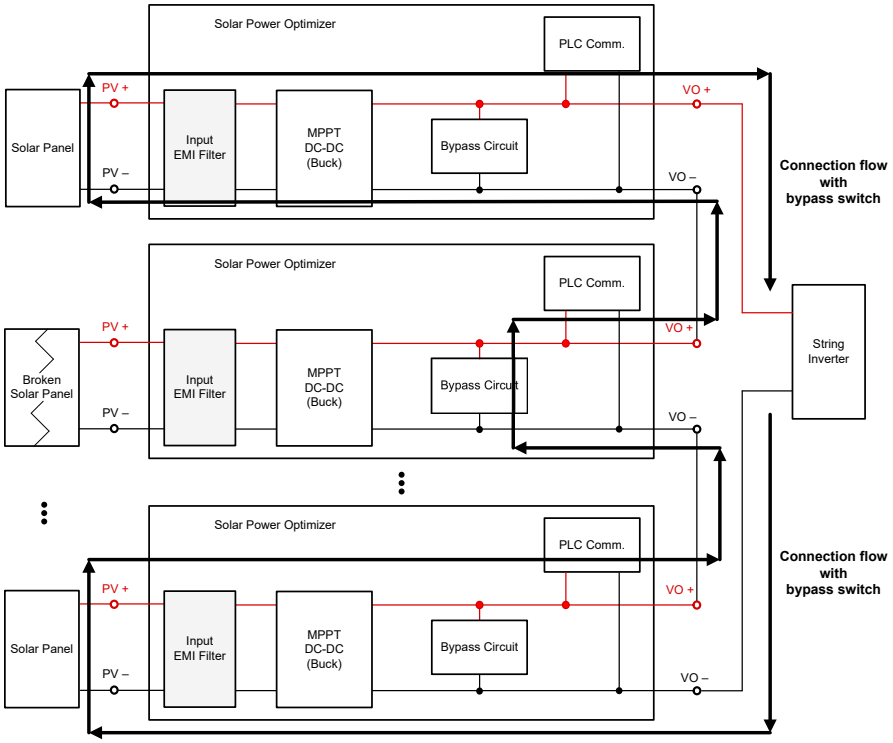

Figure 2. *Output bypass junction of a solar power optimizer.*

Output bypass circuit solutions

There are typically two kinds of solutions for the bypass circuit. The common way to achieve bypass functionality to use P-N junction diodes or Schottky diodes, as shown in **Figure 3**. It's low cost, easy to use and can achieve a very high reverse voltage based on the diode selected. There are drawbacks, however, such as a high forward voltage drop (0.5V to 1V), which causes higher power dissipation and larger printed circuit board requirements. In order to overcome the disadvantages of the bypass diode solution, using an N-channel MOSFET, which has a much lower voltage drop and lower power losses (because of low $R_{DS(on)}$), is an alternative. There are still some drawbacks, however:

- The MOSFET is not a stand-alone solution – it requires a control circuit to operate it as a switch, usually a microcontroller (MCU) with discrete MOSFET driver circuit.
- The MCU needs power from the PV panel. So if the PV panel is badly damaged or fully covered by

shadows or shade, then the MCU will not work and the MOSFET cannot turn on,

- In cases when the MCU fails, the MOSFET cannot be turned on, and the bypass path is through body diode of the MOSFET. But body diode of the MOSFET cannot withstand large currents and will accumulate high degrees of heat that can risk fire.

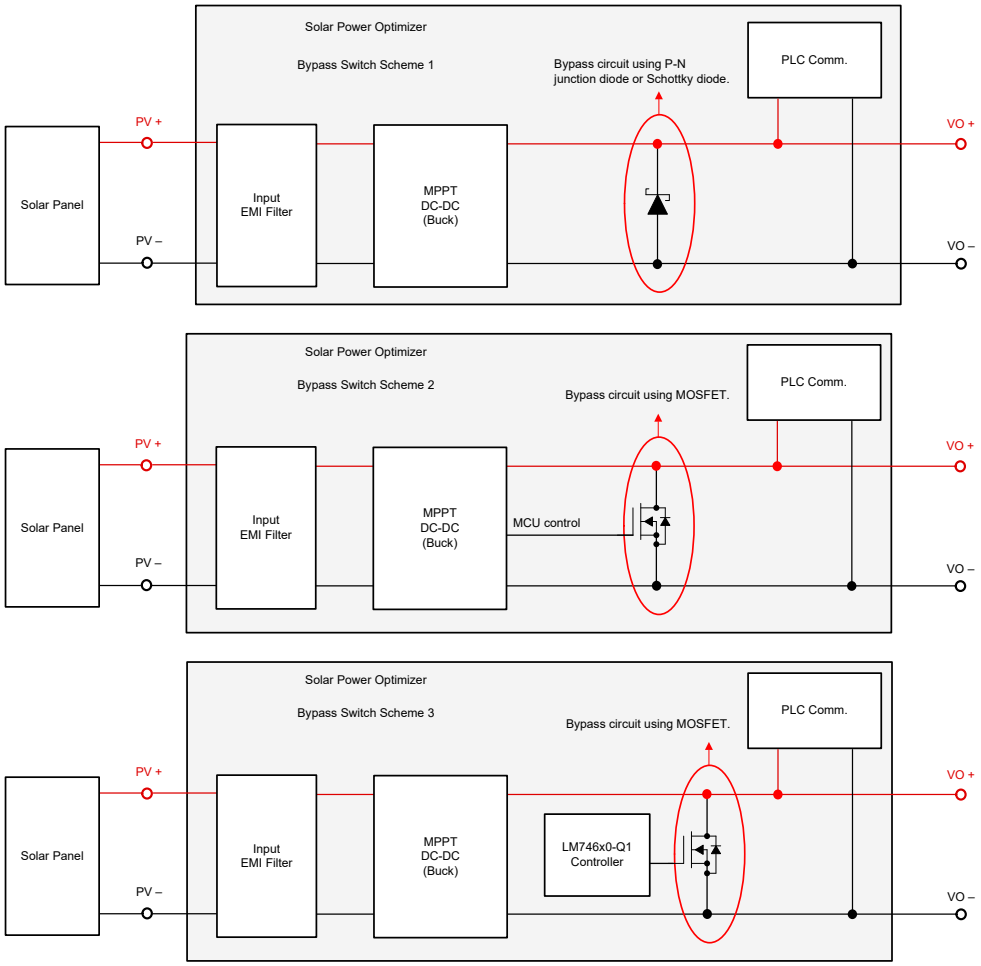

Figure 3. *Typical solutions when using a bypass switch in solar optimizers.*

An intelligent way to address the drawbacks of an MCU-based on or off control scheme is to use a stand-alone MOSFET controller that can work autonomously without any external intervention. The **LM74610-Q1** family of floating-gate ideal diode controllers from Texas Instruments provides a stand-alone, low-loss bypass switch solution by controlling the external N-channel MOSFET to emulate series diode behavior. These controllers have a floating gate-drive architecture that can operate with an input voltage as low as the MOSFET's body diode forward drop (approximately 0.5V).

However, as solar inverter power levels increase, and the adoption of higher-voltage PV panels increases, the bypass circuit has a few requirements to make it a better solution than traditional ones. It needs to work with a PV panel voltage ranging from 20V to 150V to make it scalable across multiple platforms, and it should be independent from other circuits.

A scalable bypass switch solution using a low-voltage ideal diode controller

The bypass circuit solution uses an ideal diode controller with a floating gate-drive architecture (such as the **LM74610-Q1**) to drive an external MOSFET and emulate an ideal diode as the bypass circuit so that it is independent from other circuits. Its floating gate-drive architecture can achieve a universal input range, as the gate drive does not respect to ground. In addition, a unusual advantage of this scheme is that it is not referenced to ground and thus has zero quiescent current.

When solar panels and solar equipment operate normally, the bypass MOSFET is off, and the reverse voltage equal to the maximum panel voltage appears from the cathode to the anode pins of the ideal diode controller. However, the reverse voltage (PV+ to PV–) from the cathode to the anode pins of the ideal diode controller can be very high as the PV panel and string transient voltage. In cases where the PV panels are used in series with a very large input voltage range, it can be challenging to design the maximum input voltage range for the bypass circuit. The maximum reverse voltage of the **LM74610-Q1** is limited to 45V transient. Thus, currently available ideal diode controller devices are not suitable for solar panels with a rated input voltage of 80V or 125V.

Adding a depletion MOSFET Q_D in the sense path to extend the reverse voltage range of the ideal diode controller sustains this voltage level for any range, as shown in **Figure 4**. The drain of Q_D connects to output PV+. The source connects to the cathode and the gate connects to the anode of the ideal diode controller.

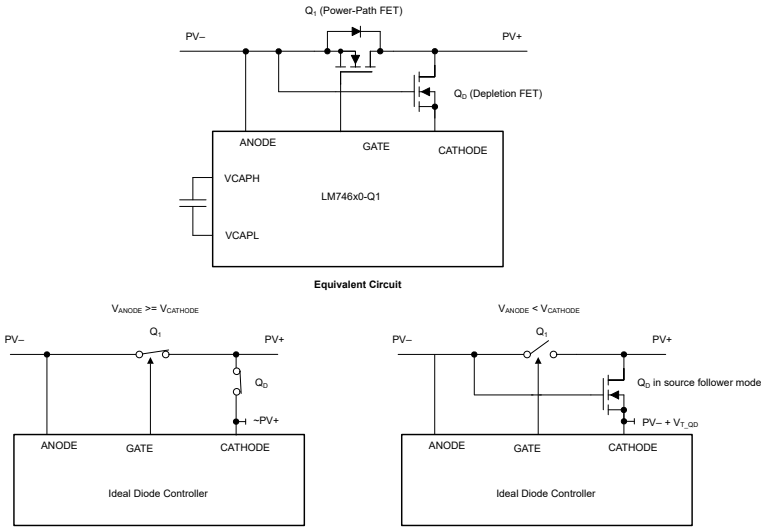

Figure 4. *Scalable bypass switch solution.*

Working principle of LM74610-Q1 reverse-voltage range extension

Depletion-mode MOSFETs are by default on when MOSFET V_{GS} is 0V, unlike enhanced-mode MOSFETs that require V_{GS} to be greater than the threshold voltage of the MOSFET. In order to turn off the depletion MOSFET, V_{GS} needs to be <0V (typical ranges are from –1V to –4V). To analyze the effect of the depletion-mode MOSFET in an ideal diode-sense path, let's look at device operation under these conditions:

- When V_{PV-} V_{PV+}: The ideal diode controller is in forward-condition mode, keeping both the power MOSFET Q_1 and depletion FET Q_D on. With these operating conditions, you can calculate the output voltage as $V_{OUT} = V_{IN} – (I_{D\_Q1}\ R_{DS(on)\_Q1})$, approximated to V_{PV+}.
- When $V_{PV-} < V_{PV+}$: The ideal diode controller is in the reverse current blocking condition, with MOSFET Q1 turned off. MOSFET Q_D is in regulation mode as a source follower, maintaining $V_{CATHODE}$ above V_{ANODE}, $V_{CATHODE} = V_{IN}(V_{ANODE})+ (V_{GSMAX})$. So the voltage across $V_{CATHODE}$ to V_{ANODE} is within the absolute maximum rating V_{GSMAX} of Q_D (usually <5V), which is far less than the maximum reverse voltage of 45V transient of the LM74610-Q1. The high reverse

voltage (V_{OUT} – V_{IN}) is sustained by the drain-to-source voltage (V_{DS}) of Q_D and Q_1.

Selecting the correct depletion MOSFET and power MOSFET depends on these points:

- Choose a V_{DS} rating of Q_1 and Q_D greater than the maximum peak input voltage.
- Select $R_{DS(on)}$ such that dissipation across the power-path MOSFET is lowest. The drain current (I_D) of the FET should be higher than the maximum peak current demanded by the output load. Selecting a depletion MOSFET with a drop of 50mV to 100mV across the power MOSFET at the full load current is a good starting point.
- $R_{DS(on)}$ can be in the hundreds of ohms range (the **LM74610-Q1**'s floating gate-drive architecture has a large impedance of cathode pin to ground, and the $I_{CATHODE}$ of the controller is in the microamperes range).

Figure 5 shows test results for a 60V bypass switch solution using the 40V **LM74610-Q1** controller.

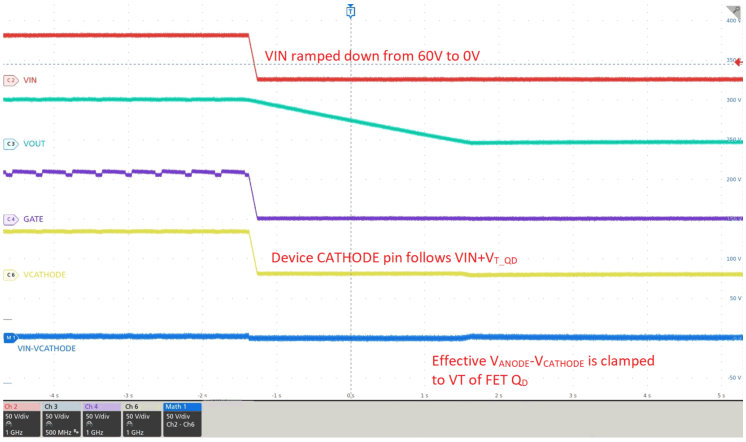

Figure 5. *Test results for a 60V bypass circuit with the LM74610-Q1 and depletion MOSFET.*

With properly scaled MOSFETs (Q1 and Q_D), the input voltage range can extend to the V_{DS} rating of the FETs.

This enables high-voltage designs using the same low-voltage controller. Also, extending the input voltage range can also be useful in enterprise, communication, power tool and high-voltage battery-management applications.

Conclusion

If PV panels or solar equipment connected in a series are broen or faulty, it is important to have a design in place to avoid hot spotting and/or voltage supply interruption. This responsibility commonly lies with the solar power optimizer or rapid shutdown. While standard rectifier diodes or Schottky diodes are the simplest solution to bypass the broken panel, they aren't preferred given thermal inefficiency. A floating-gate ideal diode controller along with an N-channel MOSFET offers less stand-alone loss than a bypass switch solution, and an additional system workaround with a depletion MOSFET offers a completely scalable solution to address the wide input voltage range of PV panels.

Additional resources

- **LM74610-Q1 Zero IQ Reverse Polarity Protection Smart Diode Controller Data Sheet**

Designing 4mA to 20mA loop-powered transmitters

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Introduction

In any process control system, sensor transmitters collate data from pressure and temperature to flow and level, and relay this information to the programmable logic controller (PLC) or distributed control system.

These transmitters depend on the 4mA to 20mA signal to transmit data to the controller. Despite the emergence of standards such as IO-Link and Profibus, 4mA to 20mA offers resiliency over long distances, reliability, immunity to noise, and universal compatibility with every PLC system.

In this article, I will provide an overview of the 4mA to 20mA transmitter structure, its operating principles, and design alternatives for implementing this transmitter type using catalog semiconductor products.

4mA to 20mA transmitter basics

4mA to 20mA transmitters are classified by power and number of wires: four, three and two wire. In this article, I will focus on the two-wire type.

The two-wire field transmitter in **Figure 1** forms a current loop by connecting to a field supply and analog input module. The first subsystem in the field transmitter is the sense subsystem, which connects to the physical sensor, conditions its output, and converts the signal to a digital code for processing, including linearization and calibration. The second subsystem is the transmit subsystem, which powers the transmitter by extracting power from the loop, sends process data by converting the digital signal back to an analog signal, and controls the loop current. The transmitter transmits the signal by regulating current within the loop, acting as a voltage-controlled current source.

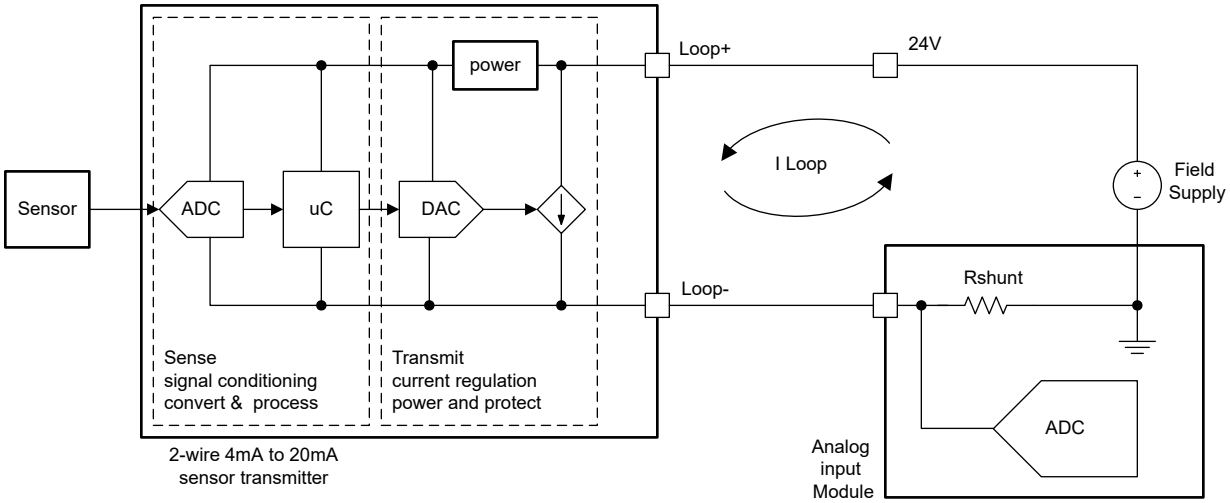


Figure 1. *Generic two-wire 4mA to 20mA sensor transmitter.*

In **Figure 2**, an N-channel P-channel N-channel (NPN) transistor sources and regulates the current, whose base is controlled through an amplifier driven by a digital-to-analog converter (DAC). A wide input voltage low-dropout (LDO) regulator powers the different components by stepping down the loop voltage to the transmitter supply level. You can use a voltage reference if the DAC does not have an integrated reference, while Highway Addressable Remote Transducer (HART)-enabled transmitters require a HART modem.

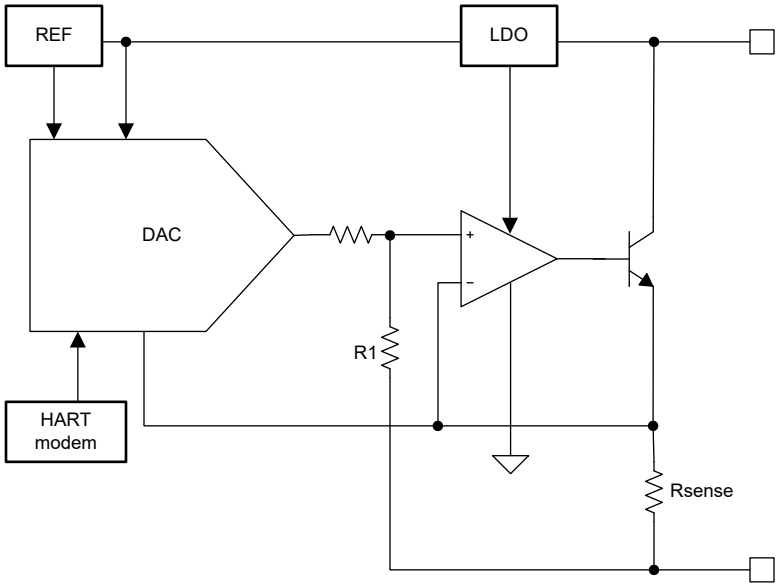


Figure 2. *Two-wire 4mA to 20mA transmitter circuit.*

The principle of operation is pretty simple: hold both inputs of the operational amplifier at virtual local ground. Whatever voltage R1 holds, Rsense also holds. With proper scaling, Rsense carries a scaled version of the R1 current. Given that Rsense current is nearly the whole current of the field transmitter (even for the sense part, not depicted in **Figure 2**), the DAC output controls the whole transmitter current. The NPN transistor and amplifier loop bypass the necessary current to complement any current used by the transmitter itself in order to achieve the required output current.

4mA to 20mA transmitter design aspects

4mA to 20mA transmitter design considerations include:

- Low-power operation.
- A small footprint.
- Accuracy and low noise over the entire industrial temperature range.
- HART protocol support.
- Low cost.

Design performance metrics

There are several transmitter performance metrics to evaluate:

Loop Compliance Voltage is the range of the loop voltage at which the transmitter is functioning. It is mainly determined by LDO limits and affected by series elements within the loop, including protection devices. The typical loop compliance voltage range is 12V to 36V.

Resolution is the number of distinct current output values that the transmitter can generate and is directly linked to the DAC native resolution. Commercial 4mA to 20mA transmitters have resolutions between 12 bits and 16 bits.

Linearity error is mostly determined by the DAC's integral nonlinearity, which is the maximum error (in least significant bits [LSBs]) over the whole output range.

Noise is measured by the root-mean-square (RMS) of output noise current. This noise can render some of the output level indistinguishable, reducing the effective resolution. Effective resolution in this context is a measure of noise performance. For 16-bit-resolution systems, effective resolution between 13 bits and 15 bits is expected, depending on signal bandwidth.

Accuracy measures the deviation of the current output from the ideal current value. This includes the RMS sum of offset errors, gain errors and nonlinearity error, plus the temperature drifts of these values. Total unadjusted error indicates the level of inaccuracy.

Dynamic performance includes signal bandwidth and transmitter stability. Bandwidth refers to the maximum current signal bandwidth that can be transmitted over the loop. This bandwidth is determined by the DAC

settling time and amplifier circuit bandwidth, as well as the transconductance of the bypass transistor. Using a degeneration resistor eliminates the dependence on variation of the transistor transconductance (g_m). Often, the amplifier circuit is externally compensated as well. Stability is related to the bandwidth of the loop and compensation capacitor values. Reducing capacitance on critical nodes of the loop will ensure stability. See the **DAC161S997 data sheet** for a detailed analysis of loop stability and its requirements. For HART-enabled transmitters, reducing the bandwidth with external components helps prevent interference with the HART signal.

Circuit protection protects the transmitter from abnormal conditions such as reverse loop polarity and surge events. Reverse polarity is blocked by a diode. If operating the transmitter with reverse polarity, use a rectifier bridge, as shown in **Figure 3**. Surge protection requires a transient voltage suppressor diode (such as the **TVS3301**) and passive elements to limit current during high-voltage events. These protection elements require some headroom during operation, and increase the minimum compliance voltage.

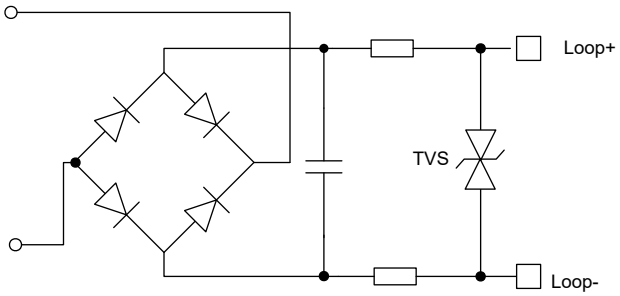


Figure 3. *Typical protection section for two-wire transmitter.*

Transmitter circuit implementations

The difference between the implementations for the block diagram in **Figure 2** lies in the integration approach. The bypass transistor is always a discrete component to enable better thermal management. All of the following implementations can support the HART protocol by adding a HART modem such as the **DAC8740H**.

Dedicated loop converter

One approach is to use a DAC such as the **DAC161S997 data sheet** with an integrated voltage reference and output amplifier. This solution consists of the DAC, a wide-input-voltage LDO and an NPN transistor, as shown in **Figure 4**. This implementation has 130µA of current consumption and excellent accuracy without calibration. The **DAC161S997** has diagnostic functions to detect current-loop errors in case of low supply or high current loads, and signals an error-low current below 4mA.

The design is simple, with a few external components to ensure loop stability and limit inrush current. This approach has a maximum operating temperature of 105°C.

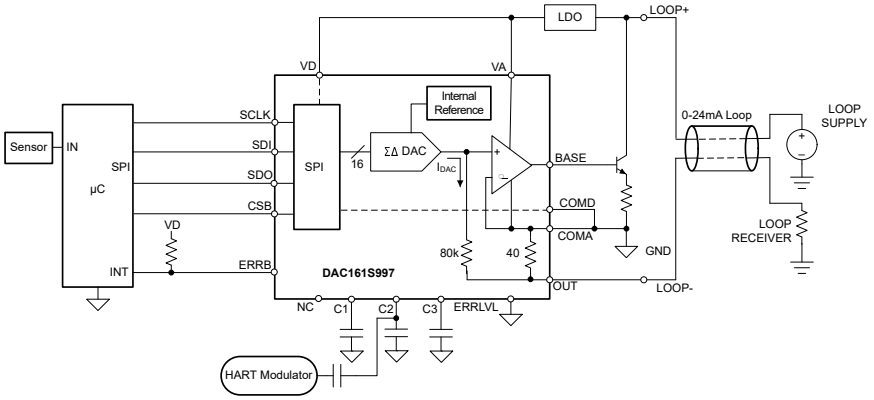


Figure 4. *Two-wire 4mA to 20mA transmitter using the DAC161S997.*

Loop transmitter device

Another implementation uses a low-power DAC such as the **DAC8551**, followed by a dedicated loop transmitter such as the **XTR115** with an integrated LDO, voltage reference and output amplifier. This approach minimizes noise and has less than 1% gain error.

There are a couple of limitations: the **XTR115** operating temperature is limited to 85°C, and the integrated LDO has a maximum input of 36V. As an alternative, the **XTR117** comes in a smaller package, consumes lower quiescent current, and operates at temperatures as high as 125°C. The **XTR117**'s integrated LDO works up to 40V. The **XTR117** does not integrate a voltage reference,

so counting an external reference, the solution becomes a three-device solution: an LDO, a DAC and a voltage reference, as shown in **Figure 5**.

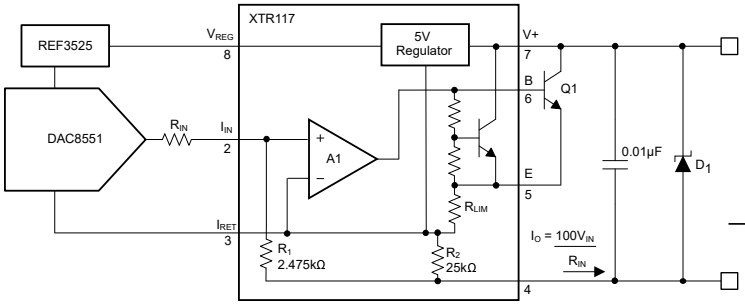


Figure 5. *Two-wire 4mA to 20mA transmitter using the XTR117.*

MCU integrated DAC

Cost-sensitive applications can employ an MCU with analog resources. The MSPM0G MCU enables a transmitter stage implementation including an integrated 12-bit DAC, internal reference and output amplifier. An LDO is the only external device needed, as shown in **Figure 6**. Given the implementation of analog functions on the MCU's digital process, they have relatively higher power consumption compared to their dedicated analog device counterparts. This approach is attractive for applications that require 11 bits of effective resolution at a very low cost. Using the VREF– pin as an internal reference negative pin instead of ground can improve performance. Separating the VREF– pin isolates digital noise from the analog reference.

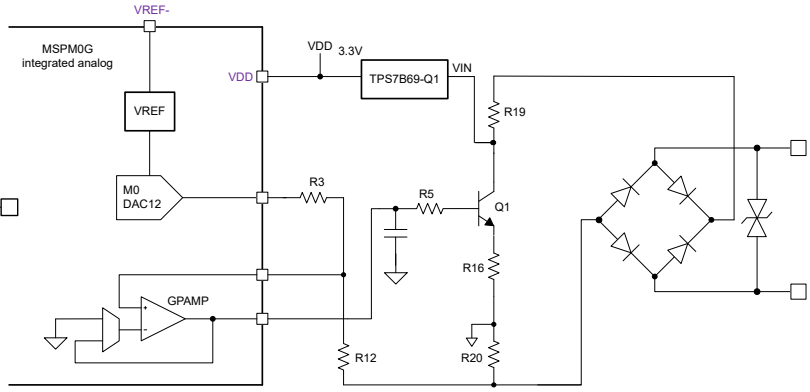


Figure 6. *Two-wire 4mA to 20mA transmitter implemented using the MSPM0G.*

PWM-based DAC

A more generic approach using an MCU (without an integrated DAC) is to rely on pulse-width modulation (PWM) to generate DAC outputs. A simple PWM DAC has a resolution of 10 bits to 12 bits. However, it is possible to realize a 16-bit resolution DAC with more advanced techniques such as two-path PWM and active ripple suppression.

To achieve a high effective resolution, the PWM signals are buffered using voltage reference-powered logic gates; the MCU needs proper bypassing to avoid digital noise injection into the loop current. The implementation depicted in **Figure 7** is low power, stable over temperature, and achieves greater than 13 bits of effective resolution at a very low cost.

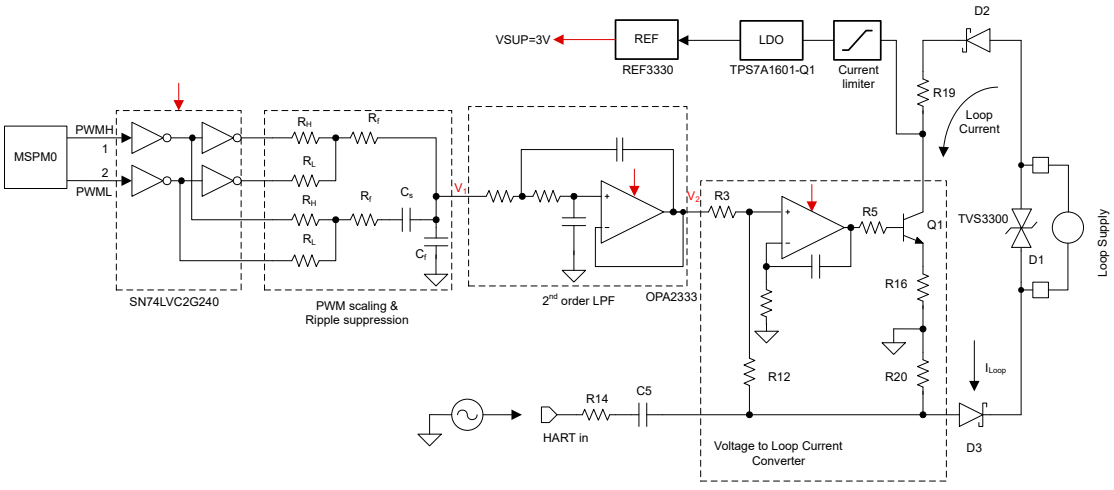


Figure 7. *Two-wire 4mA to 20mA transmitter implemented using a PWM DAC.*

Stand-alone low power DAC

Using a low-power, stand-alone DAC to realize a 4mA to 20mA transmitter such as the **AFE88101** in **Figure 8** achieves the best resolution and linearity performance. To reduce power further, a low-power voltage reference such as the REF35125 can reduce current down to 180µA. Additionally, the **AFE88101** has extensive diagnostic features, including a 12-bit ADC and a defined fail-safe mode.

The **AFE881H1** is pin-to-pin compatible with the **AFE88101**, with an integrated HART modem for a compact HART-enabled transmitter. The **AFE881H1** has low current consumption when HART is enabled. A HART modem typically consumes 10µA during operation, making it the device of choice for low-power, HART-enabled transmitters. Another feature of the **AFE88101** is compatibility with 1.8V logic to allow low-voltage digital operation and reduce power further on the MCU input/output side, as well as reducing electromagnetic emissions.

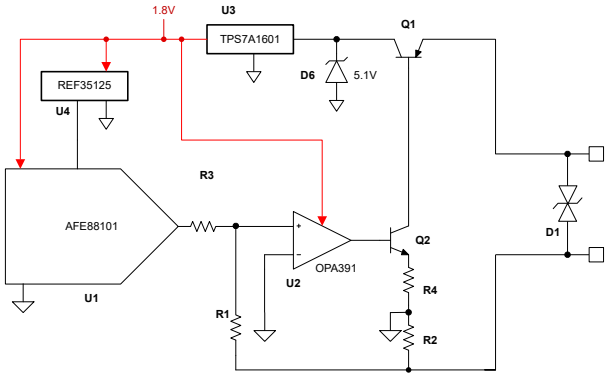


Figure 8. *Two-wire 4mA to 20mA transmitter implemented using the AFE88101.*

A lower-cost variant with the **DAC8311** DAC, LDO and external low-power reference runs with 130µA of current and still achieves reasonable performance.

Implementations Comparison

Table 1 and **Table 2** show each of the implementations, their suggested bill of materials (BOM) and their expected performance. The performance numbers are based on limited measurements.

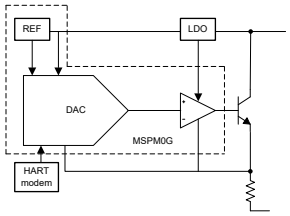
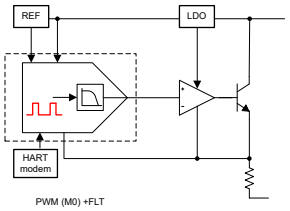
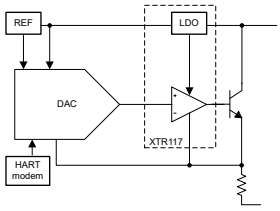
	MSPM0 DAC12	PWM using M0	XTR117
			
BOM	MSPM0G, TPS7B69, DAC8740H	TPS7A1601, REF3330, TLV2333, DAC8740H	XTR117, DAC8551A, REF3525
Compliance (volts)	40	60	40
Resolution (bits)	12	16	16
Linearity (LSBs)	2	<6	8
Effective resolution (bits)	11	13.4	14
Accuracy	1% full scale, 6uA	1% full scale, 6uA	0.7% full scale, 20uA
Current (µA)	425	240	440
Temperature (°C)	125	125	105
Advantages	Low cost	Low cost, high resolution, low power	high resolution

Table 1. *Design options for a 4mA to 20mA transmitter, suggested BOM and performance (MSPM0 DAC12, PWM using M0, XTR117).*

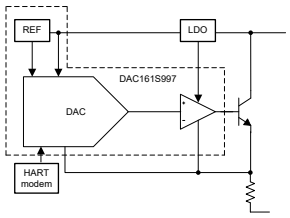
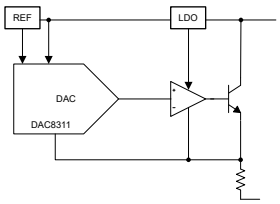
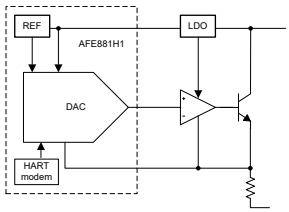
	DAC161S997	DAC8311	AFE881H1
			
BOM	DAC161S997, TPS7A1601, DAC8740H (1)	DAC8311, REF3525, OPA391, TPS7B69, DAC8740H	AFE88101 (1), REF35125, OPA391, TPS7A1601
Compliance (volts)	60V	40	60
Resolution (bits)	16	14	16
Linearity (LSBs)	5	4	4
Effective resolution (bits)	13.4	13.4	16
Accuracy	0.01%, 1uA	0.15%	0.07%
Current (µA)	130	130	180 (240 w/intREF)
Temperature (°C)	105	125	125
Compliance (volts)	Ultra-low power, high resolution, high accuracy	Ultra-low power, low cost	high resolution and accuracy, low power, low voltage

Table 2. *Design options for a 4mA to 20mA transmitter, suggested BOM and performance (DAC161S997, DAC8311, AFE881H1).*

(1) The DAC8740 has maximum power-down current of 180µA, and about 300µA when active with a crystal oscillator. The AFE881H1 HART modem, however, consumes 10µA on average. Add the corresponding current if enabling HART.

Conclusion

This selection process can help you decide the correct implementation when designing a 4mA to 20mA transmitter:

- If you are building a safety system, and need the highest accuracy and lowest noise performance, or looking for a HART-enabled transmitter with power below 200µA, the **AFE88101** and **AFE881H1** should be your first choices.
- The **DAC161S997** implementation offers the lowest possible power and footprint, followed by the **DAC8311** implementation, followed by the **XTR117** implementation if prioritizing performance over power consumption.
- For the lowest cost, choose the MSPM0G implementation. If its performance is not satisfactory, the next cost-optimized solution would be the PWM solution.

Related websites

- **4mA-20mA Current Loop Transmitter Reference Design**
- **Dual Sensor Measurement Using Single Current-Loop with FSK Modulation Reference Design**
- **2-wire, 4mA-20mA Transmitter, EMC/EMI Tested Reference Design**
- **High-Performance 16-bit PWM to 4mA to 20mA DAC for Field Transmitters**
- **Designing High-Performance PWM DACs for Field Transmitters**
- **Ultra-Low-Power, Low-Voltage, 2-Wire, 4mA to 20mA Loop Transmitter Using AFE881H1**
- **Highly Accurate, Loop-Powered, 4mA to 20mA Field Transmitter With HART Modem Reference Design**

How anti-aliasing filter design techniques improve active RF converter front ends

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Introduction

Active analog-to-digital (ADC) front ends using a fully differential amplifier (FDA) can offer a host of advantages, such as better impedance matching, pass-band flatness and signal gain. However, if you require only a portion of the ADC's band for your next design, it might be necessary to use an anti-aliasing filter (AAF) between the output of the FDA and the input of the ADC. An AAF will yield better signal-to-noise (SNR) performance and lower spurious or spurious-free dynamic range (SFDR) within your frequency band requirements.

With any kind of AAF filter constructions, you will have several trade-offs to consider during the implementation process: filter order and topology, or whether you will need back termination or series resistances to enhance the interface between the FDA and the ADC. In this paper, I'll discuss these AAF nuances and how to circumvent any huddles you might encounter in your next design.

AAF design approach

Assuming that you have decided on the correct FDA for your application and whether to use either a low-pass or band-pass filter in order to achieve optimum performance (bandwidth, SNR and SFDR) in front of the ADC, follow these three steps:

1. Understand the amplifier's characterized load impedance (RL). In order for the amplifier to perform at its best, the amplifier should "see" the correct DC load or RL listed in the data sheet for optimum performance. This is the characterized impedance typically found at the top of the specification tables.
2. Determine a starting point for the correct amount of output series resistance to use closest to the amplifier's outputs. This helps prevent unwanted peaking in the pass band. You'll also typically find this information in the FDA's data sheet - **LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifie Data Sheet**.
3. Determine whether to use one or more external parallel resistors to back-terminate the input to the ADC, and the starting value of the input series resistance to isolate the ADC from the filter. These series resistors also help reduce unnecessary peaking in the pass band and "kickback" commonly found in unbuffered ADCs.

Figure 1 shows an example of the specification table.

LMH5401

SBOS710D – OCTOBER 2014 – REVISED FEBRUARY 2018 www.ti.com

6.5 Electrical Characteristics: V_S = 5 V

at T_A = 25°C, VS+ = 2.5 V, VS– = –2.5 V, V_{CM} = 0 V, R_L = 200-Ω differential, G = 12 dB (4 V/V), single-ended input, differential output, and R_S = 50 Ω, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL(2)
AC PERFORMANCE							
GBP	Gain bandwidth product	G = 30 dB (32 V/V)		8		GHz	C
SSBW	Small-signal, –3-dB bandwidth	V_O = 200 mV_{PP}		6.2		GHz	C
LSBW	Large-signal, –3-dB bandwidth	V_O = 2 V_{PP}		4.8		GHz	C
	Bandwidth for 0.1-dB flatness	V_O = 2 V_{PP}		800		MHz	C

Figure 1. *Electrical specification table excerpt from the LMH5401 data sheet, where RL = 200Ω.*

The generalized circuit shown in **Figure 2** and filter parameter list in **Table 1** apply to most high-speed differential FDA and ADC interfaces; you can use both as a basis for the AAF design.

Although not every filter construction will be exactly the same, **Figure 2** can serve as a blueprint on how to kick-start your design. Using this design approach will tend to minimize the insertion loss of the filter by taking advantage of the relatively high input impedance of most high-speed ADCs and the relatively low output impedance of the driving source (the FDA).

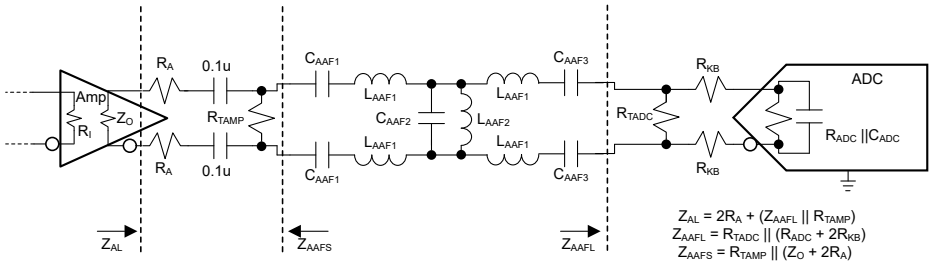

Figure 2. *Generalized FDA and ADC interface with a band-pass filter.*

Symbol	Parameter description
R_i	Amplifier input impedance
Z_o	Amplifier output impedance
R_A	Series output resistance located near the amplifier's outputs
R_{TAMP}	Back-termination resistance near the amplifier outputs
C_{AAF1}	First AAF capacitor
L_{AAF1}	First AAF inductor
C_{AAF2}	Second AAF capacitor
L_{AAF2}	Second AAF inductor
C_{AAF3}	Third AAF capacitor
R_{TADC}	Back-termination resistance near the ADC inputs
R_{KB}	Series kickback resistor located near the ADC's inputs
Z_{AL}	Aggregate load impedance as seen by the amplifier
Z_{AAFS}	Aggregate source impedance of the AAF
Z_{AARL}	Aggregate load impedance of the AAF

Table 1. *Filter parameter definitions.*

AAF design process and parameters

The basic AAF design process and guidelines are:

1. Set the external ADC termination resistor (R_{TADC}) appropriately. This helps the AAF realize a "real" impedance over its desired frequency response.
2. Select R_{KB} based on experience or the ADC data sheet recommendations; typically, this will be between 5Ω and 50Ω.
3. Use **Equation 1** to calculate the filter load impedance so that the aggregate parallel and series combination of R_{TADC}, R_{KB} and R_{ADC} is between 100Ω and 400Ω. See my recommendation in the previous section.

$$Z_{AAFL} - R_{TADC} \parallel (R_{ADC} + 2R_{KB}) \quad (1)$$

4. Select the amplifier external series resistor (R_A). This is typically between 5Ω and 50Ω. R_A helps dampen the amplifier output response and reduce unnecessary peaking in the pass band.
5. Use the calculated Z_{AAFL} so that the total load seen by the amplifier (Z_{AL}) is optimal for the particular differential amplifier chosen. See Step No. 1 above in the AAF Design Approach Section and use **Equation 2**:

$$Z_{AL} = 2R_A + Z_{AAFL} \quad (2)$$

   Keep in mind that ZAL is the FDA's characterized $_{RL}$; therefore, using too high or too low a value can have an adverse effect on the amplifier's linearity.
6. Calculate the filter source resistance using **Equation 3**:

$$Z_{AAFS} = Z_O + 2R_A \quad (3)$$

7. Using a filter design program, design the filter using the same source and load impedances, if possible, Z_{AAFS} and Z_{AAFL}. This helps reduce the amount of loss in the filter. Any mismatch between the input/output impedance has a loss of 10*log(input Z/output Z). For example, with an input impedance of 50Ω and an output impedance of 200Ω, the loss of the filter is –6.0dB or 10*log(50/200). Also, using a bandwidth that is about 10% more or higher than the desired bandwidth of the application will ensure that the intended bandwidth is covered per the application, and help overcome any second- and third-order parasitic losses unrealized during the filter implementation process.

   After running a few preliminary simulations, give the circuit a quick review for the following items:
8. The value of $C_{AAF2\ \&\ 3}$ should be sufficiently big relative to C_{ADC}, which minimizes the sensitivity of the filter to variations in C_{ADC}.
9. The ratio of Z_{AAFL} to Z_{AAFS} should not be more than 6-to-7, so that the filter is within the limits of most filter tables and design programs. Ideally, they should be the same to minimize loss, but this is not usually possible.
10. Try to use a value of C_{AAF2} in the few picofarads range to minimize sensitivity to parasitic capacitance and component variations.
11. Inductors L_{AAF1} and L_{AAF2} should be reasonable values and in the nanohenries range.
12. The value of C_{AFF2} and L_{AAF2} should be reasonable values; select these two parameters to optimize the filter's center frequency. Sometimes circuit simulators can make these values too low or too high. To make these values more reasonable, simply ratio these values with better standard-value components that maintain the same resonant frequency.
13. Use 0201 package styles if possible when designing in the gigahertz range to minimize second- and third-order parasitic effects that could disrupt the filter character shape or outline.

In some cases, the filter design program may provide more than one unique solution, especially with higher-order filters. Always choose the solution that uses the most reasonable set of component values. For filter configurations that end with a shunt capacitor, take the ADC's internal input capacitance into consideration as

well. You may need an iteration or two to set the filter pole and ultimate bandwidth correctly.

AAF design trade-offs

The parameters in this interface circuit are very interactive; therefore, it is almost impossible to optimize the circuit for the primary specifications (bandwidth, bandwidth flatness, SNR, SFDR and gain) without small trade-offs. However, you can minimize bandwidth peaking, which often occurs at the tail end of the bandwidth response, by varying R_A, R_{KB}, or both; either can have a net positive or net negative affect on AAF bandwidth performance.

Notice in **Figure 3** how the pass-band peaking is enhanced or flattened as the value of the FDA's output series resistance (R_A) changes (the blue dashed curves). As the value of this resistance decreases, there is more signal peaking, and the amplifier can drive the signal less to fill the ADC's full-scale input range at the cost of the pass-band flatness response near the edge of the AAF frequency response.

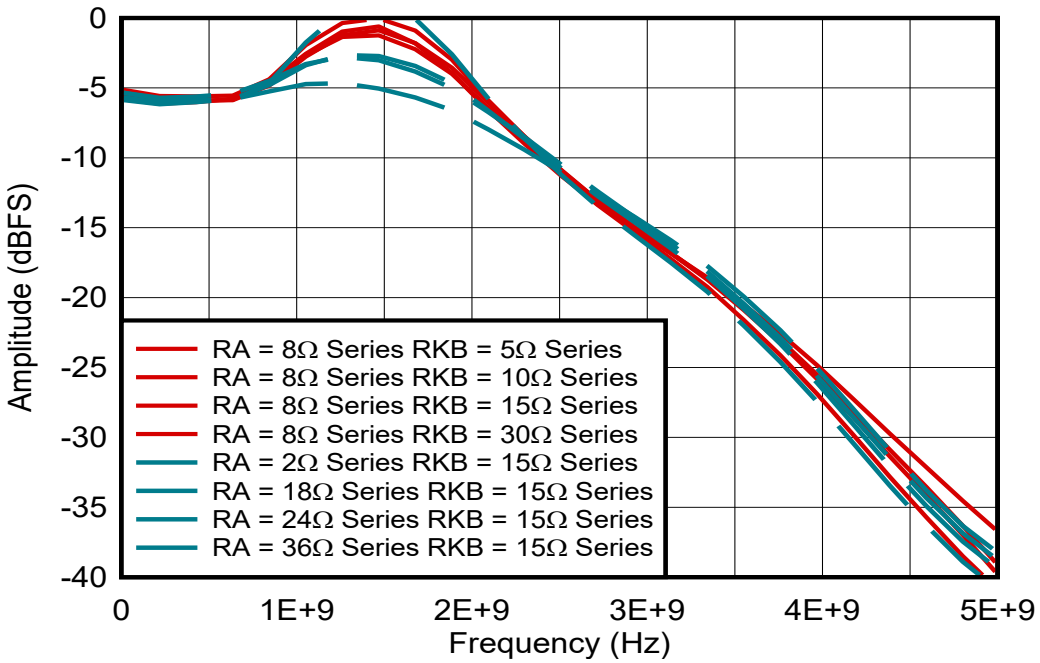

Figure 3. *Pass-band flatness performance vs. RA and RKB variations.*

The value of R_A could also affect SNR performance. Smaller values, while enhancing bandwidth peaking, tend to decrease the SNR because of the increased bandwidth and unwanted noise.

It's also important to select the R_{KB} series resistor on the ADC inputs to minimize distortion caused by any residual charge injection from the internal sampling capacitor within the ADC. However, increasing this resistor also tends to enhance or reduce bandwidth peaking as well, depending on the filter topology.

When optimizing for the AAF's rolloff frequency, varying C_{AAF2} by a small amount allows you to correct for optimal frequency coverage for the application.

Normally, determining the value of the ADC input termination resistor, R_{TADC}, makes the net ADC input impedance look near typical of most amplifier characteristic load (R_L) values. Selecting too high or too low a value for R_{TADC} can have an adverse effect on the amplifier's linearity, which will then be reflected in the overall SFDR signal-chain lineup.

AAF design example

The design example circuit shown in **Figure 4** is a wideband low-pass receiver front end based on the Texas Instruments (TI) **TRF1208**, a 10MHz to 11GHz, 3dB-bandwidth single-ended to differential amplifier and the TI **ADC12DJ5200RF**, a radio frequency (RF) sampling 12-bit dual-channel 5.2GSPS ADC. I optimized the third-order Butterworth AAF based on the performance and interface requirements of the amplifier and ADC; the total insertion loss caused by the filter network and other components was less than 6dB. In this AC-coupled design, the 0.1µF capacitors block the common-mode voltages between the amplifier, its termination resistors, and the ADC inputs.

The 10MHz to 11GHz **TRF1208** differential amplifier accepts a single-ended input and converts it to a differential signal operating at a gain of 16dB to compensate for the insertion loss of the filter network, providing an overall signal gain of +7.8dB.

An input signal of –6.8dBm produces a full-scale 800mV peak-to-peak differential signal at the ADC input.

The overall circuit has a bandwidth of 2.34GHz with a pass-band flatness of <3dB. The SNR and SFDR measured with a 534MHz analog input frequency are 52.5dBFS and 71.4dBFS, respectively. The sampling frequency is 5.2GSPS, thereby creating a wideband low-pass filter covering the entire first Nyquist zone between 10MHz and 2.5GHz. Figure 4 shows the values chosen for the final filter passive components (after adjusting for actual circuit parasitics).

The AAF was designed as a third-order Butterworth filter using a standard filter design program with a differential source impedance (Z_{AAFS}) of 39Ω (2 ´ 18Ω + 3Ω), a differential load impedance of 103Ω (Z_{AAFL}) and a cutoff frequency of 2.4GHz. Because of the higher values of series inductance required in simulation, I decreased these inductors to 3nH in order to account for the inherent trace inductances in the layout and proportionally increased the initial 1.8pF capacitors to ground in the simulations to 2.2pF, thereby helping maintain appropriate rolloff around the 2.4GHz requirement.

The **TRF1208** was not back-terminated in this case in order to achieve net performance, and the net differential impedance load was 139Ω (Z_{AL}). Implementing the 18Ω series resistors isolated the filter capacitance from the amplifier outputs. For further insight on the FDA's impedances, you can**download the S-parameters** .

Installing the 15Ω resistors in series with the ADC inputs isolated the internal switching transients from the filter and the amplifier, as well as providing the necessary characterized loading to the FDA.

I used the ADC's 100Ω input impedance per the data sheet. For further insight on the ADC's impedances, **download the S-parameters**.

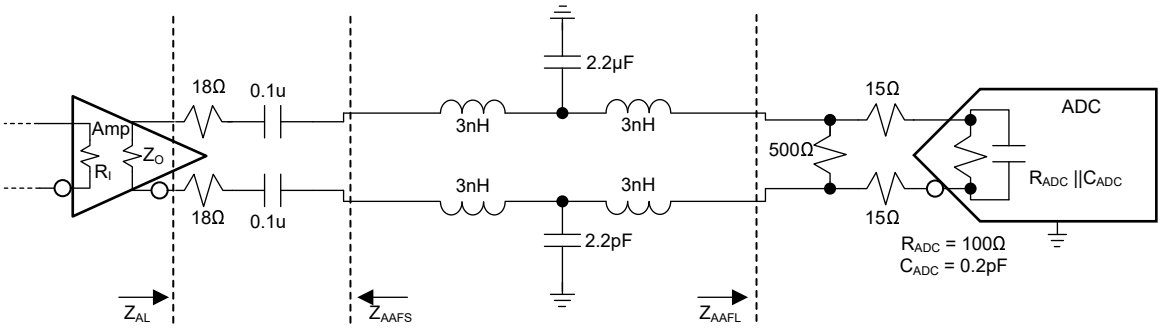

Figure 4. *FDA, AAF, ADC wideband receiver front-end design (simplified schematic).*

Table 2 summarizes the measured performance of the system, where the total insertion loss of the network is approximately 5.8dB.

Performance specs at –1dBFS (FS = 0.8V peak to peak), sample rate = 5.2GSPS, JMODE 3	Final results
Cutoff frequency	2,340MHz
Pass-band flatness (10MHz-2.2GHz)	<3.0dB
SNR full scale at 534MHz	52.5dBFS
SFDR at 534MHz	71.4dBFS
H2/H3 at 534MHz	–71.4dBFS/–73.0dBFS
Overall gain at 534MHz	+7.8dB
Input drive at 534MHz	-12.8dBm (–6dBFS)

Table 2. *Measured performance of the circuit.*

Figure 5 shows the resulting combined FDA, AAF and ADC signal chain's frequency response.

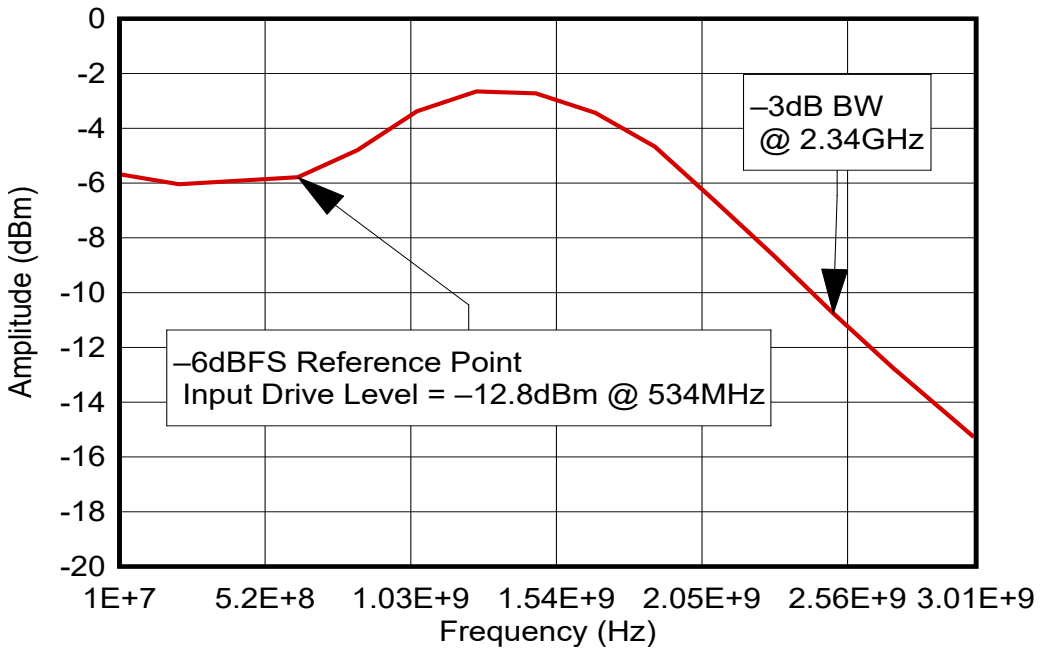

Figure 5. *Pass-band flatness performance vs. frequency.*

Figure 6 shows the SNR and SFDR performance versus frequency, respectively.

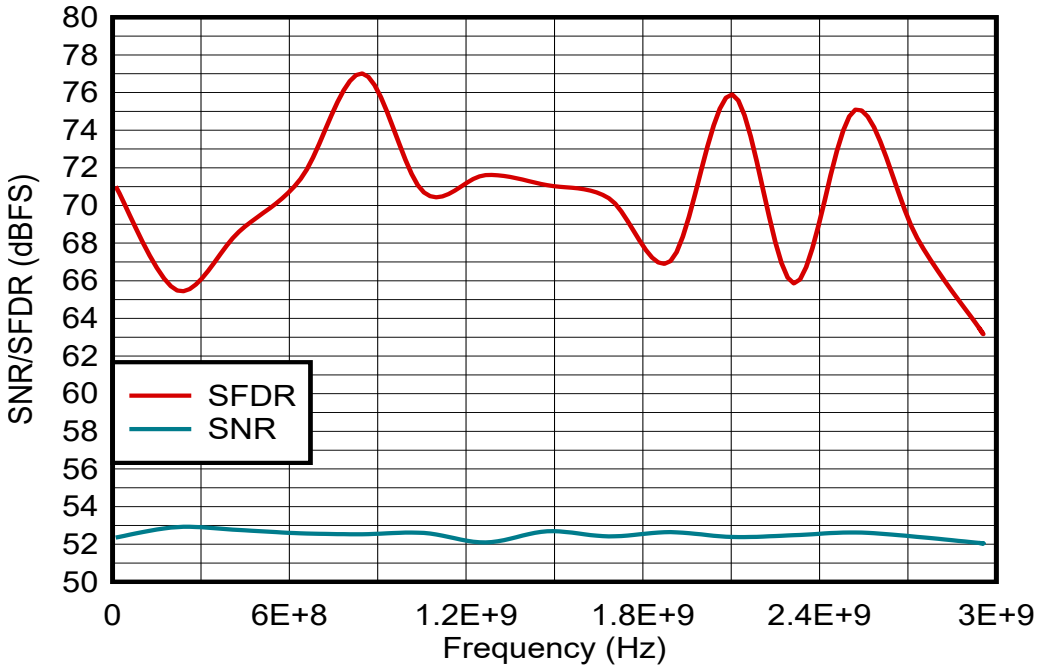

Figure 6. *SNR/SFDR performance vs. frequency, sample rate = 5.2GSPS.*

AAF design conclusion

Understanding all of the different factors, parameters and trade-offs involved in designing an AAF between an FDA and RF ADC can be more difficult than it seems. The design example described in this article gives each parameter equal weight; therefore, the values chosen represent the interface performance for all of the design characteristics. In some designs, you may choose different values to optimize SFDR, SNR or input drive level depending on system requirements. Keep all of these necessary points in mind so that your next AAF doesn't go resonant.

Additional resources

1. Keysight ADS Simulation Software: **https://www.keysight.com/us/en/products/software/pathwave-design-software/pathwave-advanced-design-system.html**.
2. Ansys/Nuhertz Technologies, Filter Solutions Design Program: **https://www.ansys.com/products/electronics/ansys-nuhertz-filtersolution** .
3. Reeder, Rob. 2022. "**Evaluating high-speed RF converter front-end architectures**." Planet Analog, April 7, 2022.
4. Reeder, Rob. 2022. "**A close look at active vs. passive RF converter front-ends**." Planet Analog, January 24, 2022.
5. Bowick, Chris. 1997. "RF Circuit Design." Boston, Massachusetts: Newnes.

Impact of voltage reference noise on ADC ENOB and noise-free resolution

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Introduction

Multiple systems ranging from thermostats to flight control employ an analog-to-digital converter (ADC) to capture real world analog signals which will be processed in the digital domain and take necessary actions based off of the digital results. Each ADC specifies a number of bits to represent the various digital levels it can produce. For a given constant ADC input, the output of the ADC is not a constant digital value due to various errors in a typical signal chain. Thus, it is important to consider the effective number of bits (ENOB) or the noise-free resolution of the signal chain for better comparison and to also extract maximum information from the captured data. Higher precision calls for higher ENOB and noise free resolution.

Typically, signal-to-noise ratio (SNR), total harmonic distortion (THD) and noise of the system play an important role in ENOB calculation. For multiple systems like field transmitters or test and measurement applications, DC input signal accuracy and precision is critical. Therefore, the noise specification becomes most critical. The voltage reference used with an ADC is a critical component in the signal chain that can impact the precision and accuracy.

The impact of the voltage reference on ADC noise

While it is possible to remove some noise by filtering, you cannot realistically filter out noise at low frequencies. In a voltage reference, it is also not possible to filter out flicker noise (which is noise from 0.1Hz to 10Hz) without having a major impact on signal chain performance because of the size of the resistor-capacitor filter components you'll need. Therefore, noise will almost always be present in your system.

In addition to the voltage reference noise, there will be noise from the ADC itself and the ADC driver. Each one of these components contributes noise to the circuit that generates a digital signal. Figure 1 is a simplified block diagram of this circuit.

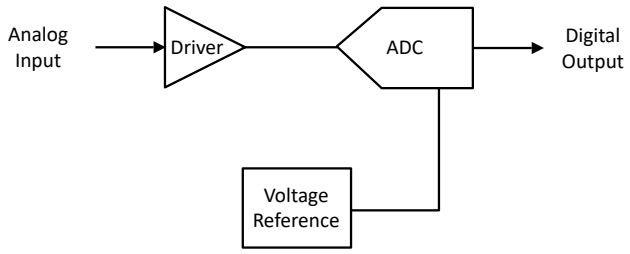

Figure 1. *Generic ADC circuit configuration with an external voltage reference.*

Equation 1 expresses the total noise of this circuit as:

$$\text{Total Noise} = \sqrt{\text{Noise}_{\text{Driver}}^2 + \text{Noise}_{\text{ADC}}^2 + \text{Noise}_{\text{VREF}}^2} \quad (1)$$

The amount of noise present in your circuit is important to know when determining your system's ENOB. In general, selecting low-noise devices is essential to a low-noise design.

In this article, I'll focus on not only voltage reference selection, but other data processing choices that can help you maximize ADC performance.

The impact of the voltage reference on THD

Repeated sampling of the voltage reference pin can cause current transients to appear that may only be separated by a few nanoseconds. However, for an ADC, the external reference must settle or recharge by the end of the sample phase in order to avoid a large gain error. Slowing the sampling speed could fix this issue, but that is not always an option. Typically, the more precise the ADC, the more current draw required on its reference input. If a voltage reference does not have high-enough bandwidth, or has too high of an output impedance, it will not be able to recharge the reference input of the ADC. This will cause a voltage droop, leading to gain error and lower ENOB.

For this reason, a high-bandwidth, low-output-impedance buffer external to the voltage reference is sometimes necessary to increase the THD of the ADC and meet the data-sheet specifications for distortion and ENOB. Some ADCs have an internal voltage reference buffer, but not all do. **Figure 2** shows where to add an external buffer to increase the THD of your circuit.

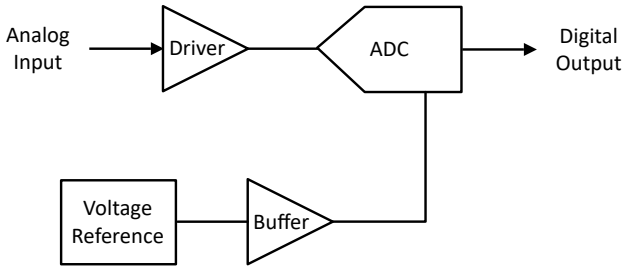

Figure 2. *Generic ADC circuit configuration with an external voltage reference and reference buffer.*

How voltage reference noise and THD affect the ENOB

ENOB measures how the AC characteristics of your circuit affect your ADC resolution. The noise and THD of your circuit are represented by a term known as signal-to-noise ratio and distortion (SINAD). SINAD represents these two AC characteristics in one number, as expressed by **Equation 2**:

$$\text{SINAD (dB)} = -20\log\sqrt{10^{-\text{SNR}/10} + 10^{\text{THD}/10}} \quad (2)$$

From **Equation 2**, you can see that as the SNR increases, SINAD also increases. Thus, the less noise and distortion present, the better the SINAD. Using SINAD, you can use **Equation 3** to easily find the ENOB of your ADC - especially since:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{dB}}{6.02} \quad (3)$$

Revisiting **Equation 1**, decreasing the total noise present in the voltage reference would decrease the total noise present in the circuit, leading to an increased SNR. With an increased SNR, the ENOB will also increase. Additionally, adding a high-bandwidth buffer on the output of the voltage reference would also lead to a decreased THD of the ADC, allowing the ENOB to increase.

How voltage reference noise affects noise-free resolution

While ENOB valuably represents the resolution of your ADC output, it does not account for DC performance. To understand the resolution implications of noise from a DC input to your ADC, consider finding the noise-free resolution of your circuit. Using **Equation 4** you can calculate the noise-free resolution by observing the code spread in number of least-significant bits (LSB) of an ADC's digital output while measuring a DC signal:

$$\text{Noise Free Resolution} = \text{N} - \log_2(\text{Code Spread}) \quad (4)$$

To highlight the impact of reference noise on the system precision performance, my colleagues and I conducted DC code spread tests for a given signal chain using the REF70 (with 0.23ppm$_{p\text{-}p}$ flicker noise) and the REF50 (with 3ppm$_{p\text{-}p}$ flicker noise). Both the REF50 and REF70 are high-precision voltage references used with high-precision ADCs, and have differing DC characteristics. However, in this exercise, the goal was solely to compare

the noise performance of these devices in a signal-chain circuit.

The design uses batteries for a stable DC source with a voltage level close to the full-scale range of the **ADS8900B** 20-bit SAR ADC, which captures data at 20kSPS. **OPA2320** is used with a gain = 1 to drive the **ADS8900B** inputs. This ADC integrates the reference buffer driver; therefore, an optional reference buffer is not required. Placing a simple resistor-capacitor low-pass filter on the output of the voltage reference further lowers the noise from the voltage reference. **Figure 3** shows the setup used for these tests.

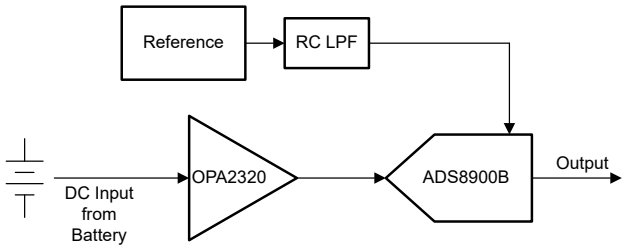

Figure 3. *The circuit used for the following noise-free resolution tests.*

The signal-chain components beside the voltage reference also have flicker noise, which will be part of the final code spread. Because the signal chain remains the same with different references only, the impact on performance numbers must be from the voltage reference noise only.

High-precision systems employ data-processing techniques to improve the precision and increase the overall resolution. In this experiment, we converted the 20-bit raw data from the **ADS8900B** to a 24-bit length by multiplying the output by 16. Different finite impulse response (FIR) filters processed the converted 24-bit data. FIR filters are easy to implement and settle faster if there's a change in the input values. The output data rate remains at 20kSPS, but with latency as defined by the filter characteristics.

At a 24-bit level, the noise (and thus the precision) of REF50 and REF70 are almost similar, with the overall noise dominated by the signal chain and its wide bandwidth noise. The difference in the average code value is because of the reference voltage difference – an accuracy specification that you can eliminate through calibration. These results can be seen in Figure 4 and Figure 5.

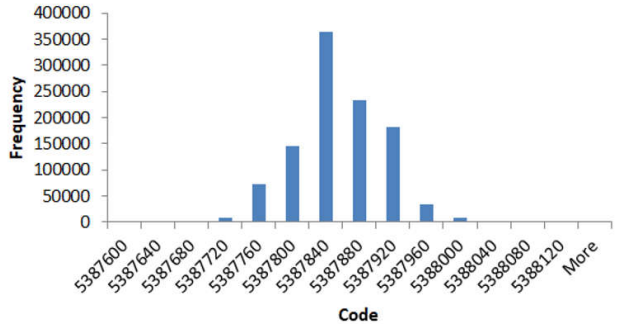

Figure 4. *Results with REF50 noise = 3ppm$_{p-p}$.*

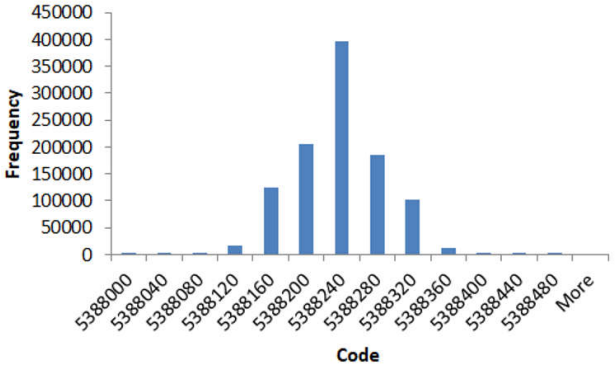

Figure 5. *Results with REF70 noise = 0.23ppm$_{p-p}$.*

We used the Octave tool to conduct post-processing of the raw data with three different digital filters:

- 1,024-tap moving average filter.
- 801-tap 17Hz low-pass filter.
- 455-tap 36Hz low-pass filter.

Figure 6 shows the filter response for these filters.

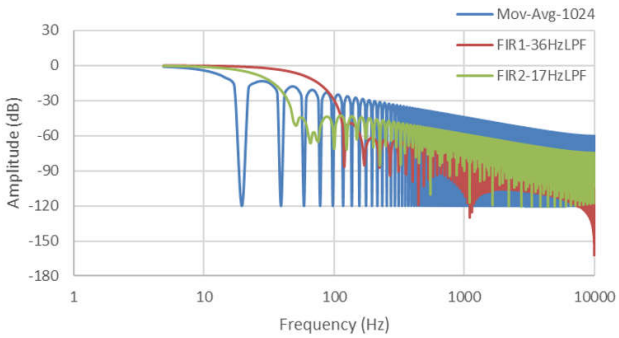

Figure 6. *Digital filter response.*

Figure 7, **Figure 8** and **Figure 9** illustrate the impact of the digital filter on the code spreads.

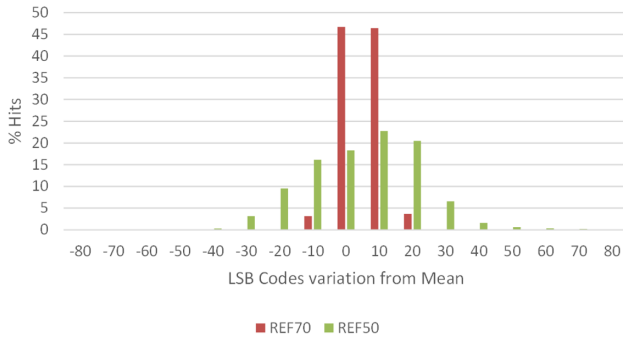

Figure 7. *1,024-tap filter histogram.*

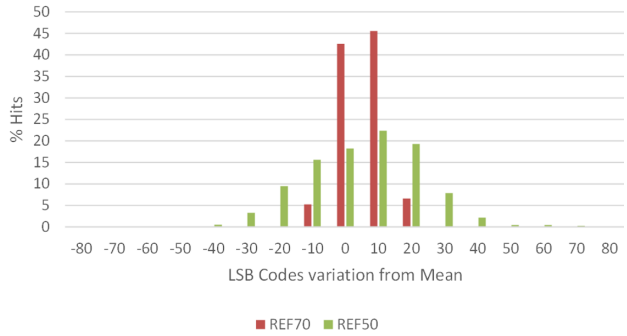

Figure 8. *455-tap filter histogram.*

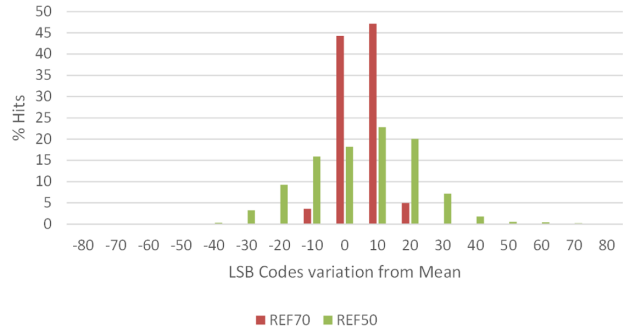

Figure 9. *801-tap filter histogram.*

Using **Equation 4**,you can easily compare the impact of the REF50 and REF70 with each filter profile on the ADC resolution. The results from these tests are summarized in **Table 1**.

Digital filte type	Corner frequency (Hz)	Number of taps	DC code spread (LSB)	Noise-free resolution (bits)	DC code spread least significan bit	Noise-free resolution (bits)
			REF70 at 24 bits		REF50 at 24 bits	
No filter	N/A	0	448	15.1	496	15.0
1,024 tap moving average	8	1,024	35	18.8	118	17.1
FIR No. 1	17	801	38	18.7	121	17.0
FIR No. 2	36	455	49	18.3	135	16.9

Table 1. *Comparison of DC code spread using different filter profiles and reference devices.*

This comparison shows that in the highest precision applications, the REF70 performs better than the REF50 when calculating noise-free resolution, mostly because of the devices' difference in flicker noise levels. The reduced code spread when using the REF70 shows that its ultra-low noise can offer nearly a 2-bit resolution advantage in high-precision applications. Additionally, we can see that using a low noise reference allows using a fast 455 tap filter while still being able to maintain a high noise free resolution. Low voltage reference flicker noise will lead to lower code spread, thus enabling higher noise-free resolution. Like the ENOB, noise is an important consideration when designing your signal chain for low noise-free resolution.

Conclusion

As ADCs are used in thousands of applications and technologies, there will always be a need to obtain better accuracy and higher precision. Whether you are designing a highly advanced x-ray system, an exceptionally precise battery test circuit, or any other world-leading innovation, careful voltage reference selection and implementation are essential to improve the precision and accuracy of your ADC signal chain. You will increase the ENOB and noise-free resolution of your ADC, enabling more advanced and diverse signal-chain implementations.

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