Optimizing multi-megahertz GaN driver design

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Discover what the important metrics are for designing supplies running at several megahertz, and how previously disregarded driver properties became fundamental to proper operation.

Introduction

The industry is embracing gallium nitride (GaN) field-effect transistors (FETs) due to their superior figure-of-merit (FOM). GaN is enabling engineers to design high-frequency applications running at several megahertz and improve overall power density to levels not possible before.

In this speed realm, there are considerations beyond the basic datasheet specs, which are required to appropriately select a FET driver. These hidden parameters can severely impact the design where the high operational speeds exacerbate every loss mechanism.

To enable high-frequency applications it is paramount to minimize losses, and an accurate analysis of losses is needed to identify areas of improvement. Some areas of loss are typically overlooked in slower switching applications where the conduction losses dominate total FET losses, but at higher frequencies the paradigm changes and switching-related losses dominate. Furthermore, many high-speed applications use small FETs that can make switching losses in the FET driver become a larger fraction of total losses.

In this paper, I will explore these losses and show how correct FET driver choice can help mitigate them, thus allowing you to push the envelope into higher-frequency operation.

Loss mechanisms

To improve efficiency in high-frequency designs, you need to understand these types of loss mechanisms:

- Third-quadrant/dead-time losses
- Bootstrap diode reverse-recovery (Q_{rr}) losses
- Driver C_{OSS} losses

Figure 1 shows a basic half-bridge schematic and highlights the location of the driver C_{OSS} and the bootstrap diode, which may suffer from Q_{rr} losses. Some drivers have an internal bootstrap, while others have an external bootstrap.

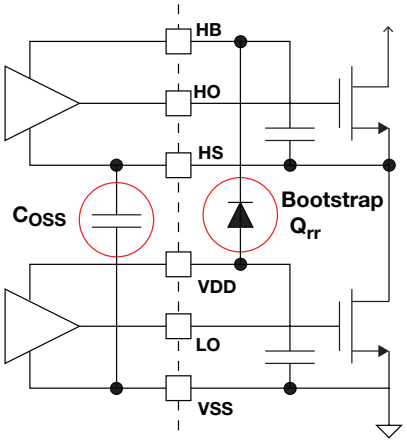

Figure 1. *Half-bridge schematic showing the location of the driver C_{OSS} and bootstrap diode with Q_{rr}.*

Third-quadrant losses

Third-quadrant losses are associated with the conduction of current from source to drain while the FET gate is low (and the FET is off). In every switching cycle, there is a short time where both FETs are off, so the inductor current may flow

through one of the FETs in third-quadrant mode. This produces a loss that is directly proportional to frequency, current and time spent in dead time.

In converters operating at high frequencies and low input or output voltages, this loss can significantly degrade efficiency. For example, in a 12V to 1.8V buck converter operating at 5MHz with 10A output, going from a 1ns to 10ns dead time can degrade efficiency by 8.5% [1].

To minimize this loss, the low- and high-side propagation delay mismatch of the driver must be very stable across device-to-device variation, temperature, bootstrap voltage, high-side pin voltage (HS in **Figure 1**) or HS slew rate. Many of these effects are not measured in datasheets.

TI's LMG1210 was designed to minimize propagation delay variation. **Table 1** summarizes the factors that cause propagation delay variations for the LMG1210 and the earlier generation LMG1205. The vast improvement in dead time of the LMG1210 results in improved efficiency.

Variation cause	Variation amount (ns)	
	LMG1205	LMG1210
Intrinsic driver	±8	+3.1/-0.55
HS voltage	±2.8	0
Bootstrap voltage	+11/-2	+0.75/-0.1
Common-mode transient immunity (CMTI) phase	+6/-2	+0.5/-0.2

Table 1. *Dead-time causes and their effects on two drivers [1].*

Reverse-recovery losses (Q_{rr} losses)

Dead time is not the only loss that the driver affects. Though GaN devices themselves do not have Q_{rr}, if you are using a diode for the bootstrap, the Q_{rr} of that diode will contribute to losses. Using a Schottky or a small third GaN device as a synchronous bootstrap can eliminate this loss if needed.

In general, the Q_{rr} loss of a diode depends on the current flow in the diode in the time shortly before it reverses. Although the average current in a bootstrap diode can be quite low, a surge of current can flow through the bootstrap diode during the dead time just before the diode voltage reverses in converters where the current flows out of the half bridge. This surge of current is caused by the sudden drop of voltage on the switch node during the dead time, which puts an equally sized forward voltage drop across the bootstrap diode and creates high currents. The current surge causes a large Q_{rr} loss when the diode reverses. This effect does not generally occur in boost-type converters because the switch node does not drop during the dead time.

The LMG1210 features a switch in series with the bootstrap diode that turns on a couple of nanoseconds after the low-side FET turns on and turns off a couple of nanoseconds before the low-side FET turns off. This means that the bootstrap diode is disconnected during the dead-time portion of the cycle, thus eliminating any surge of current through the bootstrap diode during the dead time and reducing the associated Q_{rr} loss. Consequently, the Q_{rr} loss is now directly proportional to the average bootstrap-diode current, not the surge current. This bootstrap switch also has the effect of eliminating bootstrap-voltage capacitor overcharging.

Figure 2 shows a transistor-level simulation of the LMG1205 with the switch-node voltage and bootstrap-diode current. Two cases are simulated: a normal LMG1205 case where the bootstrap diode is present during the dead time (shown in red) and another case where the diode switches out before the dead time begins, which emulates the LMG1210 (shown in blue). If the bootstrap diode is not switched, the current surges to 1.2A during the dead time and the larger reverse-recovery current is evident.

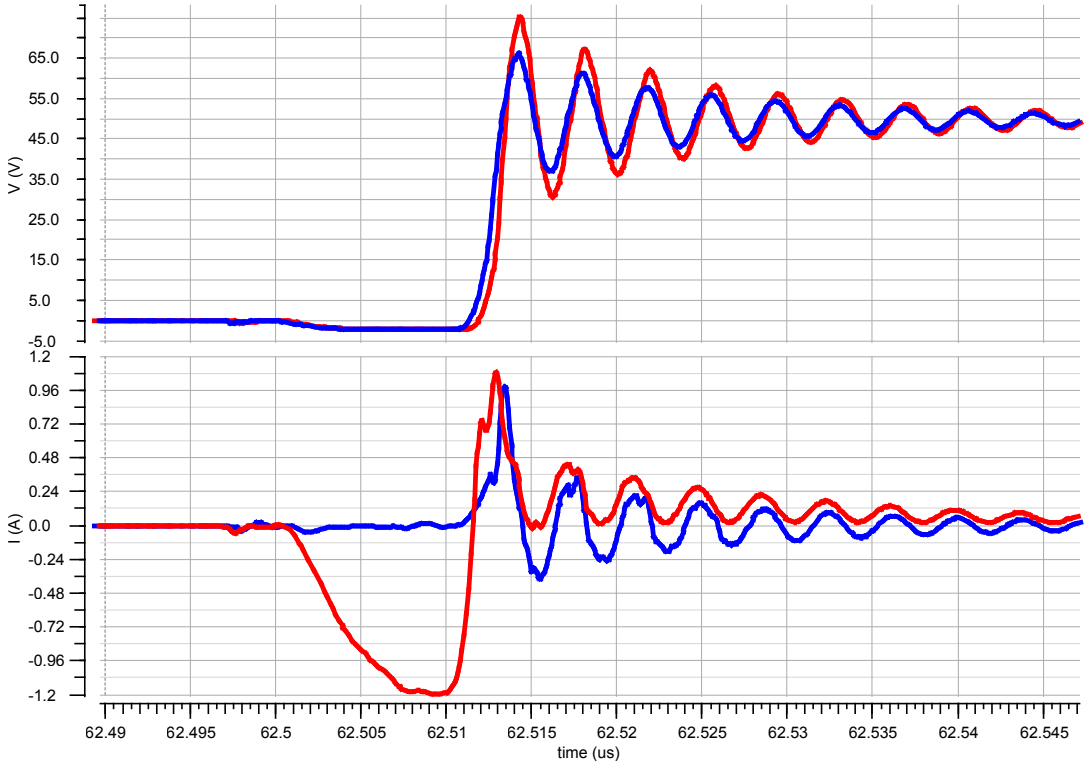

Figure 2. *Switch-node voltage (top) and bootstrap current (bottom). The red line is the LMG1205 style showing a surge of current right before the diode reverses. The blue line is the LMG1210 style where the bootstrap shuts off before the dead time.*

In this simulation, the Q_{rr} is 8nC per cycle, which is taken from the high-voltage bus supply. For a 48V bus converter at 1MHz, that is an additional 384mW of loss. This loss is linearly proportional to the frequency and bus voltage. Furthermore, the surge in current and associated Q_{rr} causes increased switch-node ringing.

To measure this effect on the bench, I configured an LMG1210 board with EPC's EPC8010 FETs as a buck converter from 12V to 6V switching at 5MHz and tested two bootstrap diodes: a 300V p-type n-type (PN) junction diode (Diodes Inc.'s BAV3004W-7-F) and a 150V Schottky diode (Diodes Inc.'s BAT46W-7-F). I used a 1.5A load with a 5ns dead time and measured the power loss with two configurations: one with the bootstrap switch operating normally and the other with the bootstrap switch shorted, which emulates the performance of the LMG1205. **Table 2** lists the results.

Diode	Total power losses (mW)		Δ loss (mW)
	BST switch shorted (LMG1205)	BST switch operating (LMG1210)	
PN junction	985	825	160
Schottky	748	743	5

Table 2. *Total losses with different diode configurations.*

The loss difference between the Schottky and PN junction diode may be caused by the increased bootstrap voltage when using the Schottky diode (due to the lower Schottky forward-voltage drop) and reduced Q_{rr}. As you can see, the PN junction diode benefits most from shutting off the bootstrap diode right before the dead time because it suffers most from Q_{rr} losses. It does not match the earlier simulation because there are different diode characteristics and different operating conditions.

The LMG1205 has an internal PN junction diode, so you cannot use an external Schottky to improve the performance without also bypassing the internal bootstrap voltage clamp. The LMG1210 with its bootstrap switch can use a cheaper PN junction diode with lower capacitance and still achieve good Q_{rr} losses, or a Schottky diode to further reduce losses.

Q_{oss} effects

Half-bridge drivers have an intrinsic capacitance from the high-side driver to the low-side ground. The LMG1210 has an improved architecture that reduces this capacitance. Furthermore, all drivers have the capacitance of the bootstrap diode. The LMG1205 diode is internal and measured as part of the driver Q_{OSS}, but for the LMG1210 the diode is external.

Figure 3 shows the isolation capacitance of the older LMG1205 and the newer LMG1210, showing the large difference between the two generations of drivers. However, keep in mind that the LMG1210 requires an external bootstrap diode, which will add to its total. The Q_{OSS} causes additional losses, which I'll describe in the next section.

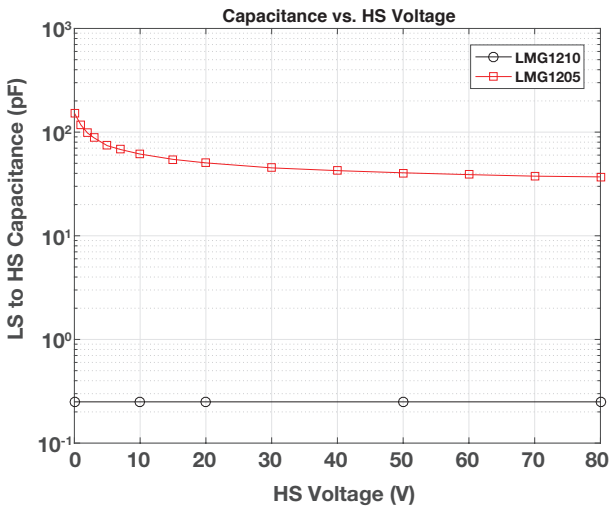

Figure 3. *High-side to low-side capacitance vs. voltage*

Q_{oss} charging/discharging losses

In hard-switched converters, the output charge gets dissipated in the FET at every turn-on transition. This loss is proportional to Q_{OSS}, bus voltage and switching frequency. GaN FETs have a significantly lower Q_{OSS} than silicon, reducing the output charge loss per cycle and therefore allowing higher frequencies.

The total Q_{OSS} is the sum of the Q_{OSS} of the FETs, the driver, the bootstrap diode and the board's parasitic capacitance. With silicon technology, Q_{OSS} losses were dominated by the silicon FET, so there was little need to pay attention to the contributions from the gate driver. When using small GaN FETs (such as the EPC EPC8000 series, with less than 1nC of Q_{OSS}), the gate driver can contribute to a significant portion of these losses. **Table 3** shows the Q_{OSS} from 0V-48V for the two drivers, which is simply **Figure 3** integrated from 0V-48V.

Device	0-48V Q_{OSS} (pC)
LMG1210	12
LMG1205	2635

Table 3. *0V-48V Q_{OSS} for the two devices*

Keep in mind, to be comparable to the LMG1205, you may consider adding the output charge of the external bootstrap diode to the LMG1210. Recommended low-capacitance diodes may add 250-800pC or more to the total for the LMG1210, with junction diodes usually on the lower end and Schottky diodes on the higher end.

In a given application, try to evaluate the ratio of the combined driver and bootstrap Q_{OSS} with respect to the FET Q_{OSS}. Keep this ratio as small as possible in order to realize the full benefits of the GaN. For the LMG1210, the driver's intrinsic capacitance is much lower than the board's parasitic capacitance and the bootstrap diode capacitance, so that is where the optimization should take place.

Conclusion

A number of loss mechanisms that designers typically ignore for applications up to a few hundred kilohertz become extremely important for new applications running with GaN at several megahertz. TI has released a new generation of gate drivers that addresses these loss mechanisms and enables this new technology to thrive. The LMG1210 enables optimized designs to up to 50MHz, leaving space for the development of future applications with GaN FETs.

References

1. Nathan Schemm. "Optimizing Efficiency Through Dead Time Control With the LMG1210 GaN Driver." Texas Instruments Application Note, SNVA815, February 2018.

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