Application Note

Getting the Most of Your Data Converter Clocking System Using LMX1204 in Cascaded Configuration

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ABSTRACT

Getting the most out of a RF signal chain design partly depends on providing a low phase noise, clean clock to the A/D converter. In this application report, phase noise data taken using the Texas Instruments' LMX1204 clock distribution device is studied. In general, the phase noise performance of any clock distribution method, is not only dependent upon the phase noise of the input clock source, but also the active clock signal chain as well. In this case the LMX1204 will be studied in both single and cascaded configurations. In general, the performance measurements confirm the operational ability of the LMX1204 device to provide as an adequate distribution method, up to 16 channels, with minimal degradation in converter performance.

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Trademarks

1 Introduction

When numerous devices in a system require a shared clock source, distributing the clock signal inadequately leads to degradation in system performance. This becomes a prevalent concern for applications utilizing digital beamforming (phased array radar, communications, ultrasound) as signal distortion increases directly as a result of increased clock jitter. The LMX1204 is a clock distribution device designed for applications requiring minimal added phase noise within the frequency range 300 MHz to 12.8 GHz. Although the LMX1204 is a high-speed clock distribution device allowing for buffered, multiplied, and divided output frequency (relative to the input frequency), this report will focus solely on the performance of this device in a buffered (1-to-1) configuration.

1.1 Cascaded LMX1204 Design

The LMX1204 creates up to four copies of an input signal, including the ability to buffer, multiply, or divide the signal to each of the outputs. This device distributes a single low power clock signal and with minimal added phase noise per stage. This design supports a two-level cascaded implementation creating 16 output clocks for distribution as shown in Figure 1-1.

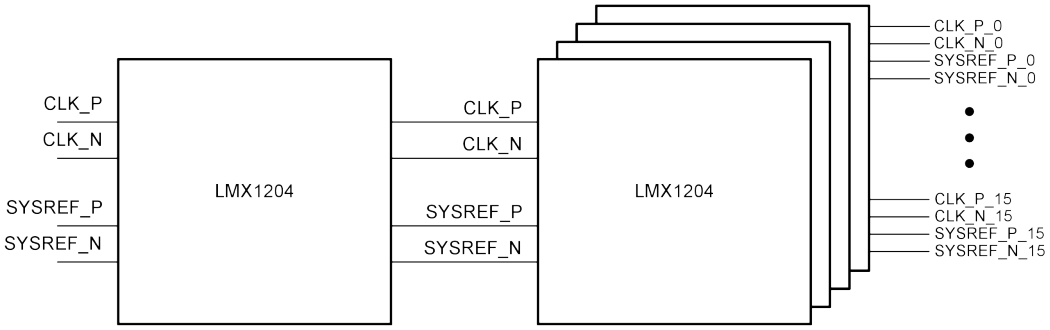

Figure 1-1. Simple Block Diagram of Cascaded LMX1204 Design

The purpose of this design is to show that the signal degradation caused by cascading two LMX1204 devices is minimal. If a design requires cascading multiple LMX1204 devices, we can expect the signal integrity to be very good, as shown in Results.

One aspect taken into consideration for this design was the board size, which was heavily determined by the number of inputs and outputs this design requires. As shown in Figure 1-2, the design uses the Samtec Bull's Eye Connector to ease the board size constraint created by 40 output differential pairs. All 20 outputs of a single LMX1204 device pass through a connector that takes up only 630mm^2, less than 1/4 of the equivalent PCB footprint using typical edge mounted SMA connectors.

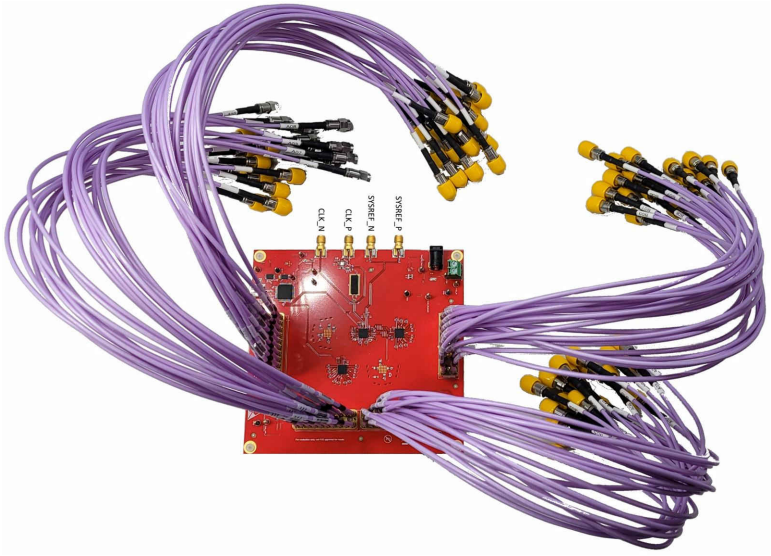

Figure 1-2. LMX1204 Clock Distribution Board

2 Results

This section provides phase noise measurements of the LMX1204 in both single and cascaded configurations and compares phase noise performance against the RF clock input source, a Rohde and Schwarz (R&S) SMA100B RF signal generator known for its ultra-low phase noise performance.

2.1 Single Device Performance

Figure 2-1 shows the phase noise performance of the LMX1204 evaluation board (LMX1204EVM) driven by the SMA100B signal generator. Device performance will be captured at the frequencies: 1 GHz, 3 GHz, 6 GHz, 10 GHz, and 12.8 GHz.

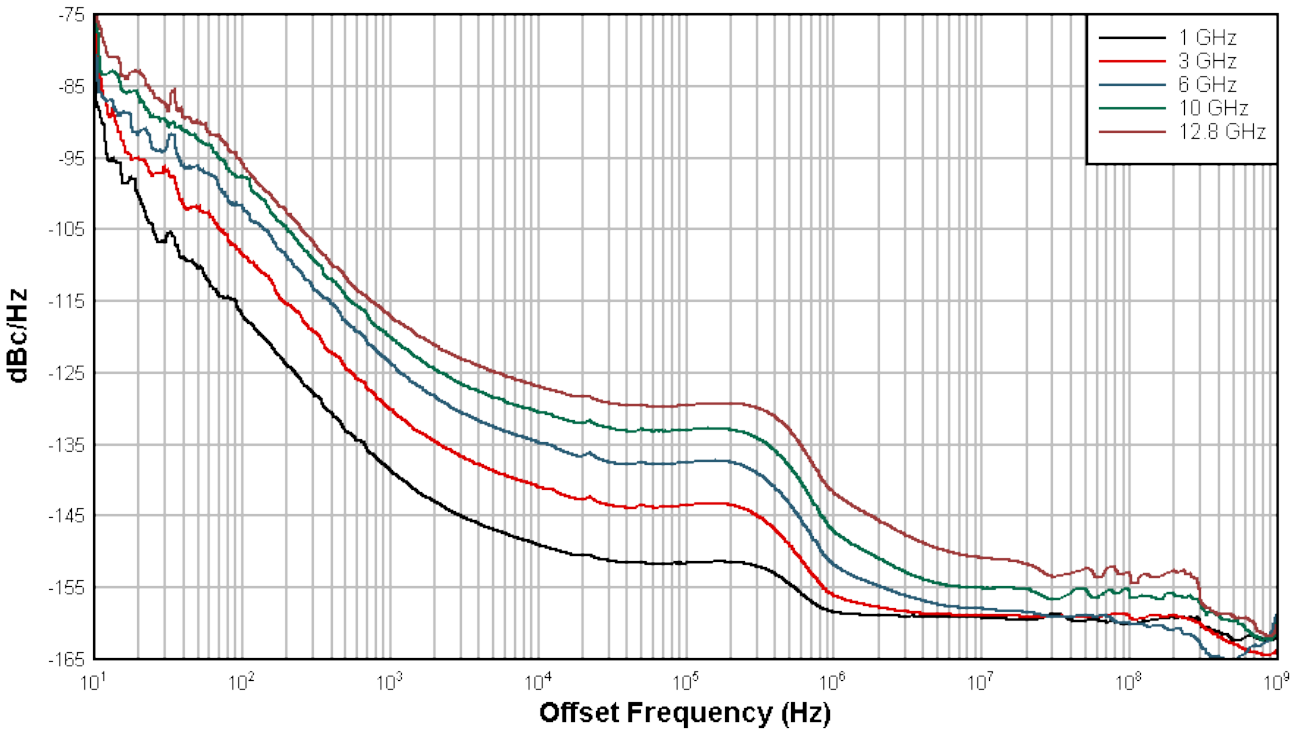

Figure 2-1. LMX1204EVM Phase Noise Measurements

The LMX1204EVM 2.5-V power supply comes from the R&S FSWP26 phase noise analyzer to avoid DC switching supply spurs coupling to the generated outputs. The LMX1204EVM operates in bypass at its highest output power.

2.2 Cascaded Device Performance

Figure 2-2 shows phase noise performance using the same R&S SMA100B RF signal generator driving the Figure 1-2. The following data showcases device performance at the same frequencies as the previous section: 1 GHz, 3 GHz, 6 GHz, 10 GHz, and 12.8 GHz.

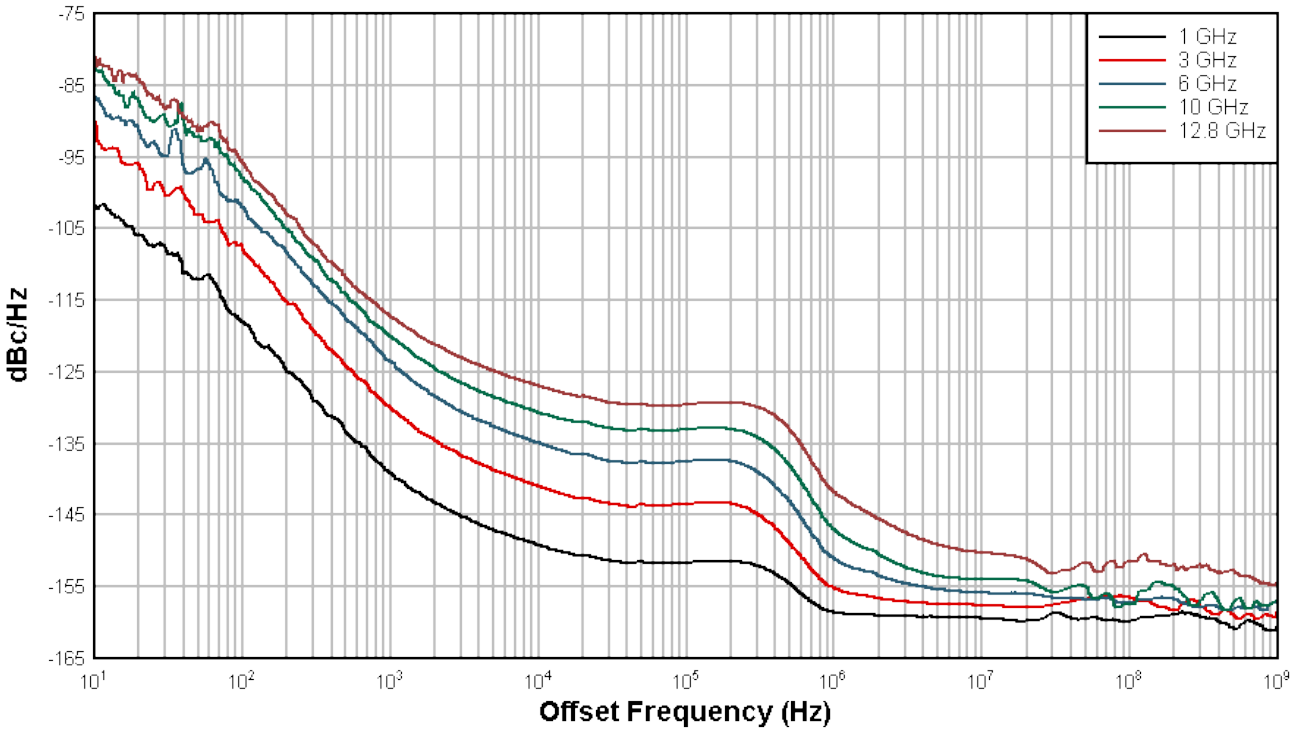

Figure 2-2. Cascaded LMX1204 Phase Noise Measurements

The +12 V supplying the cascaded LMX1204 design is generated by the R&S FSWP26 phase noise analyzer. All five LMX1204 devices are programmed for bypass mode with maximum output power.

2.3 Detailed Results

This section highlights performance at each of the individually tested frequencies and compares the results alongside the SMA100B clock source. Device performance is captured at the frequencies: 1 GHz, 3 GHz, 6 GHz, 10 GHz, and 12.8 GHz. For the following measurements, please note:

- All LMX1204 devices are from the same production lot.
- The output power for the SMA100B measurement matches the cascaded LMX1204 design output level.
- All LMX1204 devices have the output power set to maximum level (unless mentioned otherwise).

2.3.1 1 GHz Performance

The LMX1204EVM has slightly elevated phase noise compared to both the cascaded LMX1204 design and SMA100B as shown in Figure 2-3. As the cascaded LMX1204 design matches the SMA100B at low frequency offsets (< 100 Hz), the inconsistency at those low frequency offsets is likely due to PCB layout related differences.

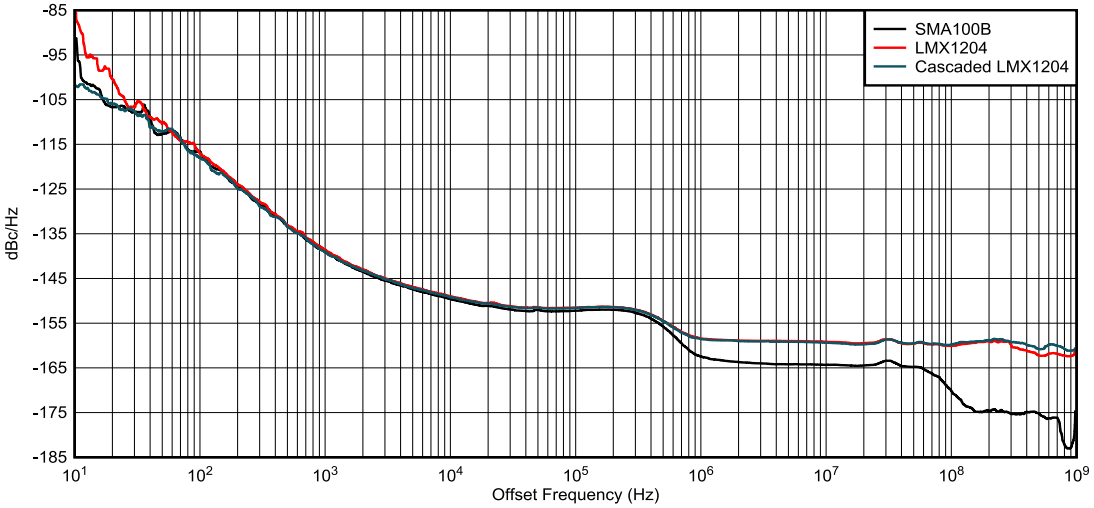

Figure 2-3. Phase Noise Comparison - 1 GHz

All three sources match to around the 400-kHz offset frequency range before diverging. At this point, the SMA100B begins to drop beneath the -160 dc/Hz noise floor shown by the LMX1204 devices. There is minimal separation between the single and dual stage LMX1204 configurations, indicating the added phase noise by the second LMX1204 is negligible at 1 GHz.

2.3.2 3 GHz Performance

Figure 2-4 shows the phase noise at close-in offset frequencies of a 3 GHz carrier for the SMA100B and cascaded LMX1204 design is slightly better than the LMX1204EVM, once again indicating board layout improvement on the cascaded LMX1204 design. The performance of all three sources is near identical out to an offset frequency of 800 kHz, which is slightly further out than the 1-GHz carrier frequency case. Both LMX1204 devices match the SMA100B to an increased offset frequency as the SMA100B noise floor is elevated.

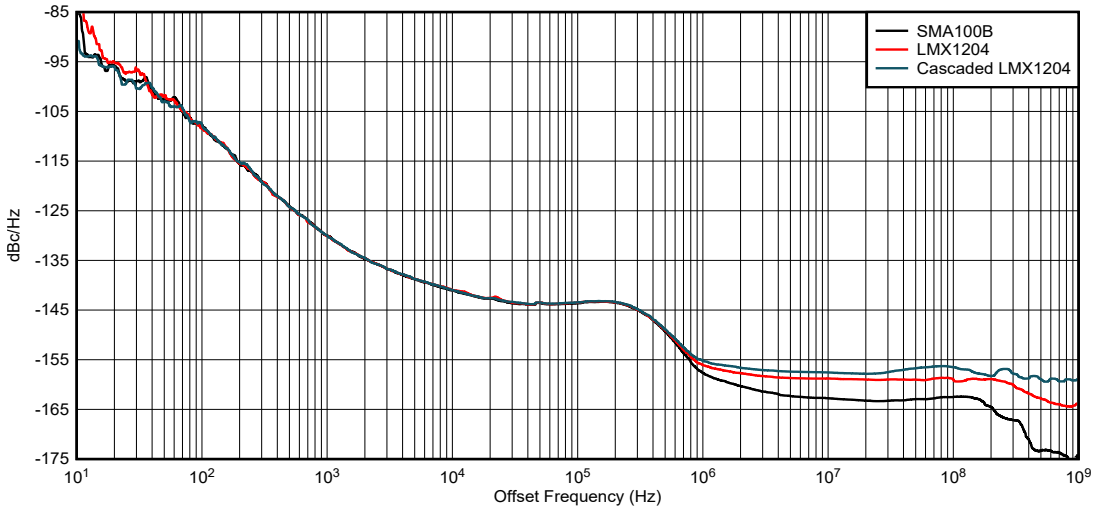

Figure 2-4. Phase Noise Comparison - 3 GHz

The cascaded LMX1204 design noise floor shows an average increase of 1.4 dB compared to the single LMX1204 response at 3 GHz. Use this increase as an estimate of the noise floor degradation as additional LMX1204 devices are cascaded. This elevation amount is important as it can be used to quickly estimate the added phase noise for a system of *N* number of devices operating near 3 GHz as each additional stage should elevate the noise floor by only 1.4 dB. Refer to Section 2.4 for a comparison in data converter performance in a 2.6 GSPS ADC application between the SMA100B and LMX1204 clock distribution board.

2.3.3 6 GHz Performance

Figure 2-5 shows phase noise at offset frequencies is quite similar for all sources out to an offset frequency of 800 kHz, which is similar to the 3 GHz carrier frequency measurements. Again, a noise floor discrepancy appears between the LMX1204EVM measurement and the cascaded LMX1204 design measurement. This elevated noise floor is caused by the additive thermal noise of the second LMX1204 stage.

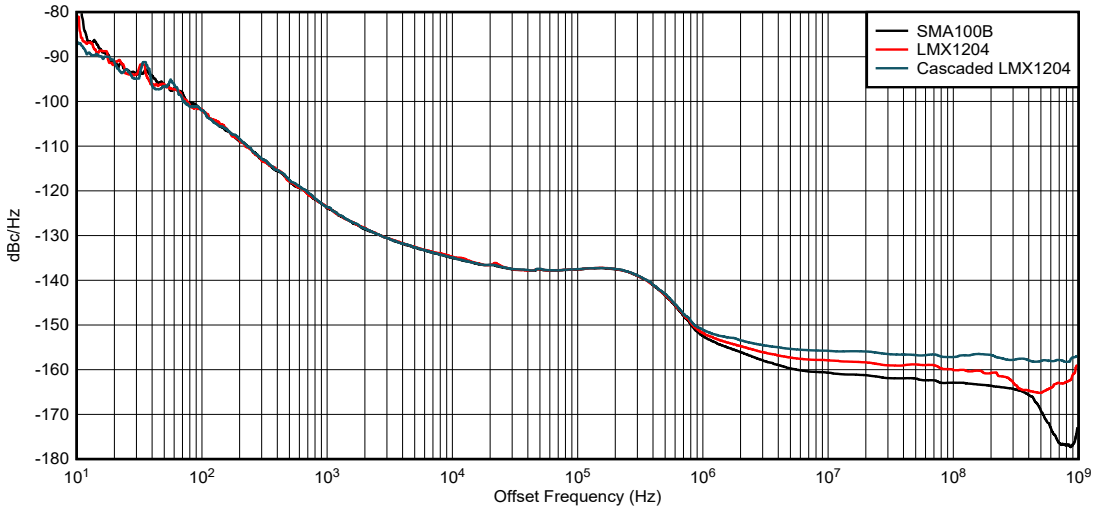

Figure 2-5. Phase Noise Comparison - 6 GHz

The difference between the two LMX1204 device noise floors is 2.2 dB on average. Use this to estimate the noise floor of a system with *N* stages of cascaded LMX1204 devices near 6 GHz.

2.3.4 10 GHz Performance

Figure 2-6 shows a 10 GHz carrier frequency. The performance of all three sources is near identical out to an offset frequency of 1 MHz, which is slightly further than the previous carrier frequencies. An average difference measures as 0.7 dB between the LMX1204EVM and the cascaded LMX1204 design. Refer to Section 2.5 for a comparison of performance in a high frequency application.

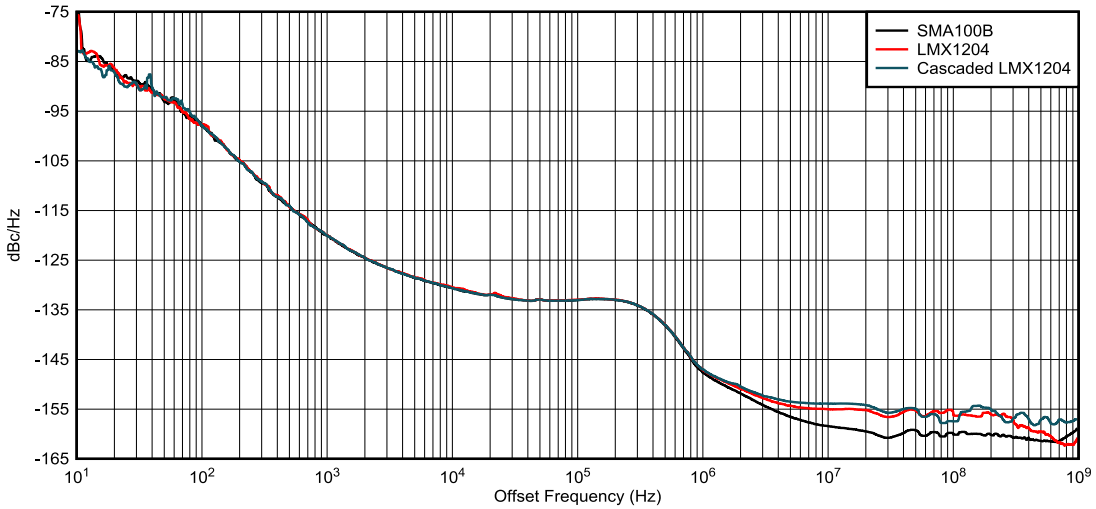

Figure 2-6. Phase Noise Comparison - 10 GHz

2.3.5 12.8 GHz Performance

Figure 2-7 shows the phase noise is similar out to an offset frequency of 2.5 MHz, at which point the LMX1204 devices' measured phase noise begins to converge. The phase noise of the cascaded LMX1204 design follows what is measured on the LMX1204EVM up to an offset frequency of 100 MHz, at which point the cascaded design follows the variation produced by the SMA100B at an elevated noise floor.

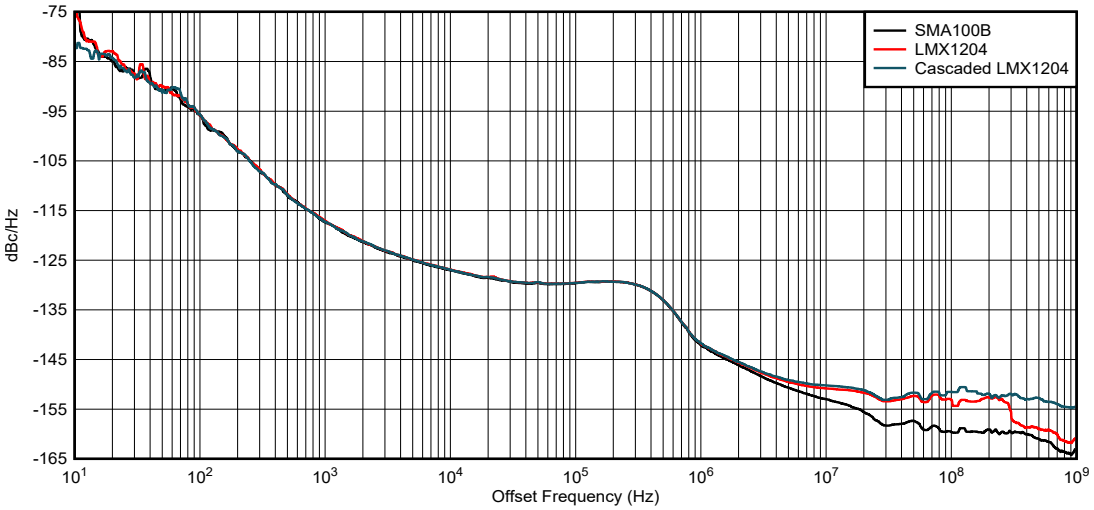

Figure 2-7. Phase Noise Comparison - 12.8 GHz

The average difference measured beyond 2.5 MHz comes out as 0.4 dB, which predicts the amount of added phase noise generated by any additional cascaded LMX1204 devices in a system operating near 12.8 GHz. Refer to Section 2.5 for a comparison in high-speed converter performance.

2.4 Cascaded LMX1204 Performance With ADC32RF54

Figure 2-8 compares the difference in SNR (signal-to-noise ratio) using the ADC32RF54EVM evaluation module clocked by the SMA100B and the cascaded LMX1204 design.

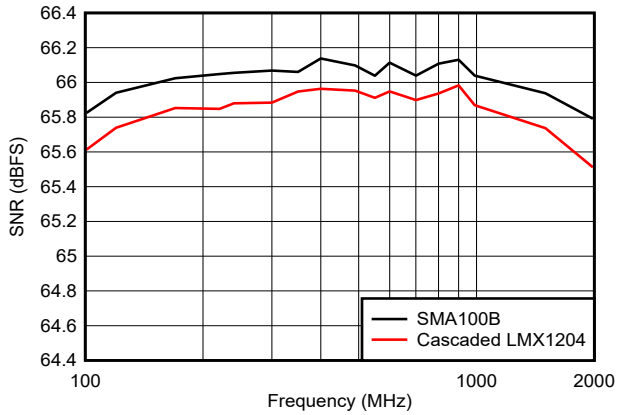

Figure 2-8. ADC32RF54 - SNR vs. Clock Source vs. Frequency

Figure 2-8 above shows SNR in dBFS (decibel relative to full-scale ADC level) at numerous frequencies within the range of 100 MHz to 2 GHz. Each of the input frequencies above is filtered using a narrow bandpass filter to reduce the impact of higher frequency noise and harmonics throughout the capture. The sample rate is a constant 2.6 GSPS and the SMA100B is set such that the output power matches the measured output power level from the cascaded LMX1204 (6.17 dBm). On average, the SNR is degraded by a mere 0.15 dB.

2.5 Cascaded LMX1204 Performance With AFE7950

This section highlights the ADC SNR performance of the AFE7950EVM analog front end evaluation module when clocked by an SMA100B versus the cascaded LMX1204 board.

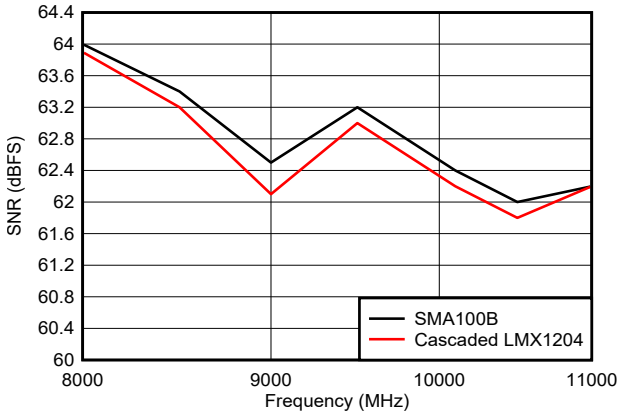

Figure 2-9. AFE7950 - SNR vs Clock Source vs Frequency

The AFE7950 is a 4T6R AFE containing four digital to analog converters (DAC) and six analog to digital converters. The input clock is 11,796.48 MHz which is suitable for X-band frequency of operation.

The sample clock of the ADC of 2949.12 MHz is derived from the input clock divided by 4. The receiver operates in a decimate by 12 mode so that the output data rate is 245.76 MSPS. The internal numerically controlled oscillator (NCO) is set to 20 MHz below the center of each RF band so that the baseband tone falls at 20 MHz.

Figure 2-9 plots SNR performance from 8 GHz to 11 GHz in 500 MHz steps. Each input frequency is filtered to reduce the noise and harmonics of the input source. The EVM requires a high clock drive level of around 7 to 15 dBm near 12 GHz due to on-board losses. The LMX1204 output drive is limited to roughly 1 dBm at 12 GHz. The clock output is increased with a Qorvo power amplifier (P/N: CMD158) to 16 dBm followed by a 1 dB pad (to further improve impedance matching) to get to the optimum input level for the AFE7950EVM. The signal generator is set such that the output power matches the measured output power of the cascaded LMX1204

(–0.88 dBm) prior to the amplifier and pad. The amplifier and pad remain in the signal chain for the SMA100B measurements. On average, the SNR is degraded by only 0.19 dB.

3 Summary

The data presented in this document confirms the ability of the LMX1204 device to distribute a clock source up to 16 simultaneous outputs with minimal loss in the quality of the clock signal. These measurements also suggest the LMX1204 to perform well in systems exceeding two cascaded devices, allowing for high-performance clock distribution in large systems with minimal degradation in performance. Designing a large clocking solution with multiple LMX1204 devices in a cascaded configuration allows for minimal design effort while maintaining high performance clocking systems.

4 References

1. *IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology---Random Instabilities,* in *IEEE Std 1139-2008*.

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