Application Note

Clocking for PCIe Applications

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ABSTRACT

Peripheral Component Interconnect Express (PCIe) is an industry standard for transferring data between CPUs and peripheral devices across motherboards. This protocol is used in personal computers, desktops, enterprise servers, and so on. This application note covers the PCIe clocking basics. This publication also includes the clocking architectures, PCIe test criteria, and post-processing tools..

Table of Contents

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1 Introduction

PCIe began with the first generation, PCIe Gen 1.1, in 2003. The standard is by the Peripheral Component Interconnect Special Interest Group (PCI-SIG). PCIe replaced the original PCI, a parallel communication bus. PCIe uses a serial point-to-point architecture which allows for higher data transfer rates, as devices are not competing for bandwidth on a bus. PCIe also employs differential HCSL or LP-HCSL clocks instead of the PCI LVCMOS clocks, allowing for better noise immunity, and Spread Spectrum Clocking (SSC) for reduction of electromagnetic interference (EMI). This application note discusses the clocking architectures for the PCIe link, as well as the measurement techniques for jitter and waveform integrity.

2 Introduction to PCIe

2.1 The PCIe Link

In a PCIe link, signals are transferred over connection pairs referred to as *lanes*. One lane for transmitting data (TX), and another lane for receiving data (RX). PCIe is a scalable architecture. Each link can be comprised of up to 32 lanes at once for maximizing data throughput. Most systems typically employ only 16 lanes. Figure 2-1 shows an example of a standard PCIe link.

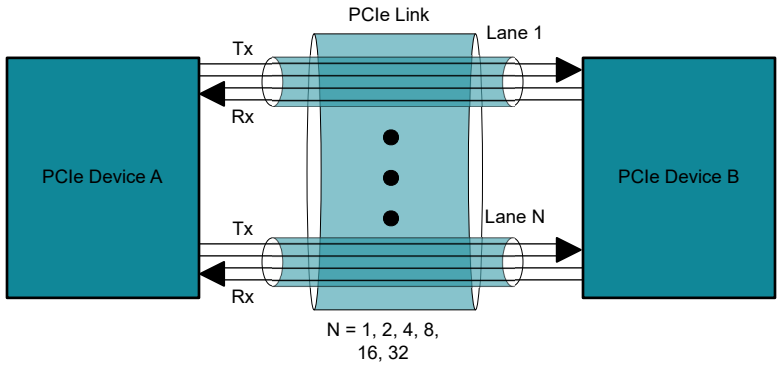

Figure 2-1. PCIe Link

As the PCIe standard has evolved, the raw bit rate per lane has improved. Modern-day PCIe Generation 6.0 allows for a bit rate of 64 Gb/s. Table 2-1 shows the data rate for each PCIe generation.

Table 2-1. PCIe Standard Bit Rate by Generation

PCIe Generation	Debut Year	Raw Bit Rate
PCIe 1.1	2005	2.5 Gb/s
PCIe 2.1	2009	5.0 Gb/s
PCIe 3.1	2013	8.0 Gb/s
PCIe 4.0	2017	16.0 Gb/s
PCIe 5.0	2019	32.0 Gb/s
PCIe 6.0	2021	64.0 Gb/s

With 8 bits per byte, the data throughput per lane per direction for PCIe 6.0 is up to 8 GB/s per direction per lane. In a 16-lane system, throughput up to 256 GB/s is achievable.

3 PCIe Clocking Architectures

In PCIe systems, both the transmitter and receiver devices are provided with a reference clock, referred to as REFCLK. For all PCIe generations, REFCLK is a 100 MHz HCSL clock, and Table 3-1 shows the maximum frequency stability requirements by generation for Common Clock architectures.

Table 3-1. REFCLK Frequency Stability by PCIe Generation

PCIe Generation	Frequency Stability (ppm)(1)
PCIe 1.1	±300
PCIe 2.1	±300
PCIe 3.1	±300
PCIe 4.0	±300
PCIe 5.0	±100
PCIe 6.0	±100

(1) For all Separate Reference architectures, the frequency stability of REFCLK is ±100 ppm, regardless of the bit rate.

The clocking architectures are as follows:

- Common Clock (CC)
- Common Clock with Spread (CCS)
- Separate Reference No Spread (SRNS)
- Separate Reference Independent Spread (SRIS)

3.1 Common Clock Architecture

In Common Clock (CC) architectures, both the transmitter and receiver devices are clocked by the same PLL. Figure 3-1 shows a block diagram of this architecture. Common clock is the most widely supported PCIe clocking architecture. This architecture easily supports SSC on both PCIe devices for EMI reduction, allowing for Common Clock with Spread (CCS). Figure 3-1 shows a typical common clock architecture.

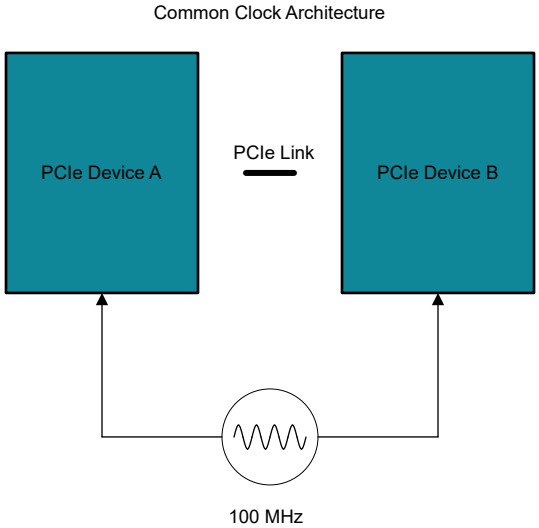

Figure 3-1. Common Clock Architecture

3.2 Separate Reference Architecture

In Separate Reference architectures, different clock sources are used for the transmitter and receiver devices. Figure 3-2 shows a block diagram of this architecture. Systems using SRNS or SNIS must account for clock shifts between the TX and RX devices using elastic buffers. Up to 600 ppm difference in the clocks is allowed, resulting in a clock shift every 1666 clocks. In SNIS, SSC adds another 5000 ppm of shift, resulting in a clock shift as often as every 178 clocks. The elastic buffer of a component that supports the SRIS architecture can need more entries than those supporting SRNS, as the data payload size varies.

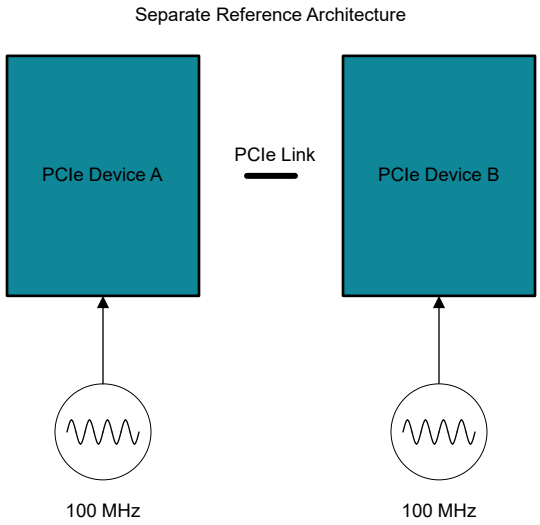

Figure 3-2. Separate Reference Architecture

3.3 Spread Spectrum Clocking

Both Common Clock and Separate Reference architectures allow for Spread Spectrum Clocking. When SSC is used, the frequency of the clock is modulated, which spreads the radiated emissions across multiple frequencies instead of a single peak frequency. This modulation of the frequency increases jitter. Common Clock PCIe systems specify a modulation frequency between 30 kHz and 33 kHz with a spread between 0% and –0.5%, referred to as down-spread SSC. For Separate Reference, the spread range is 0% to –0.3%. Figure 3-3 shows the difference in peak energy for no SSC vs –0.5% down-spread SSC. The single 100 MHz peak at -5 dB is for the no SSC case. With –0.5% down-spread SSC enabled, the peak of the energy is at –14 dB.

If the 100 MHz REFCLK has –0.5% down-spread SSC, then the PCIe devices must be able to tolerate a larger ppm variance from 100 MHz: 100 ppm from the typical frequency stability budget, and 2500 ppm from the spreading of the clock frequency. This specification is typically presented as -100 to +2600 ppm. In SRIS, the maximum down-spread SSC allowed is –0.3%. The total frequency stability in this case is –100 to +1600 ppm.

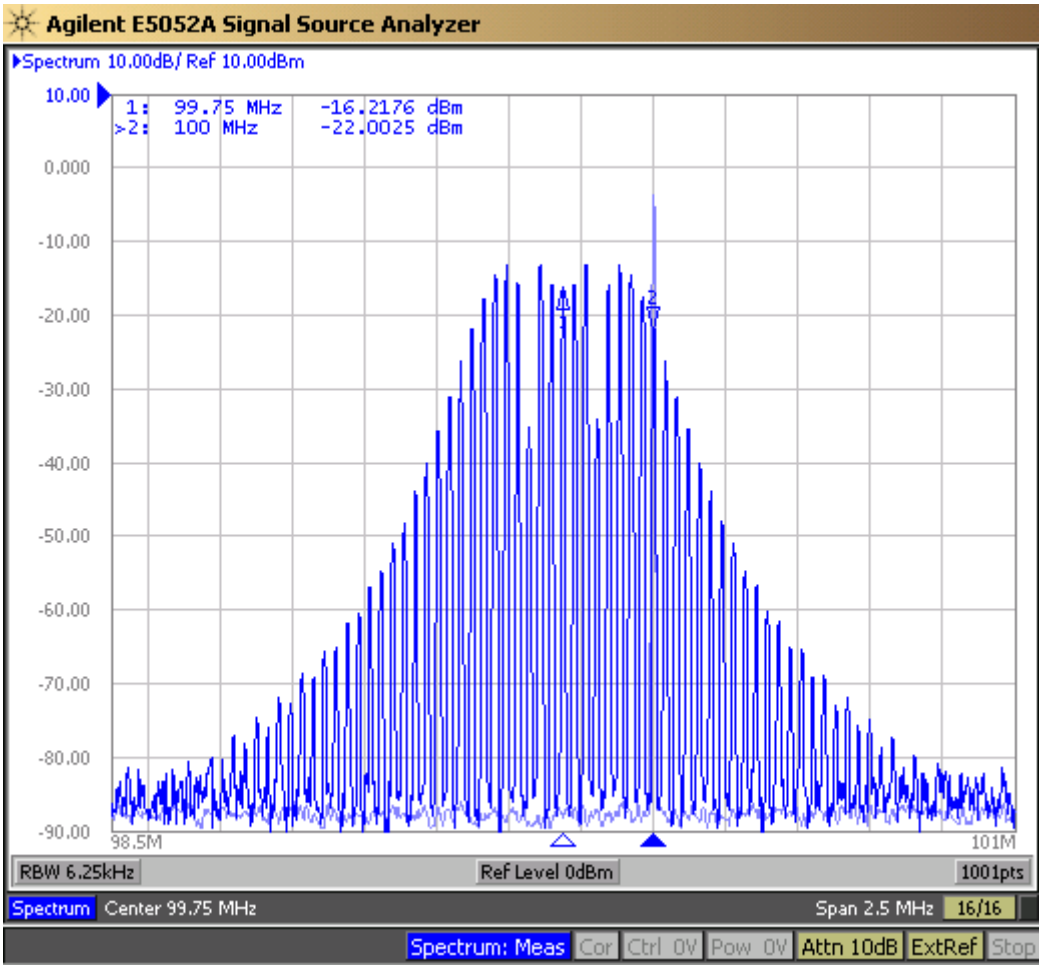

Figure 3-3. 100 MHz REFCLK With No SSC and –0.5% Down-Spread SSC

For Common Clock architectures the jitter is the same for both clocks. As such, the SSC For Separate Reference architectures, the clocks can be Separate Reference No Spread (SRNS), or Separate Reference Independent Spread (SRIS). When SRIS is used, the clock frequencies at the transmitter and receiver at any given time differ. In this case, both PCIe devices to implement buffers to account for the difference in clock frequencies.

3.4 PCIe REFCLK Topology

Figure 3-4 shows the setup of a typical Common Clock architecture with the path for data transfer. The transmitter is composed of the TX PLL and the TX Latch, and the receiver is composed of the RX PLL, RX Clock Data Recovery (CDR), and the RX Latch. REFCLK is provided to both the transmitter and the receiver, but the jitter at the receiver is impacted by the PLLs of both PCIe devices, the CDR of the receiver, and the delay between the transmission of the REFCLK through the two paths to the RX latch.

Equation 5 shows the overall transfer function of the affect of REFCLK at RX Latch. The values for the damping factors ζ and frequencies f are set by the PCIe standard based on the generation. The PLLs of TX and RX function as second order low-pass filters. Up to PCIe Gen 4.0, the CDR behaves as a first order high-pass filter. For PCIe Gen 5.0 and PCIe Gen 6.0, the CDR behaves as a second-order high-pass filter.

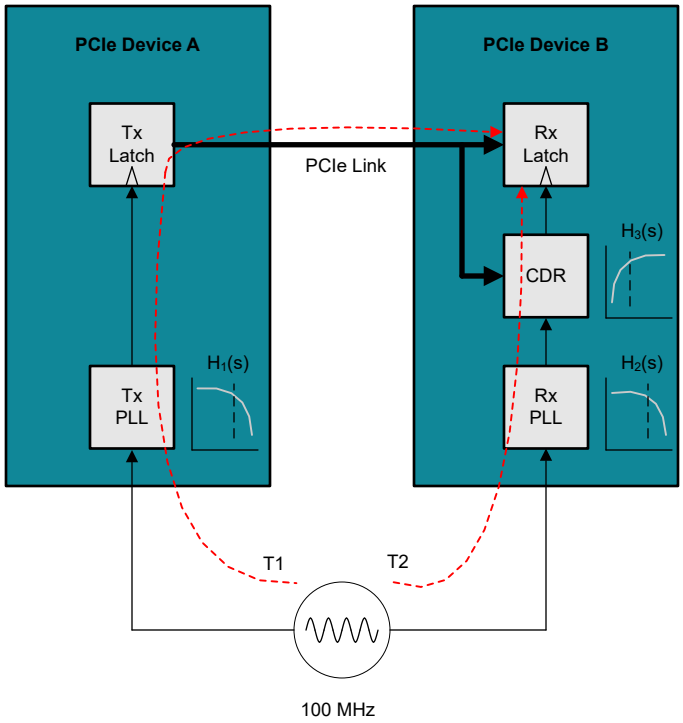

Figure 3-4. REFCLK Common Clock Distribution

$$\text{TX PLL: } H_1(s) = \frac{2s\zeta_1\omega_{n1} + \omega_{n1}^2}{s^2 + \zeta_1\omega_{n1} + \omega_{n1}^2}, \textit{ where } \omega_{n1} = 2\pi f_{n1} \quad (1)$$

$$\text{RX PLL: } H_2(s) = \frac{2s\zeta_2\omega_{n2} + \omega_{n2}^2}{s^2 + s\zeta_2\omega_{n2} + \omega_{n2}^2} \quad (2)$$

$$\text{CDR: } H_3(s) = \frac{s}{s + \omega_{n3}^2} \quad (3)$$

$$\text{Delta Between REFCLK Paths: } |T1 - T2| \quad (4)$$

$$\text{Overall Transfer Function: } H(s) = (H_1(s)e^{-st} - H_2(s))H_3(s) \text{ or } H(s) = (H_2(s)e^{-st} - H_1(s))H_3(s), \text{ whichever is larger} \quad (5)$$

For PCIe Gen 5.0 and PCIe Gen 6.0, the CDR is defined differently. For these generations, the CDR is represented by a second-order high-pass filter. Equation 6 is the equation for this filter.

$$\text{PCIe Gen 5.0/6.0 CDR: } H_3(s) = \frac{s^2}{(s+\omega_0) \times (s+\omega_1)} \times \frac{s^2 + 2s\zeta_2\omega_{n0} + \omega_0^2}{s^2 + s\zeta_1\omega_{n0} + \omega_0^2} \times \frac{s}{s+\omega_{LF}}, \textit{ where } \zeta_1 = \frac{1}{\sqrt{2}} \,\&\, \zeta_2 = 1 \quad (6)$$

For PCIe Gen 5.0, $\omega_0 = 20 \times 10^6 \times 2\pi$, $\omega_1 = 1.1 \times 10^6 \times 2\pi$, $\omega_{LF} = 160 \times 10^3 \times 2\pi$

For PCIe Gen 6.0, $\omega_0 = 10 \times 10^6 \times 2\pi$, $\omega_1 = 3.88 \times 10^6 \times 2\pi$, $\omega_{LF} = 87 \times 10^3 \times 2\pi$

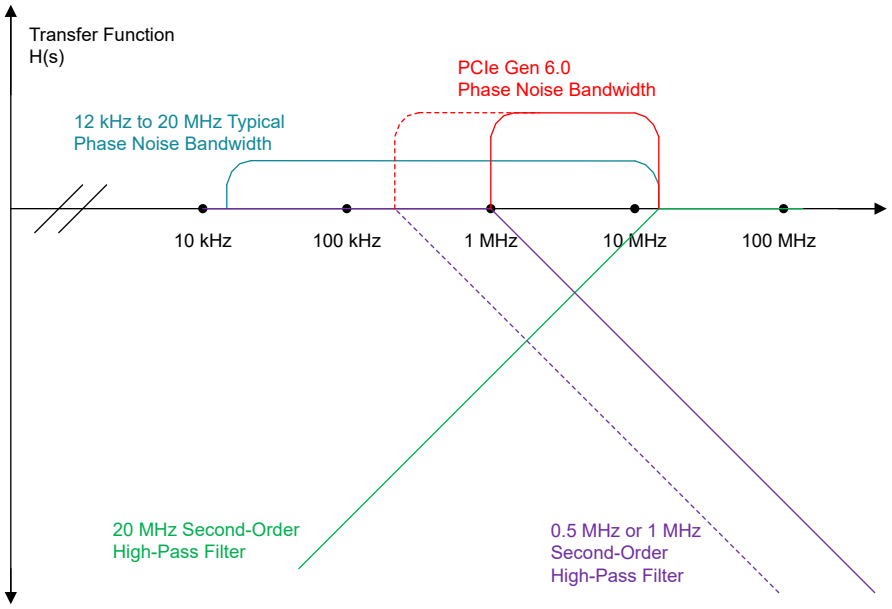

Figure 3-5. PCIe Bandwidth Visualization

Figure 3-5 is a visual representation of the bandwidth of the system for PCIe Gen 6.0. Table 3-2 provides the PCIe jitter filter characteristics for Gen 6.0. There are 16 possible jitter filter combinations. The PCIe standard lists the full jitter filter characteristics for each generation. The values for ω and ζ vary from generation to generation.

Table 3-2. PCIe Gen 6.0 Jitter Filter Characteristics

PLL1 Characteristics	PLL 2 Characteristics	CDR Characteristics
ω_{n1} = 0.112 Mrad/s ζ_1 = 14	ω_{n1} = 0.112 Mrad/s ζ_1 = 14	BW_{CDR} = 10 MHz, 2nd order
ω_{n1} = 0.224 Mrad/s ζ_1 = 14	ω_{n1} = 0.224 Mrad/s ζ_1 = 14	BW_{CDR} = 10 MHz, 2nd order
ω_{n1} = 1.50 Mrad/s ζ_1 = 0.73	ω_{n1} = 1.50 Mrad/s ζ_1 = 0.73	BW_{CDR} = 10 MHz, 2nd order
ω_{n1} = 3.00 Mrad/s ζ_1 = 0.73	ω_{n1} = 3.00 Mrad/s ζ_1 = 0.73	BW_{CDR} = 10 MHz, 2nd order

3.5 Noise Folding

The PCIe standard allows phase jitter measurements to be made with a phase noise analyzer when noise folding is implemented. Noise folding is a flat extension of the signal at the noise floor. Each *noise fold* is a 50 MHz extension of the signal. Noise folding must be implemented up to 200 MHz from the carrier, or three *noise folds*. The phase noise at the receiver is then be calculated with the noise folded signal.

4 PCIe Clocking Specifications

4.1 REFCLK Output Format

In PCIe systems, the REFCLK is a differential High-Speed Current Steering Logic (HCSL) clock. HCSL drivers source current into an external 50-Ω load. Low-Power HCSL (LP-HCSL) reduces the power consumption of the driver, and integrates the termination resistors into the driver, removing the need for external components. LP-HCSL drivers are more capable of driving long traces compared to HCSL, and are able to be AC-coupled without change to the termination or swing. Figure 4-1 and Figure 4-2 demonstrate the drivers for HCSL and LP-HCSL, respectively.

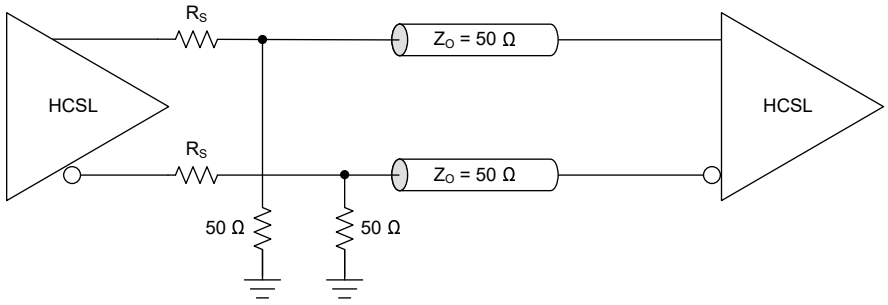

Figure 4-1. HCSL Output Termination

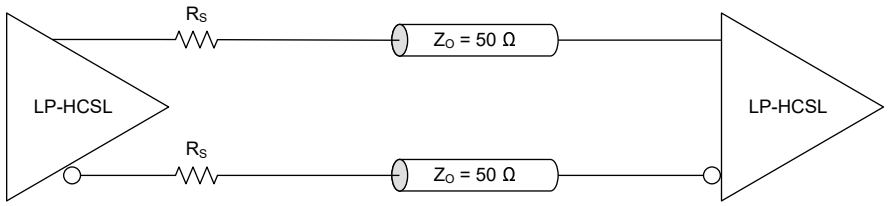

Figure 4-2. LP-HCSL Output Termination

4.2 PCIe Jitter Requirements

For Common Clock architectures, the PCIe standard sets an upper bound on the RMS jitter allowed through the filters, defined by Equation 5. This limit applies for each filter combination in a given generation. If the jitter after one set of filters exceeds the limits, then the REFCLK does not meet the requirements for that PCIe generation. Table 4-1 shows the jitter limits for Common Clock architectures after the filtering is applied. Note that these limits apply for both CC and CCS. For Separate Reference architectures, a phase jitter limit is not set by the PCIe standard; instead, the limits are left up to the engineer designing the system.

Table 4-1. PCIe REFCLK Phase Jitter Limit by Generation

PCIe Generation	REFCLK Phase Jitter Limit (ps RMS)
PCIe 1.1	86
PCIe 2.1	3.1
PCIe 3.1	1.0
PCIe 4.0	0.5
PCIe 5.0	0.15
PCIe 6.0	0.1

4.3 PCIe Time Domain Requirements

In addition to the jitter requirements of the REFCLK, there are limitations on various time-domain parameters as well. Table 4-2 summarizes these limits. The limits are not dependent upon PCIe generation or clock architecture.

Table 4-2. PCIe Time Domain Parameters

Parameter	PCIe Limit
V_{Cross}	250 mV to 550 mV
V_{High}	+150 mV minimum
V_{Low}	–150 mV maximum
$\lvert V_{Ringback} \rvert$ (1)	100 mV minimum
Period	9.847 ns to 10.203 ns
Duty Cycle	40% to 60%
$V_{Overshoot}$	+300 mV
$V_{Undershoot}$	–300 mV
Rising Edge Rate	0.6 V/ns to 4 V/ns
Falling Edge Rate	0.6 V/ns to 4 V/ns

(1) The measurement method for PCIe $V_{Ringback}$ and Intel® $V_{Ringback}$ are not the same. Intel® defines this as the single-ended voltage level that is allowed be reached after an undershoot or overshoot occurs, ±200 mV, before the voltage settles at the V_{Low} or V_{High} level, but measured with respect to V_{Low} and V_{High} instead of GND

Unless stated otherwise, the parameters in Table 4-2 are measured using the differential waveform, which is typically a math channel of a high-bandwidth oscilloscope configured for subtraction between the two single-ended waveforms. A PCIe REFCLK analysis tool, such as the *Texas Instruments PCIe Reference Clock Analysis Tool*, uses the individual waveforms and performs the calculation. Table 4-3 describes the parameters in Table 4-2.

Table 4-3. PCIe Parameter Descriptions

Parameter	Description
V_{Cross}	Single-ended voltage when the + and – REFCLK outputs are equal with respect to the system GND, measured on the rising edge of the + output, as measured into an AC load
V_{High}	High level voltage, as measured into an AC load
V_{Low}	Low level voltage, as measured into an AC load
$V_{Ringback}$	As measured into an AC load, the voltage level that is allowed be reached after an undershoot or overshoot occurs, before the voltage settles at the V_{Low} or V_{High} level, measured from GND
Period	Time for a full clock cycle, as measured between rising clock edges, including jitter and SSC
Duty Cycle	Percentage of time that clock is held high in relation to full clock period
$V_{Overshoot}$	Overshoot of voltage on rising clock edges, as measured into an AC load
$V_{Undershoot}$	Undershoot of voltage on falling clock edges, as measured into an AC load
Rising Edge Rate	The rate at which rising clock edges transition from –150 mV to +150 mV, as measured into an AC load
Falling Edge Rate	The rate at which rising clock edges transition from +150 mV to –150 mV, as measured into an AC load

$V_{Overshoot}$, $V_{Undershoot}$, and $V_{Ringback}$ can appear to violate the PCIe specification when the outputs are improperly terminated, resulting in reflections. Matching the impedance as specified by the REFCLK source and the receiver is critical for minimizing reflections. Refer to *Termination Guidelines for Differential and Single-Ended Signals* for guidance on properly terminating REFCLK.

5 REFCLK Measurement Technique

For measuring the performance of REFCLK, a Phase Noise Analyzer (PNA) can be used to measure the frequency-domain of the jitter, the phase noise. The output trace can be output to a text file, which can then be post-process through a PCIe processing tool. Newer PNAs, such as the R&S® FWSP used in this paper, are able to support both SSC and non-SSC phase noise data collection, allowing for post-processing of spread-spectrum clocks. Figure 5-1 shows the test setup for the PNA measurements. Table 5-1 lists the equipment and devices used in the REFCLK measurements.

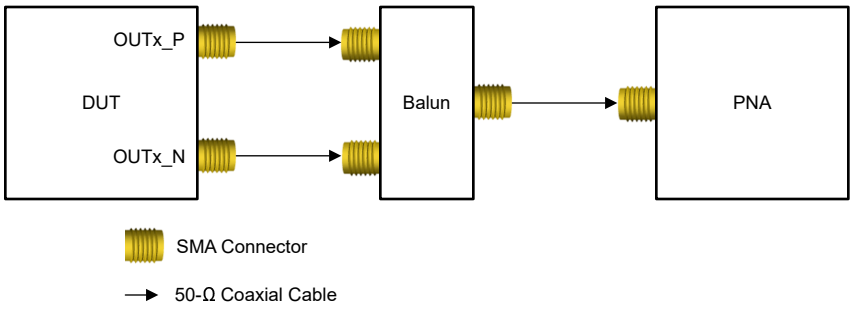

Figure 5-1. PNA Measurement Test Setup

Table 5-1. Equipment Used in REFCLK Measurements

Low-Noise Source	Devices Under Test (DUTs)	Balun	Measurement Equipment
R&S® SMA100B Agilent E5052B	LMK3H0102 LMKDB1120(1)	Mini-Circuits® ADTL2-18	R&S® FSWP(2) Agilent DSO80804B(3)

(1) The LMKDB1120 device uses the R&S® SMA100B as the low-noise clock source for PCIe measurements. Using a low noise source is critical for accurate jitter measurements.
(2) R&S® FSWP used for frequency domain measurements.
(3) Agilent DSO80804B used for time domain measurements.

5.1 Clock Generator Measurement Results

5.1.1 PNA Measurement Result without SSC

Figure 5-2 is the phase noise plot of the LMK3H0102 output clock as measured by the PNA. The 12 kHz to 20 MHz phase jitter is measured to be 179 fs. The PNA measurement is exported as a text file, from which we can import into the *Texas Instruments PCIe Reference Clock Analysis Tool* in TICS Pro. As PCIe Gen 6.0 requires data from 10 kHz to 50 MHz, the tool estimates the noise floor and extends the data to a full Nyquist band, 50 MHz.

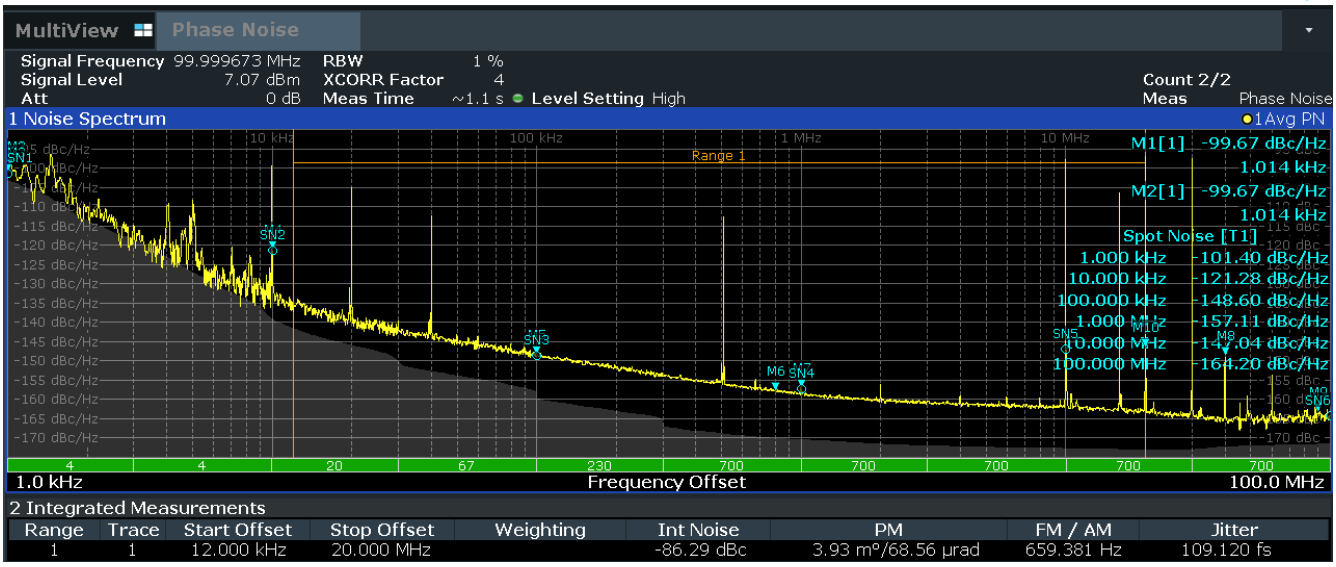

Figure 5-2. LMK3H102 Phase Noise Without SSC

5.1.2 PCIe Filtered PNA Result without SSC

Table 5-2 shows the result of the PNA capture after post processing using the PCIe Gen 6.0 filters. Each possible combination of PLL and CDR parameters is tested, resulting in 16 total filter combinations, all of which pass the PCIe Gen 6.0 limit of 100 fs of RMS jitter. The maximum noise fold is used in this case, with the noise floor extended to 200 MHz offset from the carrier.

Table 5-2. LMK3H0102 Detailed PCIe Gen 6 Measurements, Non-SSC

PCIe Gen	Clock Architecture	Noise Fold	Filter Combination	PLL1 f_1	PLL1 ζ_1	PLL2 f_2	PLL2 ζ_2	CDR f_3	Jitter (fs)	Limit (fs)	Status
6	CC	3	1	5.000e+5	14.0	5.000e+5	14.0	1.000e+7	4.864	100.0	PASS
6	CC	3	2	5.000e+5	14.0	5.000e+5	0.73	1.000e+7	4.209	100.0	PASS
6	CC	3	3	5.000e+5	14.0	1.000e+6	14.0	1.000e+7	8.117	100.0	PASS
6	CC	3	4	5.000e+5	14.0	1.000e+6	0.73	1.000e+7	5.873	100.0	PASS
6	CC	3	5	5.000e+5	0.73	5.000e+5	14.0	1.000e+7	4.209	100.0	PASS
6	CC	3	6	5.000e+5	0.73	5.000e+5	0.73	1.000e+7	3.281	100.0	PASS
6	CC	3	7	5.000e+5	0.73	1.000e+6	14.0	1.000e+7	8.180	100.0	PASS
6	CC	3	8	5.000e+5	0.73	1.000e+6	0.73	1.000e+7	5.654	100.0	PASS
6	CC	3	9	1.000e+6	14.0	5.000e+5	14.0	1.000e+7	8.117	100.0	PASS
6	CC	3	10	1.000e+6	14.0	5.000e+5	0.73	1.000e+7	8.180	100.0	PASS
6	CC	3	11	1.000e+6	14.0	1.000e+6	14.0	1.000e+7	9.352	100.0	PASS
6	CC	3	12	1.000e+6	14.0	1.000e+6	0.73	1.000e+7	8.525	100.0	PASS
6	CC	3	13	1.000e+6	0.73	5.000e+5	14.0	1.000e+7	5.873	100.0	PASS
6	CC	3	14	1.000e+6	0.73	5.000e+5	0.73	1.000e+7	5.654	100.0	PASS
6	CC	3	15	1.000e+6	0.73	1.000e+6	14.0	1.000e+7	8.525	100.0	PASS
6	CC	3	16	1.000e+6	0.73	1.000e+6	0.73	1.000e+7	6.563	100.0	PASS

5.1.3 PNA Measurement Result, With SSC

Figure 5-3 is the phase noise plot of the LMK3H0102 output clock as measured by the PNA when SSC is enabled. The SSC is configured for –0.5% down-spread modulation. The 12 kHz to 20 MHz phase jitter is higher as SSC adds jitter, but much of this is filtered out when applying the PCIe filters. For CCS and SRIS, spurs from the fundamental frequency and harmonics are removed only up to 2 MHz. This is done to minimize removal of non-SSC related spurs.

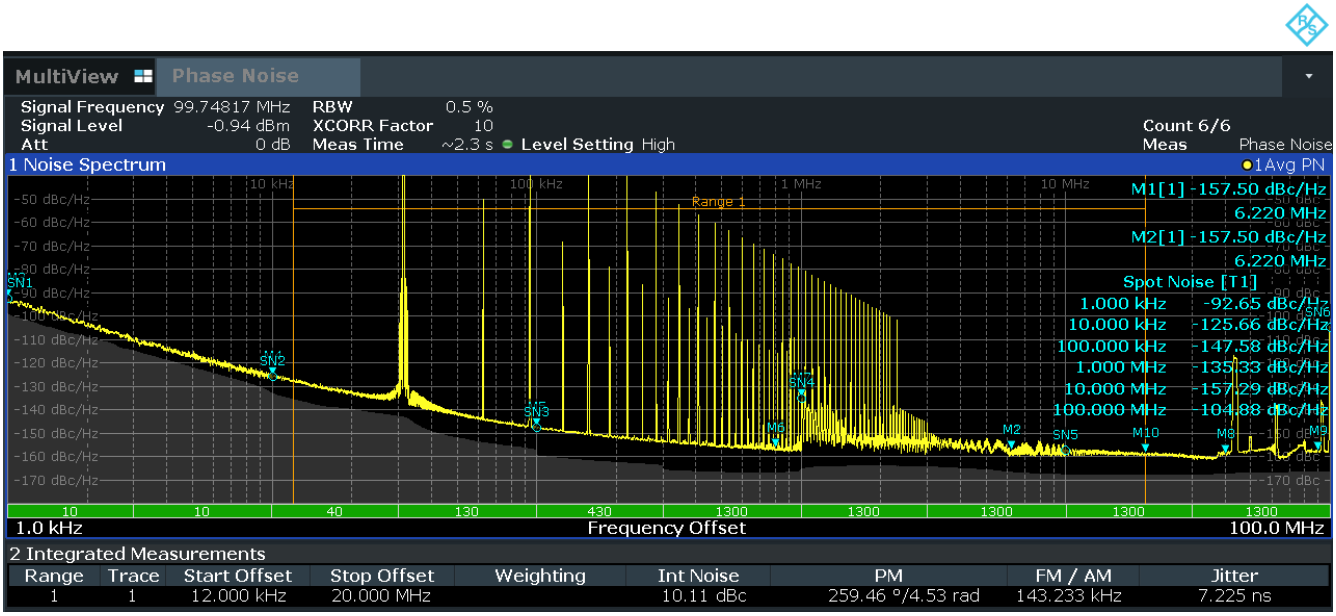

Figure 5-3. LMK3H0102 Phase Noise with SSC

5.1.4 PCIe Filtered PNA Result, With SSC

Table 5-3 shows the result of the SSC PNA capture after post processing using the PCIe Gen 6.0 filters. With the addition of SSC, each of the filter combinations continue to pass the PCIe Gen 6.0 limit of 100 fs of RMS jitter.

Table 5-3. LMK3H0102 Detailed PCIe Gen 6 Measurements, With SSC

PCIe Gen	Clock Architecture	Noise Fold	Filter Combination	PLL1 f_1	PLL1 ζ_1	PLL2 f_2	PLL2 ζ_2	CDR f_3	Jitter (fs)	Limit (fs)	Status
6	CCS	3	1	5.000e+5	14.0	5.000e+5	14.0	1.000e+7	10.825	100.0	PASS
6	CCS	3	2	5.000e+5	14.0	5.000e+5	0.73	1.000e+7	12.809	100.0	PASS
6	CCS	3	3	5.000e+5	14.0	1.000e+6	14.0	1.000e+7	19.740	100.0	PASS
6	CCS	3	4	5.000e+5	14.0	1.000e+6	0.73	1.000e+7	17.380	100.0	PASS
6	CCS	3	5	5.000e+5	0.73	5.000e+5	14.0	1.000e+7	12.809	100.0	PASS
6	CCS	3	6	5.000e+5	0.73	5.000e+5	0.73	1.000e+7	7.595	100.0	PASS
6	CCS	3	7	5.000e+5	0.73	1.000e+6	14.0	1.000e+7	22.194	100.0	PASS
6	CCS	3	8	5.000e+5	0.73	1.000e+6	0.73	1.000e+7	18.944	100.0	PASS
6	CCS	3	9	1.000e+6	14.0	5.000e+5	14.0	1.000e+7	19.740	100.0	PASS
6	CCS	3	10	1.000e+6	14.0	5.000e+5	0.73	1.000e+7	22.194	100.0	PASS
6	CCS	3	11	1.000e+6	14.0	1.000e+6	14.0	1.000e+7	21.601	100.0	PASS
6	CCS	3	12	1.000e+6	14.0	1.000e+6	0.73	1.000e+7	20.718	100.0	PASS
6	CCS	3	13	1.000e+6	0.73	5.000e+5	14.0	1.000e+7	17.380	100.0	PASS
6	CCS	3	14	1.000e+6	0.73	5.000e+5	0.73	1.000e+7	18.944	100.0	PASS
6	CCS	3	15	1.000e+6	0.73	1.000e+6	14.0	1.000e+7	20.718	100.0	PASS
6	CCS	3	16	1.000e+6	0.73	1.000e+6	0.73	1.000e+7	15.170	100.0	PASS

5.1.5 Time Domain PCIe Measurement Result

Figure 5-4 is the time domain capture of the OUT0_P and OUT0_N outputs of the LMK3H0102 as measured by the oscilloscope for the non-SSC case. These results are exported to text files, which can be read by the *Texas Instruments PCIe Reference Clock Analysis Tool* and analyzed for compliance.

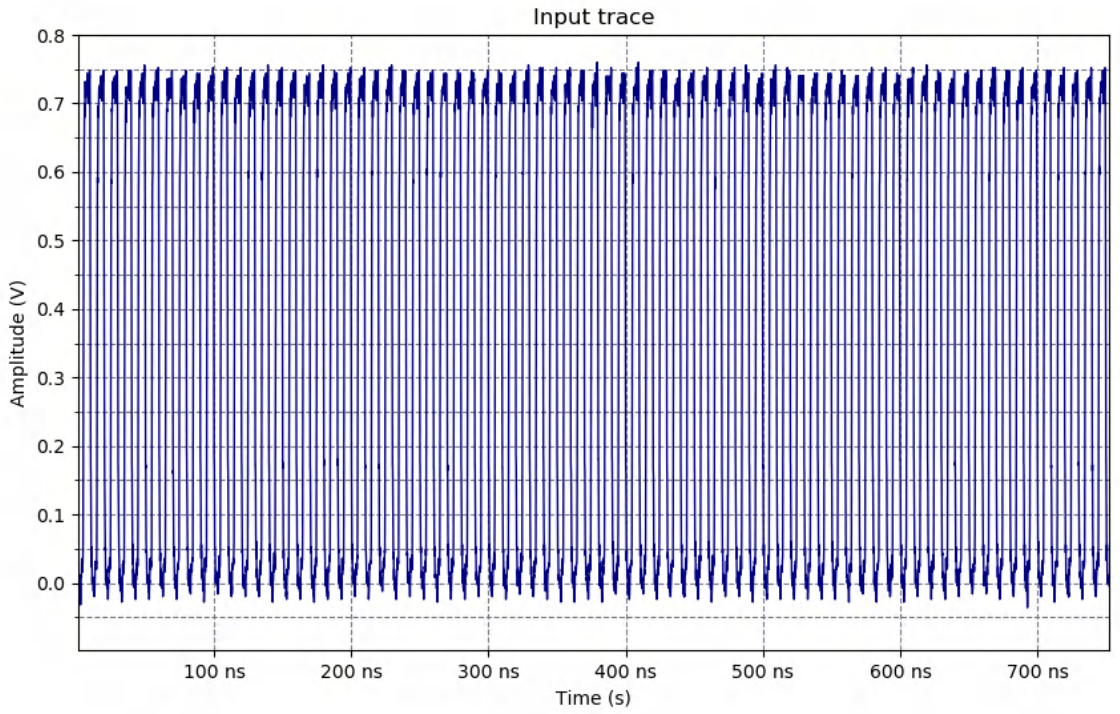

Figure 5-4. LMK3H0102 PCIe Time Domain Capture

Table 5-4 shows the result of the oscilloscope measurement after analysis. For the LMK3H0102, all of the parameters meet the limits specified in Table 4-2.

Table 5-4. LMK3H0102 PCIe Time Domain Results

Parameter	Units	Minimum	Average	Maximum	Limit	Status
V_{Cross}	mV	396.62	407.61	416.73	250 mV to 550 mV	Pass
V_{High}	mV	720.0	720.0		150 mV	Pass
V_{Low}	mV		–12.0	–12.0	–150 mV	Pass
$V_{Ringback}$	mV	621.9476	645.43		100 mV	Pass
Period	ns	9.9	9.996	10.1	9.847 ns to 10.203 ns	Pass
Duty Cycle	%	50.02	50.58	51.021	40% to 60%	Pass
$V_{Overshoot}$	mV		28.26	40.0	300 mV	Pass
$V_{Undershoot}$	mV		–32.28	–48.0	–300 mV	Pass
Rising Edge Rate	V/ns	2.24	2.584	2.92	0.6 V/ns to 4.0 V/ns	Pass
Falling Edge Rate	V/ns	2.12	2.612	3.08	0.6 V/ns to 4.0 V/ns	Pass

5.2 Clock Buffer Measurement Results

5.2.1 PNA Measurement Result

Figure 5-2 is the phase noise plot of the LMKDB1120 output clock as measured by the PNA. The 12 kHz to 20 MHz phase jitter is measured to be 57.2 fs. The PNA measurement is exported as a text file, from which we can import into the *Texas Instruments PCIe Reference Clock Analysis Tool* in TICS Pro. As PCIe Gen 6.0 requires data from 10 kHz to 50 MHz, the tool estimates the noise floor and extends the data to a full Nyquist band, 50 MHz.

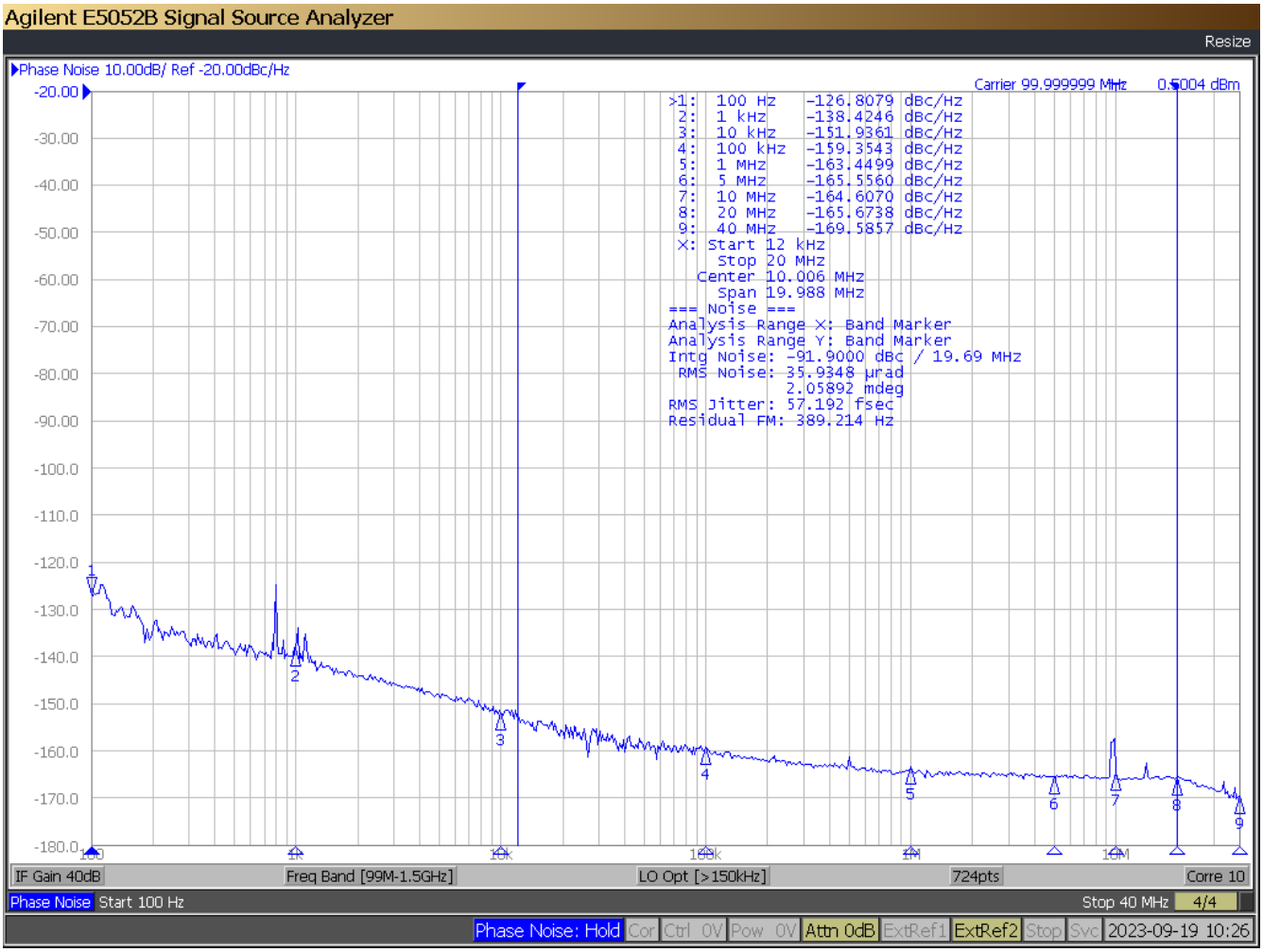

Figure 5-5. LMKDB1120 Phase Noise

5.2.2 PCIe Filtered PNA Result

Table 5-5 shows the result of the PNA capture after post processing using the PCIe Gen 6.0 filters. Each possible combination of PLL and CDR parameters is tested, resulting in 16 total filter combinations, all of which pass the PCIe Gen 6.0 limit of 100 fs of RMS jitter. The maximum noise fold is used in this case, with the noise floor extended to 200 MHz offset from the carrier.

Table 5-5. LMKDB1120 Detailed PCIe Gen 6 Measurements

PCIe Gen	Clock Architecture	Noise Fold	Filter Combination	PLL1 f_1	PLL1 ζ_1	PLL2 f_2	PLL2 ζ_2	CDR f_3	Jitter (fs)	Limit (fs)	Status
6	CC	3	1	5.000e+5	14	5.000e+5	14	1.000e+7	2.639059	100.0	PASS
6	CC	3	2	5.000e+5	14	5.000e+5	0.73	1.000e+7	2.384618	100.0	PASS
6	CC	3	3	5.000e+5	14	1.000e+6	14	1.000e+7	4.637093	100.0	PASS
6	CC	3	4	5.000e+5	14	1.000e+6	0.73	1.000e+7	3.323399	100.0	PASS
6	CC	3	5	5.000e+5	0.73	5.000e+5	14	1.000e+7	2.384618	100.0	PASS
6	CC	3	6	5.000e+5	0.73	5.000e+5	0.73	1.000e+7	1.848678	100.0	PASS
6	CC	3	7	5.000e+5	0.73	1.000e+6	14	1.000e+7	4.710578	100.0	PASS
6	CC	3	8	5.000e+5	0.73	1.000e+6	0.73	1.000e+7	3.227408	100.0	PASS
6	CC	3	9	1.000e+6	14	5.000e+5	14	1.000e+7	4.637093	100.0	PASS
6	CC	3	10	1.000e+6	14	5.000e+5	0.73	1.000e+7	4.710578	100.0	PASS
6	CC	3	11	1.000e+6	14	1.000e+6	14	1.000e+7	5.268353	100.0	PASS
6	CC	3	12	1.000e+6	14	1.000e+6	0.73	1.000e+7	4.836191	100.0	PASS
6	CC	3	13	1.000e+6	0.73	5.000e+5	14	1.000e+7	3.323399	100.0	PASS
6	CC	3	14	1.000e+6	0.73	5.000e+5	0.73	1.000e+7	3.227408	100.0	PASS
6	CC	3	15	1.000e+6	0.73	1.000e+6	14	1.000e+7	4.836191	100.0	PASS
6	CC	3	16	1.000e+6	0.73	1.000e+6	0.73	1.000e+7	3.697889	100.0	PASS

5.2.3 Time Domain PCIe Measurement Result

Figure 5-6 is the time domain capture of the OUT0_P and OUT0_N outputs of the LMKDB1120 as measured by the oscilloscope. These results are exported to text files, which can be read by the *Texas Instruments PCIe Reference Clock Analysis Tool* and analyzed for compliance.

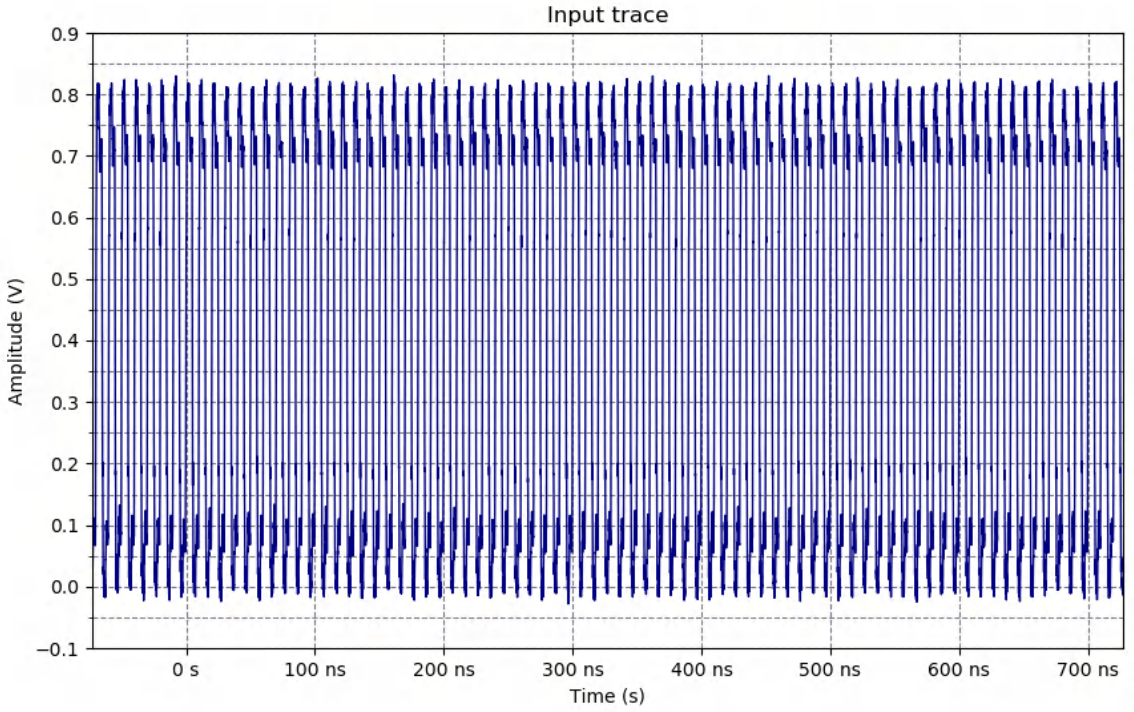

Figure 5-6. LMKDB1102 PCIe Time Domain Capture

Table 5-6 shows the result of the oscilloscope measurement after analysis. For the LMKDB1120, all of the parameters meet the limits specified in Table 4-2.

Table 5-6. LMKDB1120 PCIe Time Domain Results

Parameter	Units	Minimum	Average	Maximum	Limit	Status
V_{Cross}	mV	334.15	346.91	361.14	250 mV to 550 mV	Pass
V_{High}	mV	746.784	746.784		150 mV	Pass
V_{Low}	mV		–54.042	–54.042	–150 mV	Pass
$V_{Ringback}$	mV	557.354	586.954		100 mV	Pass
Period	ns	9.981	9.996	10.022	9.847 ns to 10.203 ns	Pass
Duty Cycle	%	49.343	49.493	49.663	40% to 60%	Pass
$V_{Overshoot}$	mV		69.48	84.82	300 mV	Pass
$V_{Undershoot}$	mV		–67.09	–82.29	–300 mV	Pass
Rising Edge Rate	V/ns	2.067	2.336	2.615	0.6 V/ns to 4.0 V/ns	Pass
Falling Edge Rate	V/ns	1.974	2.2	2.629	0.6 V/ns to 4.0 V/ns	Pass

6 Texas Instruments Products with PCIe Compliance

Texas Instruments offers a variety of clock generator and clock buffer products that meet the PCIe standards. Table 6-1 lists the products that have been evaluated for PCIe compliance. As stringency of the standard increases with PCIe generation, each product passes generations prior to the listed generation. PCIe reports are available on the product pages for the LMK3H0102 and LMKDB11xx device families.

Table 6-1. Texas Instruments PCIe Compliant Devices

Part Number	Product Family	Differential Outputs	Product Family Link	PCIe Generation Compliance
LMK3H0102	Reference-less BAW-based Clock Generator	2	LMK3H0102 Product Page	Gen 6.0
LMKDB1120 LMKDB1108 LMKDB1104 LMKDB1204 LMKDB1202	LP-HCSL Clock Buffers and Multiplexers	20 8 4 4 2	LMKDB11xx Product Page	Gen 6.0
LMK6H LMK6C (1)	Low Jitter High Performance BAW-based Oscillator	1 LVCMOS	LMK6H Product Page	6.0
CDCE6214 CDCE6214-Q1 CDCE6214Q1TM	Ultra-Low Power Clock Generators	4 4 4	CDCE6214 Product Page	Gen 5.0
LMK00338 LMK00334 LMK00334-Q1	LP-HCSL Clock Buffers and Level Translators	8 4 4	LMK00338 Product Page	Gen 5.0
LMK03328 LMK03318	Ultra-Low Jitter Clock Generator With Eight Outputs	8 8	LMK03328 Product Page	Gen 4.0
LMK00301 LMK00308 LMK00306 LMK00304	Ultra-Low Additive Jitter Differential Clock Buffer and Level Translator	10 8 6 4	LMK00301 Product Page	Gen 3.0

(1) The LMK6C can be used as the clock source for butter devices to provide LP-HCSL outputs with the industry-leading reliability benefits stemming from TI's BAW technology.

7 Summary

Systems that use PCIe must take care to plan the architecture appropriately. Each of the different architectures has tradeoffs, and the system designer must determine which one meets the requirements of their system. The addition of Spread Spectrum Clocking is an excellent choice for reducing EMI, but at the cost of adding complexity to the REFCLK design.

Both frequency and time domain specifications must be met to be compliant to PCIe. Selecting a low RMS jitter clock source is critical. Measuring PCIe jitter requires understanding PCIe filtering. Using a newer PNA allows for simple collection of non-SSC and SSC phase noise data for frequency domain analysis. The *Texas Instruments PCIe Reference Clock Analysis Tool* allows for rapid analysis of PNA and oscilloscope data to determine PCIe compliance.

The widespread use of PCIe and the need for increased data throughput needs requires clocking products. Texas Instruments offers a broad portfolio of clock generator and clock buffer products that meet the most demanding PCIe Gen 6.0 compliance. The *Texas Instruments Clocks and Timing Overview* provides further information on the PCIe compliant products available.

8 References

- Texas Instruments, *Texas Instruments Clocks and Timing Overview*.
- Texas Instruments, *Texas Instruments Clocks and Synthesizers (TICS) Pro Software*.

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