Application Report

Thermal Design and Performance of Top-Side Cooled QFN 12x12 Package for Automotive 650-V GaN Power Stage

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ABSTRACT

A new top-side cooled quad flat no-lead (ts-QFN) package has been developed by Texas Instruments (TI) for automotive-grade LMG352x family of 650-V gallium nitride (GaN) power stages. It has the same compact size of 12 mm x 12 mm x 0.9 mm as its bottom-side cooled QFN counterpart devices (LMG342x). This latest ts-QFN surface-mount package has an exposed copper thermal pad on the opposite side of its mounting pins. Enhanced thermal performance is realized by affixing a heatsink or coldplate directly on top of the package without thermal impediment caused by printed circuit board. While enabling direct driving and function integration, TI's new ts-QFN 12x12 package shows lower thermal resistance from device junction to system cooling plane than competitors' top-side cooled packages developed for discrete GaN devices. Taking advantage of top-side cooling configuration, system thermal performance and design flexibility can be improved for automotive applications like on-board charger and DC/DC converter.

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1 Introduction

As the trend of automotive electrification becomes more prevalent, the need for smaller, more reliable, and more efficient power conversion units such as on-board charger and high-voltage DC/DC converter is growing exponentially. Comparing with incumbent Silicon (Si)-based transistors and another wide-bandgap semiconductor Silicon Carbide (SiC)-based power switches, Gallium Nitride (GaN) high-electron-mobility transistor (HEMT) can better address the demand for high-power-density, high-efficiency automotive systems, thanks to its unrivaled high-frequency and efficient switching ability, see GaN and SiC enable increased energy efficiency in power supplies and Automotive GaN FETs engineered for high frequency and robustness in HEV/EVs. An optimized package solution is desirable for GaN HEMT to take greater advantage of its superior switching characteristics and adequately remove thermal energy to maintain system performance and device lifetime. Texas Instruments (TI) has developed a new generation of 650-V GaN power stages (LMG352xRxxx-Q1) for automotive applications that integrates a high-voltage GaN transistor with a fast-switching, 2.2-MHz Si gate driver with protection into a compact top-side cooled quad flat no-lead (ts-QFN) package in 12-mm x 12-mm x 0.9-mm dimension, see product release news. This leadless QFN package not only reduces parasitic inductances but also has an exposed thermal pad on its top side which allows the heat dissipation directly from device junction to the cooling components without hindrance by the mounting printed circuit board (PCB). Offering lower thermal resistance (R_{θ}) than other popular surface-mount type packages, the new top-side cooled QFN 12x12 package (ts-QFN 12x12) allows automotive designers to use smaller cooling system while simplifying thermal solutions with more design flexibility. In addition, the integrated digital temperature reporting function enables in situ system monitoring for active thermal management. This application report introduced the thermal management consideration and performance for the newly developed ts-QFN 12x12 package.

2 New Top-Side Cooled QFN 12x12 (ts-QFN 12x12) Package

The new ts-QFN 12x12 package has the identical footprint of 12 mm x 12 mm and typical thickness of 0.9 mm as TI's previously released bottom-side cooled QFN 12x12 package, as shown in Figure 2-1. The major difference between the two is the exposed copper (Cu) thermal pad location: the top-side cooled package has its thermal pad on the opposite side of the package from mounting pins, whereas the bottom-side cooled one on the same side as other pins for surface-mount on PCB. A more effective thermal management solution and optimized electrical design can be implemented simultaneously using top-side cooled package. Additionally, ts-QFN 12x12 package, featuring wettable-flank on the side of pins, enables automated optical inspection for solder joint quality control which is commonly requested by automobile manufacturers.

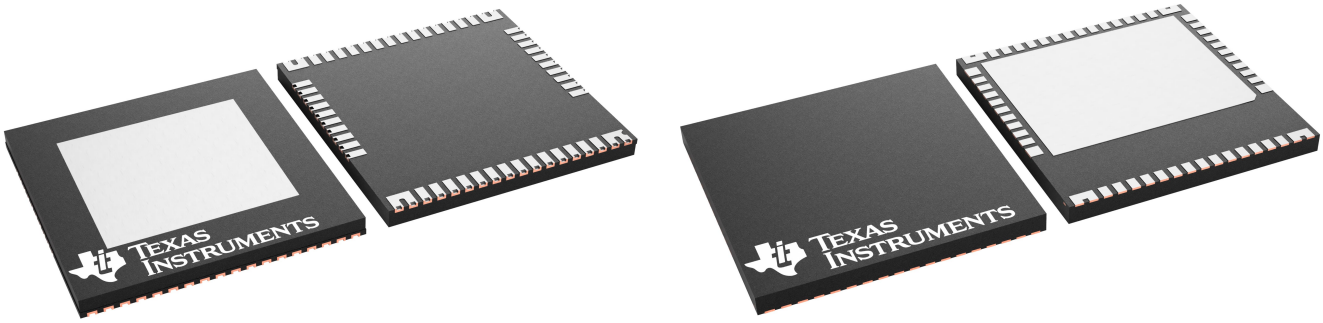
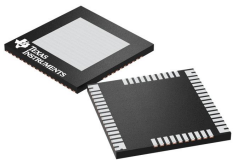
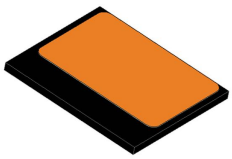
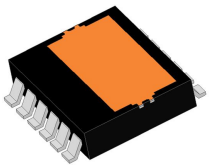


Figure 2-1. External Appearance of (a) ts-QFN 12x12 and (b) QFN 12x12 Packages

Top-side cooling provides an alternative heat dissipation route for surface-mount packages, which becomes an increasingly popular option adopted by many manufacturers. Table 2-1 compares the form factor and thermal pad size among three automotive-grade, 650-V GaN products packaged in the top-side cooled format. TI's ts-QFN 12x12 package has a larger exposed thermal pad than competitor A's package and a smaller overall size than the other which has the same thermal pad area as TI's. While competitors' GaN products are discrete devices, TI's 650-V GaN power stage has driving and protection being integrated into one package. Detailed package and thermal analysis will be discussed in the following sections.

Table 2-1. Dimensional Comparison of Top-Side Cooled Surface-Mount Packages for Automotive-Grade, 650-V GaN Devices

MANUFACTURER	TI	COMPETITOR A	COMPETITOR B
Package	 ts-QFN 12x12	 Embedded Package	 Leaded Package
Footprint (mm^2)	144	69	144
Thickness (mm)`	0.9	0.7	2.5
Exposed thermal pad area (mm^2)	64	46	64

3 Top-Side Cooling Configuration and Thermal Design Consideration

3.1 Top-Side Cooled Surface-Mount Package

Cooling for surface-mount type packages is challenging. Traditional QFN and other surface-mount packages have low thermal impedance (R_θ) to their bottom side where has the exposed Cu thermal pad. Cooling from package top side is not efficient and the main heat flow path on the bottom interferes with electrical layout on the PCB. Therefore, careful design tradeoffs have to be made between thermal dissipation pathway and electrical routing in order to optimize the performance for the power devices in bottom-side cooled packages. The high R_θ of PCB becomes the most limiting factor in this type of thermal design. Different board materials and/or structures, for example, Cu-inlay and ceramic-inlay boards, insulated metal substrate (see Thermal Comparison of FR-4 and Insulated Metal Substrate PCB for GaN Inverter), have been used to reduce the board and total R_θ with a higher cost than standard PCB.

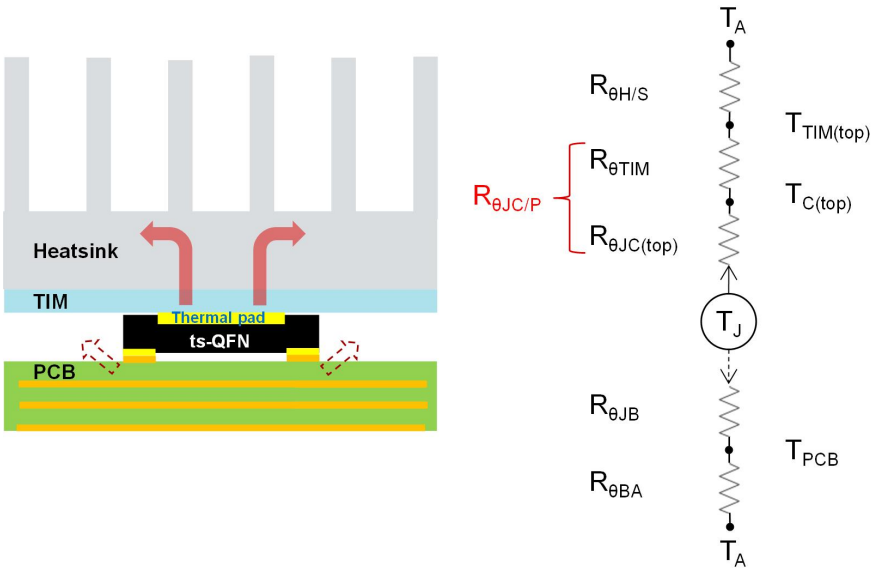


Figure 3-1. Top-Side Cooling Configuration and Thermal Resistance (R_θ) Model

Table 3-1. List of Thermal Resistance (R_θ) Parameters, Unit (°C/W)

SYMBOL	DESCRIPTION
$R_{\theta JA}$	Junction-to-ambient thermal resistance
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance
$R_{\theta BA}$	Board-to-ambient thermal resistance
$R_{\theta JC/P}$	**Junction-to-cooling plane thermal resistance**
$R_{\theta TIM}$	Thermal resistance of thermal interface material (TIM)
$R_{\theta H/S}$	Thermal resistance of heatsink

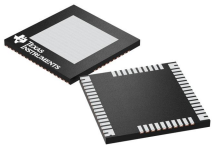
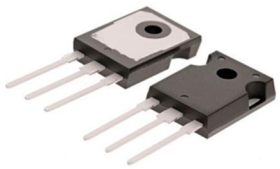
The top-side cooled surface-mount package allows heat to be easily removed from device by mounting the heatsink or coldplate directly to its exposed, top-side Cu thermal pad with a layer of thermal interface material (TIM) placed in between. Figure 3-1 illustrates such cooling design with an analogous one-dimensional R_θ circuit model. Most heat is dissipated from package top through TIM and heatsink to ambient. The descriptions of various R_θ parameters indicated in Figure 3-1 are summarized in Table 3-1. The defined junction-to-cooling plane thermal resistance $R_{\theta JC/P}$ can be simply calculated using Equation 1:

$$R_{\theta JC/P} = R_{\theta JC(top)} + R_{\theta TIM} \quad (1)$$

For the detailed explanation of using $R_{\theta JC/P}$ not $R_{\theta JC(bot\ or\ top)}$ or $R_{\theta JA}$ to evaluate package thermal performance at system level, please refer to Thermal Performance of QFN 12x12 Package for 600-V GaN Power Stage.

The developed ts-QFN 12x12 package has its thermal pathway decoupled from PCB in common with through-hole type packages like TO-247/220, but offers a significantly smaller body size and lower package parasitic inductance due to being leadless. QFN-type package has higher pin count on all four sides, enabling system integration of desirable functions into one package. Additionally, surface-mount type packages are capable of being automatically assembled on system board to save manufacturing cost. A comparison Table 3-2 showing different package features is presented below.

Table 3-2. Characteristic Comparison for Different Package Types

PACKAGE	ts-QFN 12x12(top-side cooled package)	TOLL / D2PAK (bottom-side cooled package)	TO-247
Mechanical drawing			
Package body size	Small (130 mm^3)	Medium (265 mm^3)	Large (1560 mm^3)
Thermal pathway decoupled from PCB	Yes	No	Yes
Typical parasitic inductance (PKG + PCB trace)	< 3 nH	> 5 nH	> 15 nH
Available pin count for driving/ function integration	> 50	< 8	3 or 4
Automatic assembly	Yes	Yes	No

3.2 Thermal Management Solutions

A number of thermal management solutions with various types of TIMs and cooling components can be utilized to lower the junction temperature (T_J) of top-side cooled devices. Figure 3-2 depicts two thermal design examples with heatsink attachment on two GaN power stages in ts-QFN 12x12 package mounted on a multilayer PCB. In one design, a large heatsink is attached on top of both devices using insulating adhesive tape as TIM. To improve thermal performance, high thermal conductive TIMs, such as gap filler pad, can be used with a suitable clamping method (e.g., fasten screws, push-pins, or clips) based on available space and needed pressure. Another cooling option is to use two smaller heatsinks which are individually bonded on the exposed top-side Cu thermal pad of each device by direct soldering. The R_θ of this solder joint layer is low; thus, the $R_{\theta JA}$ is mainly determined by the heatsink property in this design. Recommendations for heatsink/TIM selection and the clamping method can be found in application notes SNOA946 and SNOAA14.

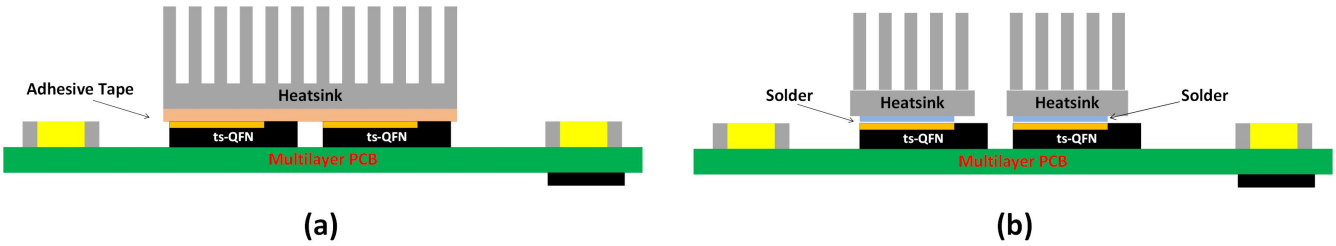


Figure 3-2. Heatsink Attachment on ts-QFN 12x12 Using (a) Adhesive Tape and (b) Solder Layer

For power conversion units used in electric vehicles (EVs), coldplate, instead of heatsink, is more commonly applied to cool not only active power switches but also other passive components by circulating liquid coolant through the system. Based on different TIMs, multiple thermal design options for ts-QFN 12x12 package with coldplate are demonstrated in Figure 3-3: (a) a cure-in-place, liquid-dispense gap filler gel TIM is used between coldplate and the top-side cooled package. The thickness of cured gel layer between coldplate pedestal surface and package thermal pad is controlled by the height of coldplate standoff and pedestal as well as the thickness of device package and solder layer. Thanks to the low-profile of ts-QFN 12x12 package (0.9 mm) gap filler gel can ramp around its sides before curing to provide additional cooling effect when in use. Fastening force can be exerted only on coldplate standoffs, therefore, minimal normal stress is applied on the package and solder joints.

Furthermore, the dispensable gel material has excellent conformability and good tolerance in component height variance and surface planarity across the board. Another typical TIM which can be utilized in the similar cooling configuration is a pre-cured, gap filler pad (b). A large sheet of solid pad can be automatically cut into the desired size and shape, then picked and placed onto coldplate for assembly. A compressive load is needed constantly to press the pad for making the intimate contact of adjoining surfaces. Higher pressure leads to a thinner TIM layer and thus lower R_{θ}. However, excessive force may damage the package and/or affect the solder joint integrity. In (c), a direct-bonded Cu (DBC) substrate is soldered on top of ts-QFN 12x12 package. The ceramic layer offers both high thermal conductivity and stable high-voltage isolation property. Hence, a thin layer (less than 150 um) of non-insulating thermal grease or phase change material could be compressed between coldplate and the top Cu layer of DBC substrate, displacing air and conforming to the contacting surfaces. This design offers the best thermal performance among the three enumerated examples, but with the tradeoff of the higher cost of ceramic substrate. Comparing gap filler gel and pad TIMs, the gel is more easily to conform to rough surface and tolerate variable gaps in a large system, while the latter usually has lower R_{θ} under the same bond line thickness of the TIM. For system thermal design, it is critical to ensure that distance between metal parts (e.g., exposed PCB Cu pads/traces, coldplate, and screws) and high-voltage devices meets regulatory safety requirements for creepage and clearance.

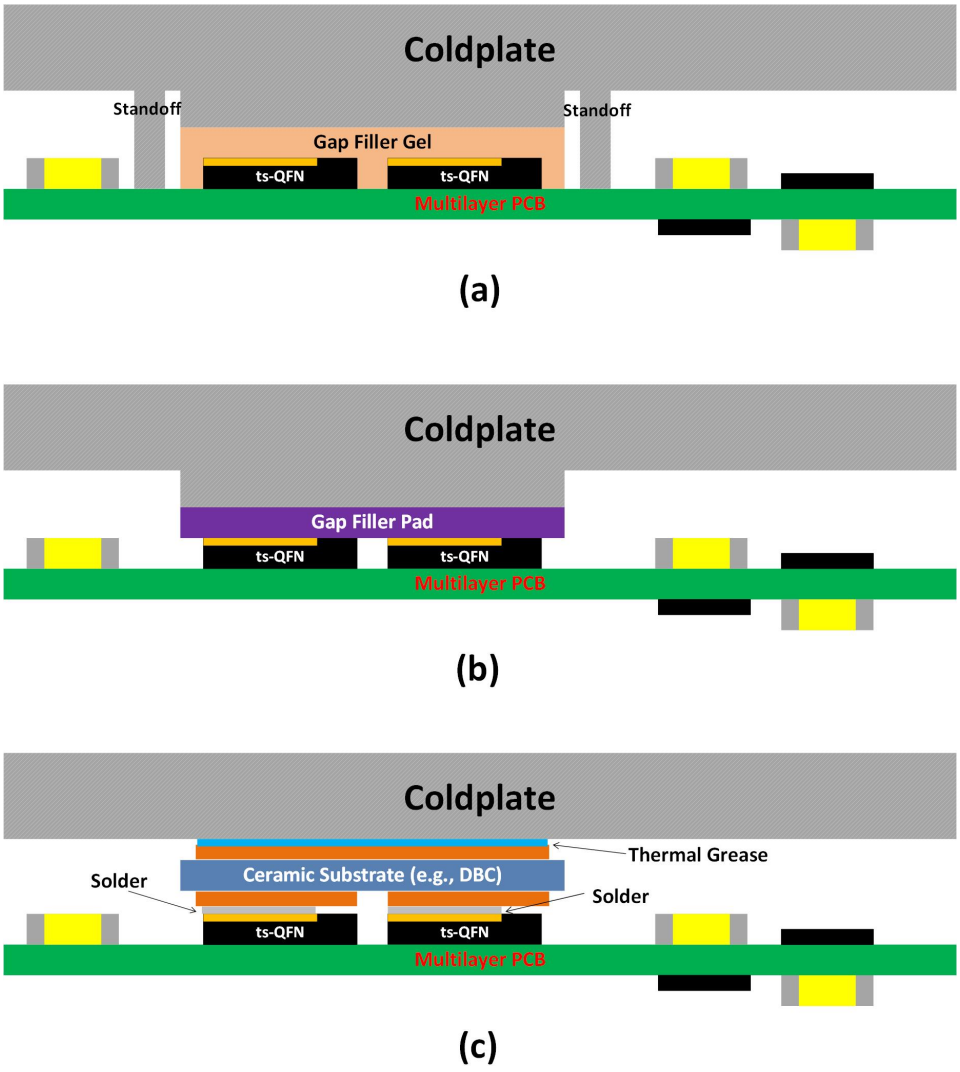


Figure 3-3. Thermal Management Solutions for ts-QFN 12x12 Package with Coldplate Using (a) Gap Filler Gel, (b) Gap Filler Pad, and (c) Thermal Grease/DBC Substrate

4 Thermal Simulation Models and Results

4.1 Simulation Models and Results for ts-QFN 12x12 Package

Two finite element analysis (FEA) simulation models were built using ANSYS tool, in order to evaluate the thermal performance of the ts-QFN 12x12 package with gap filler gel and pad TIMs. Figure 4-1 shows a cross-sectional view of the generated models and shows the structures of the thermal testing vehicles in accordance with experimental setup. The top-side cooled QFN 12x12 package is sandwiched by the PCB and coldplate, with a layer of TIM inserted between the package and coldplate. A thin polymer film and an aluminum (Al) frame with cut openings are used as standoffs to define the thickness of the TIM. For the design using gel TIM, the polymer film is under the Al frame, having its centered open window the same size as the package footprint, i.e., 12 mm x 12 mm. Comparing this model with the one using pad TIM, gel covers not only the package top surface but the surrounding four sides, which simulates the actual use case. Table 4-1 summarizes the thickness and thermal conductivity for major components used in thermal modeling.

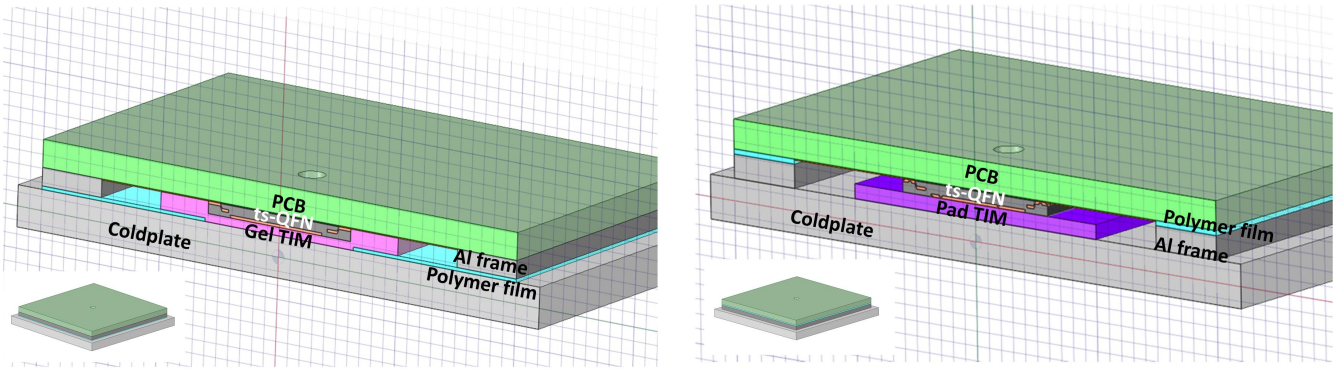


Figure 4-1. Thermal Simulation Models with: (a) Gel TIM and (b) Pad TIM

Table 4-1. Properties of Simulation Model Components

COMPONENT	THICKNESS (mm)	MATERIAL	THERMAL CONUCTIVITY (W/mK)
Solder	0.05	Lead-free solder	50
PCB	2.4	FR4	0.3
TIM	0.9	Gap filler pad	8
		Gap filler gel	3.8
Polymer film	0.25	Polyester film	0.15
Aluminum frame	1.6	Aluminum alloy	160
Coldplate	2.5		

The steady-state FEA thermal simulations were performed with a power loss of 10 W applied on device and a constant temperature of 30 °C set on coldplate. Natural convection condition was assumed on the PCB surfaces with ambient temperature set at 25 °C. The simulation results of temperature distributions for internal elements of the package (mold compound removed) with gel and pad TIMs are shown in Simulation Results of Temperature Distribution for ts-QFN 12x12 Package with (a) Gel TIM and (b) Pad TIM (a) and (b), respectively. The T_J can be directly obtained from simulation results and then used for $R_{\theta JC/P}$ calculation following the Equation 2 shown below:

$$R_{\theta JC/P} = (T_J - T_{coldplate}) / Power \quad (2)$$

The calculated $R_{\theta JC/P}$is 3.62 °C/W for gel TIM and 2.18 °C/W for pad TIM. The reason for a higher $R_{\theta JC/P}$ for the gel TIM is because the thermal conductivity of the gel used in the simulation is a typical value of 3.8 W/mK which is less than 8 W/mK of pad TIM. Experimental testing results of using different TIMs for the ts-QFN 12x12 package will be discussed in section 5.

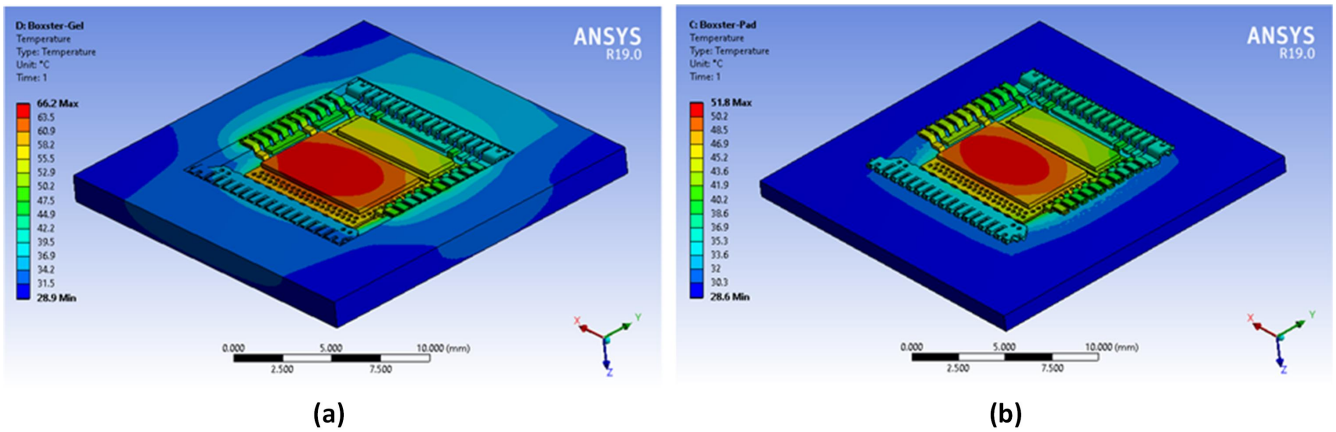


Figure 4-2. Simulation Results of Temperature Distribution for ts-QFN 12x12 Package with (a) Gel TIM and (b) Pad TIM

4.2 Competitive Analysis with Other Top-Side Cooled Packages

Similar FEA thermal models were constructed and thermal performance analyzed for competitors' 650-V GaN HEMTs with similar on-resistance ($R_{DS,ON}$) fabricated in top-side cooled packages. As introduced in Table 2-1, the other two packages have different form factors and sizes of exposed thermal pad from TI's ts-QFN 12x12 package. Based on simulation results, Figure 4-3 compares the calculated $R_{\theta JC/P}$ values for these three different GaN products using the same gel or pad TIM. It is clearly revealed that for the devices with similar $R_{DS,ON}$ of around 30 mΩ, the $R_{\theta JC/P}$ value of TI's ts-QFN 12x12 package is 20-30% lower than that of competitors' packages using either gel or pad TIM. Consequently, TI's GaN power stage in the top-side cooled QFN 12x12 package is capable of dissipating more power than the others. Competitor A's near chip-scale embedded package has the smallest and the thinnest top Cu pad and the heat spreading within the package is hence constrained. Therefore, the effective TIM area for its heat dissipation is smaller that results in a higher $R_{\theta TIM}$. The reason for a higher $R_{\theta JC/P}$ of competitor B's product in a leaded package, which has the same package footprint and thermal pad size as ts-QFN 12x12, is because its die position is not at the center of die-attach pad. Another comparison analysis had also been done for 50-mΩ devices which are packaged in TI's ts-QFN 12x12 format and competitor A's low-profile enclosure. Still, this newly developed ts-QFN 12x12 package demonstrates a competitive advantage with regard to thermal performance.

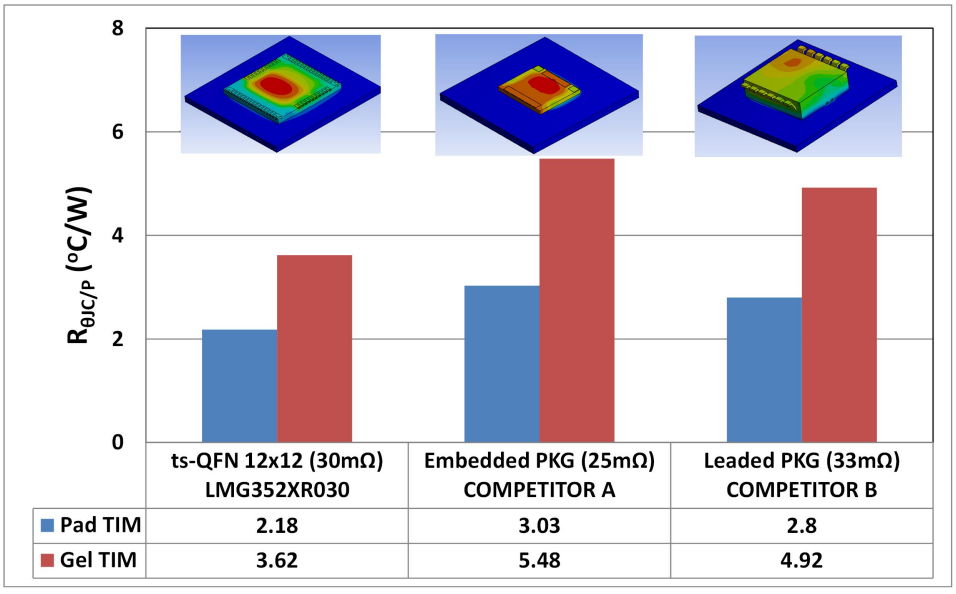


Figure 4-3. R_θ Simulation Result Comparison of Different Top-Side Cooled Surface-Mount Packages for 650-V GaN Devices

5 Experimental Setup and $R_{\theta JC/P}$ Testing Results

A thermal test bench setup for R_θ measurement has been designed and implemented in order to verify the thermal simulation results and to compare thermal performance using different TIMs under the same testing condition. The 30-mΩ LMG3522R030-Q1 in ts-QFN 12x12 package was selected as the device under test (DUT). As shown in conceptual drawings Figure 5-1 (a), the experimental setups have been assembled in the same manner with simulation models described in section 4. Both gel and pad TIMs can be tested using the same testing vehicle by changing polymer films with different cutout window sizes. Because the top-side cooled package mounting on PCB is flip clamped to coldplate, such configuration makes the direct detection of package surface temperature by infrared camera very difficult. It is therefore that a 2-mm diameter through-hole was drilled at the center of PCB, enabling the use of thermocouple to be inserted to monitor the package case temperature ($T_{C(bot)}$, opposite side of thermal pad). Another thermocouple tip was placed 2 mm underneath the top surface of coldplate to measure the cooling plane temperature ($T_{C/P}$). Figure 5-1 (b) presents the photo of real bench testing setup. A machined coldplate (Hi-Contact 6-Pass, Aavid) and a connected chiller unit (6560M, PolyScience) with running liquid coolant of 30 °C were employed as the cooling system. $T_{C(bot)}$ and $T_{C/P}$ were read and recorded by a data logger (OM-2041, Omega). To generate a controlled loss inside the package, direct current was used to heat the device junction, and the dissipated power was calculated by voltage and current measured across the DUT. As introduced in application note SNOAA61, the $R_{DS,ON} – T_J$ correlation fitting equation was formulated to calculate T_J using the same measured direct current/voltage results. The $R_{\theta JC/P}$ of ts-QFN 12x12 package with different pad TIMs in 1-mm thickness (0.9 mm after compression) and gel TIMs in both 0.9- and 0.6-mm thickness were evaluated.

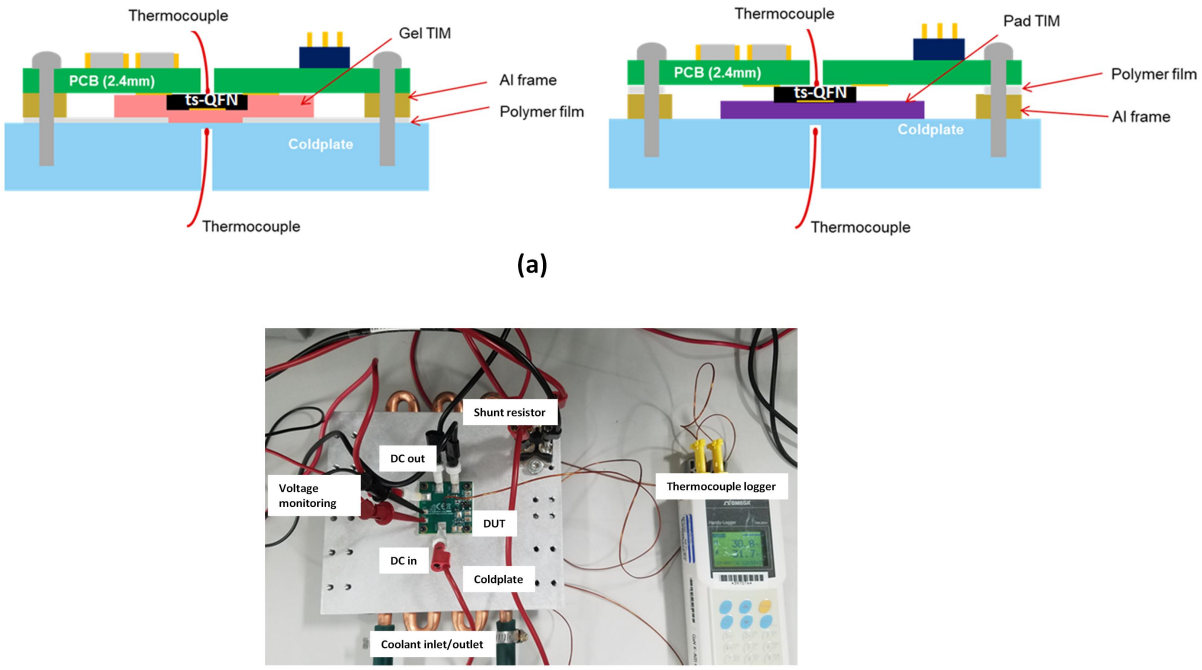


Figure 5-1. Experimental Setup for R_θ Measurement: (a) Cross-Section Illustration and (b) Top-View Photo

All testing results of $R_{\theta JC/P}$ calculated using $R_{DS,ON} – T_J$ fitting equation and measured $T_{C/P}$ are summarized in Table 5-1. The gap filler pad TIM GR80A from Fujipoly and gel TIM SC1500 from LORD were used as benchmark materials in both thermal modeling work and experimental testing. Specifically, simulated $R_{\theta JC/P}$ values with SC1500 gel and GR80A pad TIMs are 3.62 and 2.18 °C/W, respectively; comparing with experimental results of 3.72 and 2.27 °C/W accordingly, less than 4% discrepancy is observed for both types of TIMs. The accuracy of simulation model is verified, and so is the competitive analysis demonstrated in Figure 4-3. The slightly higher $R_{\theta JC/P}$ from testing could be explained by variations of the components (e.g., TIM thickness variation) and measurement setup, which are not considered in the simulation model.

Table 5-1. Experimental Results of $R_{\theta JC/P}$ Tested Using Different TIMs

TIM TYPE	PRODUCT	THERMAL CONDUCTIVITY (W/mk) on DATSHEET	THICKNESS (mm)	$R_{\theta JC/P}$ (°C/W)
Gap Filler Pad	GR80A	8	0.9	2.27
	XLIM-HL	10		2.65
	T-Work9000	20		1.83
Gap Filler Gel	SC1500	3.8	0.9	3.72
			0.6	2.95
	CGW4.5	4.5	0.9	3.38
			0.6	2.65
	TIA282GF	8.2	0.9	2.41
			0.6	2

As indicated in Figure 3-1 and Equation 1, the $R_{\theta JC/P}$for top-side cooled package includes only two components: $R_{\theta JC(top)}$ and $R_{\theta TIM}$. The $R_{\theta JC(top)}$ is typically less than 0.5 °C/W, which makes the selection of TIM ($R_{\theta TIM}$) even more critical than that for bottom-side cooled package. $R_{\theta JC/P}$ testing results for other commercially available TIMs are listed in Table 5-1. XLIM-HL pad TIM obtained from Sekisui shows a higher $R_{\theta JC/P}$ (2.65 °C/W) than benchmark GR80A pad (2.27 °C/W), but it has a lower dielectric constant which leads to a smaller parasitic capacitance generated between coldplate and package, showing benefit for high-frequency applications. Additionally, this pad material is silicone-free which is required for use cases where out-gassing and oil-bleeding are strongly concerned. LiPoly T-Work9000 reports a very high thermal conductivity of 20 W/mK on its datasheet, which is evidenced by the lowest tested $R_{\theta JC/P}$ result of 1.83 °C/W. And its ultra-softness property yields a lower compressive force on the package under the same compression ratio among all pad TIMs being tested. But as a rule of thumb, the higher thermal conductivity the more expensive of a TIM for a specific type. Tradeoff has to be made wisely to achieve the best performance/cost ratio. Two other gel TIMs, CGW4.5 (4.5 W/mK) from Sekisui and TIA282GF from Momentive (8.2 W/mK), were tested to compare with benchmark SC1500 material. All three products are two-component system, silicone-contained gap filler gels. The thermal performance comparison shows consistency between thermal conductivity values reported on datasheets and measured $R_{\theta JC/P}$ data – the higher the TIM thermal conductivity the lower the $R_{\theta JC/P}$. Showing a comparable thermal performance as pad TIM, TIA282GF gel can be used as a liquid-dispensable alternative to pre-cured gap filler pads.

6 Thermal Performance of Half-Bridge Evaluation Board (EVM)

6.1 EVM Thermal Designs with Coldplate and Heatsink

An evaluation board EVM (LMG3522EVM-042), consisting of two LMG3522R030-Q1 devices configured in a half-bridge topology, was built with two cooling solutions – coldplate and heatsink. A small customized coldplate was used and the same chiller unit applied for package thermal performance evaluation can also be used for testing this thermal management solution. A 35mm x 50mm x 20mm elliptical fin heatsink (UB3550-20B, Alpha Novatech) and 12-V, 1.68-W DC fan (F-3010H12BIII-16, Cofan) utilized for another evaluation board (LMG3422EVM-043) incorporating bottom-side cooled QFN 12x12 packages, were again selected to cool this new EVM board and compare with the other solution using coldplate. Figure 6-1 illustrates the exploded view of two assemblies. Both designs using the same 0.5-mm thick GR80A pad TIM between cooling component and ts-QFN 12x12 packages. For coldplate version, a plastic frame was inserted between Al coldplate and PCB to control the thickness of TIM while avoiding excessive stress applied on packages and providing more isolation protection. Four mounting screws were fastened from the top side of PCB to guarantee a seamless contact in between PCB, plastic frame, and coldplate. In cooling design with heatsink, four sets of push-pins and springs were used to apply a constant 20-psi pressure on two packages through the pad TIM which has the same deformed thickness as the one used in coldplate design.

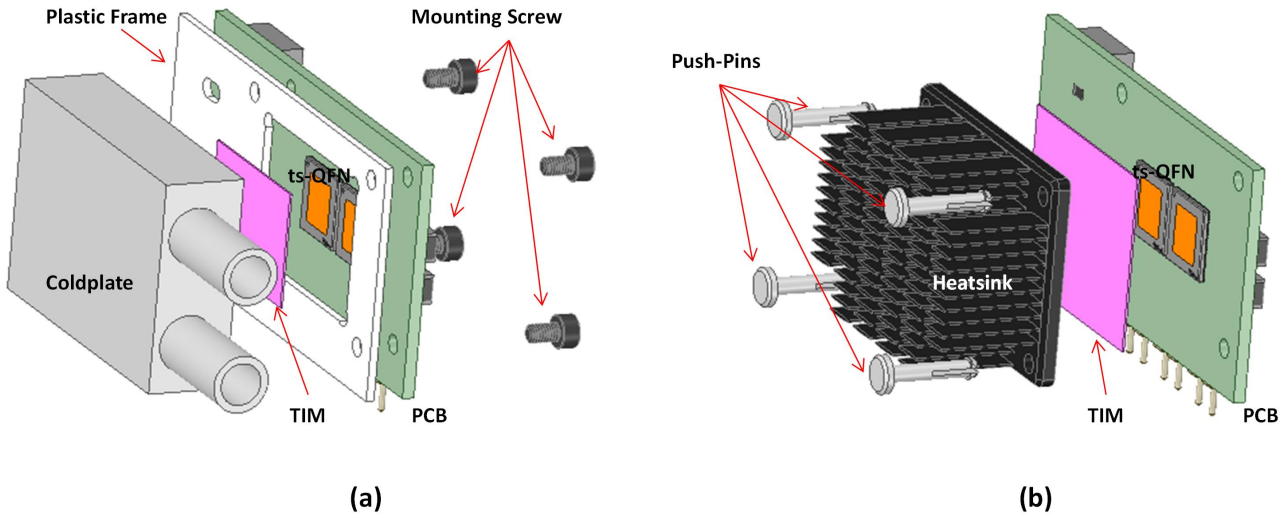


Figure 6-1. Exploded View of Evaluation Board Assemblies (LMG3522EVM-042) with (a) Coldplate and (b) Heatsink

6.2 Testing Results

The thermal performance of this evaluation board was assessed under two operating conditions: one is only single device being heated (e.g., Buck converter) and the other is two devices dissipating equivalent amount of thermal energy concurrently (e.g., PFC). Both coldplate and heatsink cooling systems were tested. The calculated $R_{\theta JCoolant}$ and $R_{\theta JA}$ results are presented in Table 6-1. It is shown that coldplate with running coolant provides more efficient cooling effect than heatsink with forced air for this EVM design. Junction-to-coolant R_θ of coldplate is about 1 and 1.5 °C/W lower than junction-to-ambient R_θ of heatsink for conditions 1 and 2, respectively. Due to the thermal coupling effect of two closely arranged ts-QFN 12x12 packages, R_θ for individual GaN device increases when both high-side and low-side devices are heated simultaneously, comparing to the R_θ value obtained from single heating source scenario. But the total power dissipation is actually higher when the half-bridge is operating at condition 2 as the effective R_θ (two paralleled resistors) for the system is lower.

Table 6-1. Measured R_{θ} with Different Cooling Methods

COOLING ELEMENT	COLDPLATE		HEATSINK	
R_{θ}	$R_{\theta JCoolant}$		$R_{\theta JA}$	
	($T_{Coolant}$ = 20 °C)		($T_{Ambient}$ = 25 °C)	
SWITCH	HIGH SIDE	LOW SIDE	HIGH SIDE	LOW SIDE
CONDITION 1 (Heating 1 switch)	1.67	-	2.8	-
CONDITION 2 (Heating 2 switches)	2.32	2.39	3.83	3.79

Figure 6-2 (a) shows the experimental setup of LMG3522EVM-042 with attached heatsink and DC fan. Two thermocouple wires were used to monitor the board temperature (T_B). Their tips were mounted on PCB in the proximity of each GaN device through the gap between heatsink and PCB. Taking advantage of the integrated temperature reporting function, GaN device T_J can be directly recorded from generated pulse width modulation (PWM) signals which can be converted to digital reading. The T_J and T_B results captured at different dissipation powers are plotted in Figure 6-2 (b). The T_J data obtained from $R_{DS,ON}$ correlation and PWM signal reading are in good agreement with each other, and the detected T_B is constantly lower than measured T_J at all examined power levels. To decouple heat from PCB by using top-side cooled package can allow device to operate at higher T_J without concerning PCB reliability for long-term use; while for the case of using bottom-side cooled package, device T_B and T_J are approximately the same because of the direct solder bonding between package thermal pad and its corresponding PCB landing pad. Therefore, the heated circuit board at elevated temperature close or above its glass transition temperature (110 – 130 °C for typical FR4 board) becomes the limiting factor for high power dissipation of bottom-side cooled surface-mount devices even though they have a higher T_J.

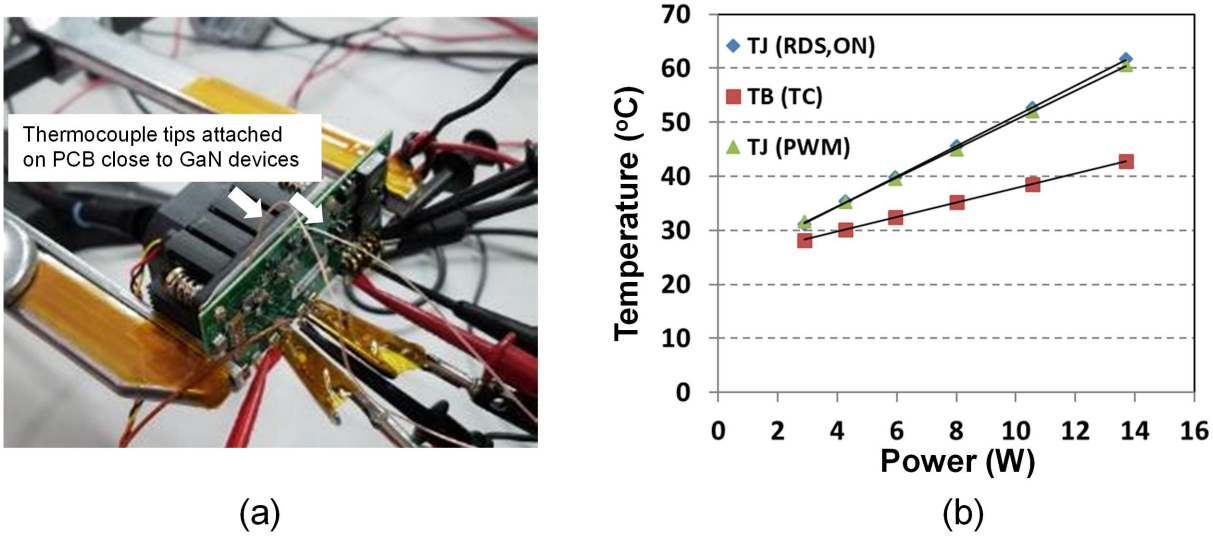


Figure 6-2. (a) EVM Thermal Performance Testing Setup with Heatsink and (b) Comparison of Measured PCB Temperature (T_B) and T_J Obtained by $R_{DS,ON}$ Correlation and PWM Signal under Different Power Levels

The thermal performance of LMG3522EVM-042 evaluation board mounted on the customized coldplate was characterized. The photos assembled daughter card are shown in Figure 6-3. It was mounted to the LMG342X-BB-EVM mother board for continuous synchronous Buck converter operation (Please see EVM User Guide SNOU178). The switching frequency is 100 kHz with 50% duty cycle, the turn-on slew rate is set to 100 V/ns, the dc-link voltage is 400 V, and output current is 30 A for 6-kW operation. The converter waveforms are shown in Figure 6-4 where blue is the PWM signal, green is the inductor current, and purple shows the switch-node waveforms. The T_J of the hard-switching device can be obtained from LMG352xR030 device's digital (PWM signal) junction-temperature output. At 6-kW output power, the hard-switching device's T_J stabilizes at 91 °C under a coolant temperature of 35 °C.

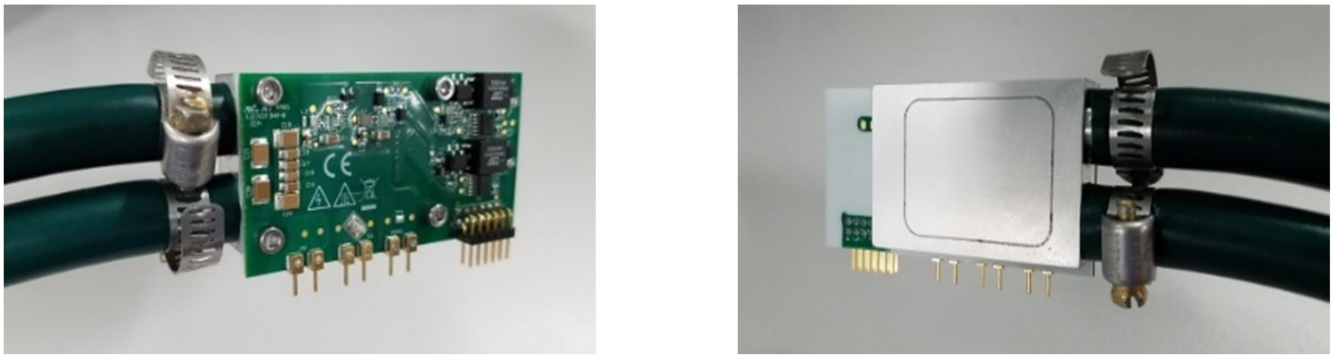


Figure 6-3. EVM Assembly with Coldplate (a) Front View (b) Back View

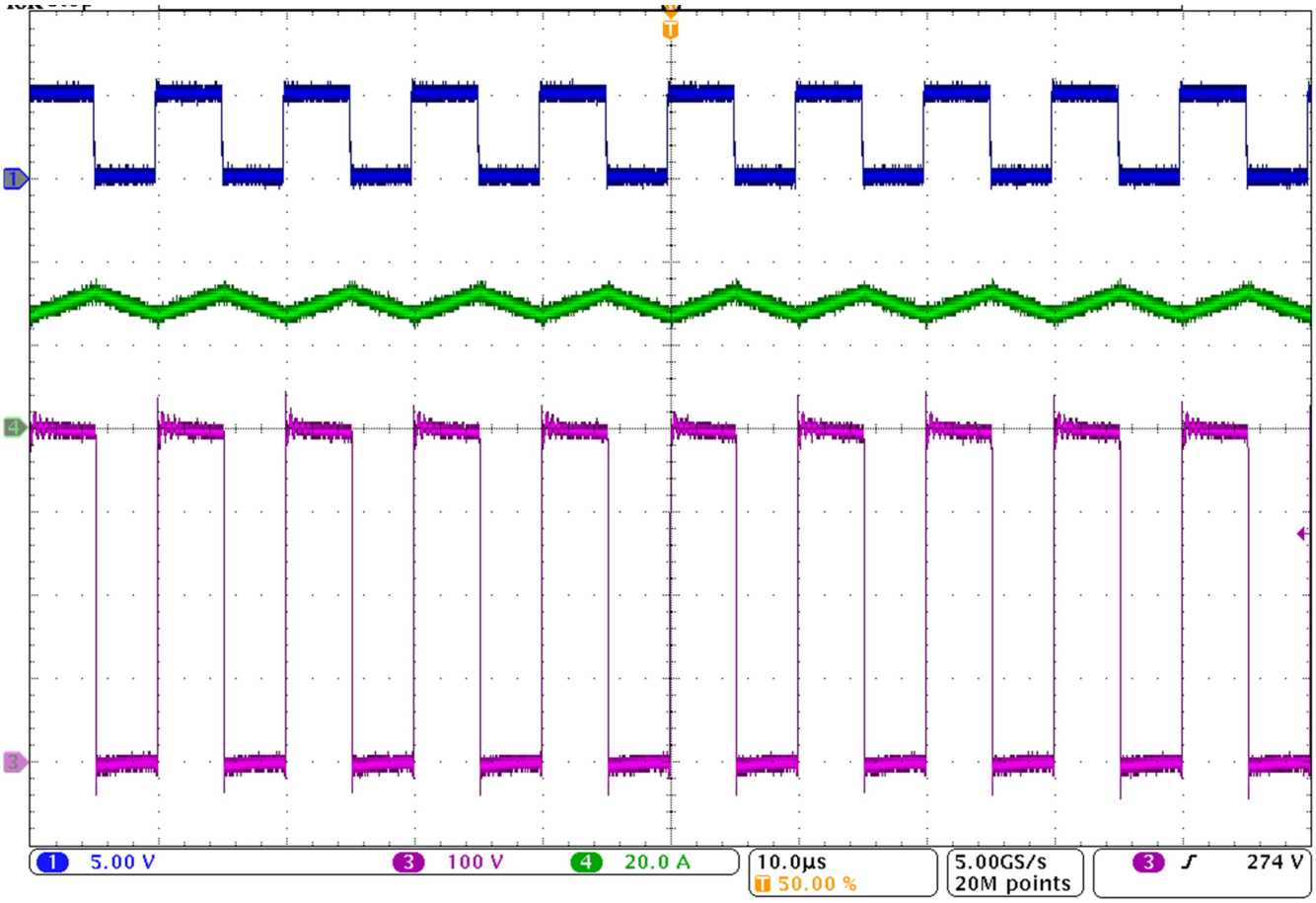


Figure 6-4. Buck Operation at 6 kW with Coldplate

7 Summary

To accelerate the adoption of EVs, more efficient power devices with thermally enhanced packages are needed to improve power density of power conversion units. A newly developed top-side cooled surface-mount package ts-QFN 12x12 for TI's LMG352x 650-V GaN power stages has been introduced to address this stringent thermal requirement for automotive applications. As demonstrated in simulation results, the $R_{\theta JC/P}$ value of this new package is about 20-30% lower than that of competitors' top-side cooled packages. Thermal bench testing results have validated the simulation analysis, showing less than 4% discrepancy. Furthermore, a practical half-bridge evaluation board was designed and manufactured using two LMG3522R030-Q1 units with interchangeable heatsink and coldplate as cooling devices. Its thermal characteristics were tested under various use cases. The measured junction-to-coolant R_{θ} could be as low as around 1.7 °C/W using coldplate setup and a 0.5-mm thick gap filler pad TIM. Moreover, the top-side cooling design not only provides an efficient thermal pathway for power device but also alleviates thermal stress on PCB side. While maintaining all the switching merits and integrated functions as TI's other GaN products, this automotive-grade, 650-V GaN power stage family in the new ts-QFN 12x12 package delivers enhanced thermal management solutions that can increase system power-density, improve reliability, and enable high-efficient power conversion for EVs.

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