Application Note

Industrial Communication Protocols Supported on Sitara™ Processors and MCUs

ABSTRACT

This application report shows the industrial communication protocols supported by each of the devices in the Sitara™ MCU+ and Sitara Arm® Cortex®-A processor portfolio, as well as where and how to get these protocols.

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Trademarks

1 Introduction

Industrial communication is typically handled by the Programmable Real-Time Unit Industrial Communication Subsystem (PRU-ICSS) in Sitara processors and microcontrollers (MCUs). The PRU-ICSS is a co-processor subsystem containing Programmable Real-Time (PRU) cores and Ethernet media access controllers (EMACs), which implement the low level industrial Ethernet and fieldbus protocols through firmware. The upper layers of the protocols stacks are implemented in software running on Arm cores. Three models for this protocol software are supported, full stacks from TI, 3rd party protocol stacks or a customer can use their own stack.

PRU cores are primarily used for industrial communication, and can also be used for other applications such as motor control and custom interfaces. The PRU-ICSS frees up the main Arm cores in the device for other functions, such as control and data processing.

This document describes certified industrial protocols supported directly by TI. The protocols are provided by TI and have been validated and certified on the evaluation boards. For production, the only requirement is to use a part number which enables the stacks. The MCU+ SDK Industrial Toolkit contains the binary version of the industrial communication protocol which run on AM64x and AM243x devices that enable full stack support designated with F (underlined and in bold) in the part number such as AM2432AS**F**GHAALXR. This is also shown in field f of the device-specific data sheet as shown in Figure 1-1. All evaluation modules, starter kits and launchpads use a part number enabling the stacks.

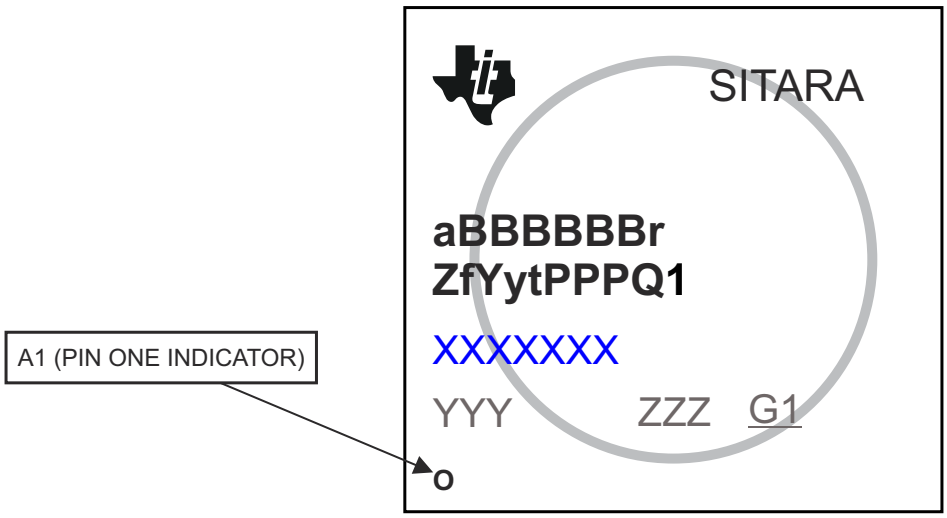

Figure 1-1. Package Marking (letter at location f determines support for full stacks)

The PRU-ICSS is flexible and powerful enough to support most industrial communications protocols. Currently the Sitara devices support 100-Mb versions of the protocols. The AM6x and AM243x families feature an upgraded PRU-ICSS that supports capability for gigabit speeds and Time Sensitive Networking (TSN) features. TI is continuously working both at TI and with the third party partners to expand offerings, so if a specific protocol is not explicitly shown in this document, reach out to TI through E2E or contact your local TI sales representative.

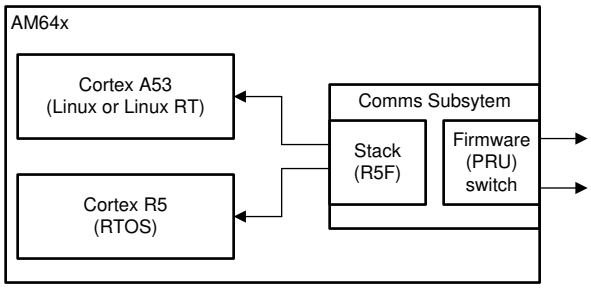

Figure 1-2. Implementation Using the Integrated Industrial Communication Stack

Sitara further supports protocols supported by TI firmware with a third party stack, as well as several other protocols supported by third party partners. AM335x, AM437x, and AM57x families support this 3rd party model. For AM64x and AM243x the third party model is supported as well for all part numbers except for the letter C (at location f). For a comprehensive list of all third parties supporting PRU-ICSS industrial communication, see Processors Third Party Search Tool.

2 Communication Protocols

2.1 PROFINET

Sitara AM64x and AM243x families currently have support for PROFINET® RT and IRT device. The supported feature set is summarized in Table 2-1.

Table 2-1. Supported Feature Set

Feature	Description	Relevant Conformance Class	Support
Mandatory Features CC-A			
Real Time Cyclic - Class 1	Unsynchronized real time cyclic protocol	CC-A,B,C	Yes
Real Time Acyclic	Real-time acyclic protocol	CC-A,B,C	Yes
Device diagnostics/Alarms	Diagnostics and Maintenance Alarms	CC-A,B,C	Yes
Device identification (I&M0)	Supported mandatory Identification records	CC-A,B,C	Yes
Neighborhood detection	LLDP protocol	CC-A,B,C	Yes
Port-related network statuses via PROFINET	PDEV records	CC-A,B,C	Yes
Optional Features CC-A			
Extended Identification & Maintenance	Supported extended I&M records	CC-A,B,C	I&M1, 2, 3, 4
Shared Input	Multiple access to inputs by various controllers	CC-A,B,C	In planning
Shared device	Distribution of device functions to various controllers	CC-A,B,C	In planning
Slave-to-slave communication	Direct communication between IO-Devices	CC-A,B,C	No
Mandatory Features CC-B			
Network diagnostics	SNMP protocol	CC-B,C	Yes
Optional Features CC-B			
Name assignment via DCP, PDEV	Automatic addressing of devices after device replacement	CC-B,C	Yes
Configuration in Run (CiR)	Configuration changes during operation	CC-B,C	In planning
Time sync	Time stamping of I/O data	CC-B,C	Yes
Fibre-optic cable Support	Fiber-optic cable diagnostics for POF/HCS	CC-B,C	No
Fast Start-Up	Fast start-up after voltage recovery for switching operations	CC-B	In planning
Media redundancy protocol	Higher availability through ring redundancy	CC-B	In planning
System redundancy (Mandatory only for PA)	System redundancy with two I/O Controllers	CC-B	In planning
Mandatory Features CC-C			
PROFINET with IRT	Bandwidth reservation with update rates of 250 us and higher	CC-C	Yes
PROFINET with IRT	Isochronous operation	CC-C	Yes

Table 2-1. Supported Feature Set (continued)

Feature	Description	Relevant Conformance Class	Support
	Update rates less than 250 us	CC-C	No
DFP	Optimized IRT mode for line topologies	CC-C	No
Two-way transmission, MRPD	Higher availability through harmonious redundancy switchover	CC-C	No

2.2 EtherCAT

Sitara AM64x and AM243x families currently have support for EtherCAT® slave. EtherCAT is supported by ICSS-PRU on part numbers with E or F in the location f of the full part number. The EtherCAT stack in MCU+ SDK will run on F part numbers. For E part numbers the EtherCAT slave stack is available for free for EtherCAT Group (ETG) members, and can be found on their website. The supported feature set is summarized in Table 2-2.

Table 2-2. Supported Feature Set

Feature	Description	Implementation
Distributed Clocks	By using distributed clocks the EtherCAT real-time Ethernet protocol is able to synchronize the time in all local bus devices within a very narrow tolerance range.	Yes
Object Dictionary	Freely definable, only limited by available resources	Yes
CiA 402	This profile standardizes the functional behavior of controllers for servo drives, frequency inverters, and stepper motors.	Yes
Mailbox Queue	Mailbox services will be stored in a queue. Mailbox services can be processed in parallel.	Yes
AoE	ADS over EtherCAT service support.	No
CoE	CANopen over EtherCAT service support.	Yes
Complete Access support	Accessing all entries of an object with one SDO service is supported.	Yes
Segmented SDO support	Segmented SDO service is supported.	Yes
SDO Response Interface	If a SDO response cannot be generated immediately, return ABORTIDX_WORKING.	Yes
Diagnosis support	Diagnosis messages are supported.	Yes
Emergency support	Emergency messages are supported.	Yes
VoE	Vendor Specific Protocol over EtherCAT service support.	No
SoE	Sercos over EtherCAT service support.	Yes
EoE	Ethernet over EtherCAT service support.	Yes
FoE	File access over EtherCAT service support.	Yes
OP State requires process data	Transition from SafeOP to OP State requires process data.	Yes
Explicit device ID	Explicit device ID requests are handled.	No
Error Counters	RX Invalid Frame Counter Port 0/1	Yes
	RX ERR Counter Port 0/1	Yes
	Forwarded Error Counter Port 0/1	Yes
	ECAT Processing Unit Error Counter	Yes
Fieldbus Memory Management Units (FMMU)	Convert logical addresses into physical addresses by means of internal address mapping	4
SYNC Manager	Insure consistent and secure data exchange between EtherCAT master and local application of slave device	4

Table 2-2. Supported Feature Set (continued)

Feature	Description	Implementation
EtherCat Commands	NOP, APRD, APWR, APRW, FPRD, FPWR, FPRW, BRD, BWR, BRW, LRD, LWR, LRW, ARMW and FRMW	All supported
Processdata	Maximum Input	1024 Bytes
	Maximum Output	1024 Bytes
	Cycle time	
Cycle Time	Free run	31.25 µs
	DC mode	100 µs
Distributed Clocks	Accuracy	64-bit
	SYNC0	Generation single shot and cyclic mode support
	SYNC1	SYNC1 cycle time multiple of SYNC0 cycle time

2.3 EtherNet/IP

Sitara AM64x and AM243x families currently support EtherNet/IP® adapter. The supported feature set is summarized in Table 2-3.

Table 2-3. Supported Feature Set

Feature	Description	Implementation
EtherNet/IP Device Class	Adapter	Yes
	Scanner	No
Device Profile	Generic Device	Yes
Device Configuration	EDS File	Yes
Connection Types	Exclusive Owner	Yes
	Input Only	Yes
	Listen Only	Yes
Connection Trigger Types	Cyclic	Yes (1 ms)
	Application Triggered	no
	Change of State	Yes
Maximum Connections	Class 1	8
	Class 3	32
Explicit Messaging	Connected	Yes
	Unconnected	Yes
Standard Objects	Identity Object (0x01)	Yes
	Message Router Object (0x02)	Yes
	Assembly Object (0x04)	Yes
	Connection Manager Object (0x06)	Yes
	Device Level Ring Object (0x47)	Yes
	QoS Object (0x48)	Yes
	TCP/IP Interface Object (0xF5)	Yes
	Ethernet Link Object (0xF6)	Yes

Table 2-3. Supported Feature Set (continued)

Feature	Description	Implementation
Supported Elementary Data Types	BOOL	Yes
	SINT	Yes
	INT	Yes
	DINT	Yes
	LINT	Yes
	USINT	Yes
	UINT	Yes
	UDINT	Yes
	ULINT	Yes
	REAL	Yes
	LREAL	Yes
	STRING	Yes
	BYTE	Yes
	WORD	Yes
	DWORD	Yes
	LWORD	Yes
	STRING2	Yes
	SHORT_STRING	Yes
	EPATH	Yes
Supported Constructed Data Types	Formal Array	Yes
IP Addressing Modes	DHCP	Yes
	BOOTP	Yes
	Static	Yes
VLAN tagging	IEEE802.1Q, 3 bit PCP (8 levels)	Yes
	Switch queues	8
Statistics	Media counters supported per interface (dual port switch)	Yes
	Interface counters supported per interface	Yes
CIP Sync (PTP/IEEE1588)	Supports Drives Profile : E2E clock	Yes
	PTP over UDP	Yes
	Transparent Clock supported	Yes
	Ordinary Clock supported	Yes
	Single and Two step clock supported	Yes
Supported Network Features	Device Level Ring (DLR) - Beacon based	Yes
	Address Conflict Detection (ACD)	Yes
	Quality of Service (QoS)	Yes
	CIP Reset Services	Identity Object Reset Services of Typ 0, 1, and 2
Device Level Ring (DLR)	Beacon based	Yes
	Self configuring	Yes
	Min. beacon interval	200 µs
	Min. beacon timeout	400 µs
Baud Rate	100 Mbit/s	Yes
	10 Mbit/s	Yes
Duplex Mode	Half	No
	Full	Yes
	Auto-Negotiation	Yes

Table 2-3. Supported Feature Set (continued)

Feature	Description	Implementation
Conformance		ODVA CT18

2.4 IO-Link

Sitara AM64x and AM243x families currently provide support for the IO-Link® master.

Table 2-4. Support Feature Set

Feature	Description	Implementation
IO-Link Types	IO-Link Master	Yes
IO-Link Standards	IO-Link Specification IEC 61131-9 V1.1.2 (V1.0 backwards compatible)	Yes
	IO-Link Specification IEC 61131-9 V1.1.3	Yes (depends on ratification)
	IODD V1.1	Yes
Communication Classess	Com1, Com 2, Com 3 (4.8, 38.4, 230.4 Kbit/s)	Yes
Telegram Types	0, 1, 2.1, 2.2, 2.3, 2.4, 2.5	Yes
Max. IO-Link Channels	8	Yes
IO-Link Stack	Hardware interface (BSP, HW control)	Yes
	Message handler	Yes
	Application layer (on-request data objects, process data objects)	Yes
	System management	Yes
	Data storage (master)	Yes
	Standard master interface via API	Yes
	Standard master interface via UART	Yes
Device Configuration	IO-Link Master Configuration Tool	Yes

2.5 Simple Open Real-Time Ethernet (SORTE)

Sitara processors currently support SORTE using PRU-ICSS. SORTE is an open-source protocol developed by TI. AM64x MCU+ SDK will include a giga-bit version of SORTE.

2.6 Parallel Redundancy Protocol (PRP)

Sitara processors currently support 100M PRP using ICSS. The ICSS based solution offloads the duplicate removal on receive. The AM64x/AM243x version will be available later. For Sitara AM335x/AM437x/AM57x evaluation and production software is available through the HSR/PRP firmware add-on package for the RTOS version of the Processor SDK, or through the Linux version of the Processor SDK.

Additional resources:

- http://www.ti.com/tool/TIDEP0054 (RTOS TI Design)
- http://www.ti.com/tool/TIDEP-0103 (Linux TI Design)

2.7 High-Availability Seamless Redundancy (HSR)

Sitara processors currently support 100M HSR using ICSS. The AM64x/AM243x version will be available later. For Sitara, AM335x/AM437x/AM57x evaluation and production software is available through the HSR/PRP firmware add-on package for the RTOS version of the Processor SDK, or through the Linux version of the Processor SDK. The ICSS-based solution supports cut through switching and further offloads the duplicate removal on receive and the maintenance of the node table.

Additional resources:

- http://www.ti.com/tool/TIDEP0053 (RTOS TI Design)
- http://www.ti.com/tool/TIDEP-0096 (Linux TI Design)

2.8 OPC UA

Sitara processors currently support OPC UA server (device or endpoint) using TI's Ethernet MAC using either PRU-ICSS or CPSW. Below is a link to an open source OPC UA server stack from open62541.org.

Additional Resources:

- TI Design
- Documentation on open62541.org stack

2.9 Modbus TCP/IP

Though not yet certified on Sitara, Modbus TCP/IP can be implemented on any Sitara processor through the use of open source stacks, and TI's Ethernet MAC using either PRU-ICSS or CPSW. Linked below are examples of open source stacks that could potentially be used. For help in getting this running in your design, ask our experts at e2e.ti.com.

Additional resources:

- Modbus for Linux: https://libmodbus.org/
- Modbus for RTOS: https://github.com/cwalter-at/freemodbus

3 Position Encoders

The firmware for each of the supported encoders below is offered as open source.

3.1 EnDat 2.2

Sitara processors currently support EnDat. Evaluation and production software is available MCU+ SDK. The supported features are listed below:

- EnDat 2.2 command set
- EnDat 2.1 command set
- Interrupted and continuous clock mode
- Clock configuration up to 16 MHz
- Cable length up to 100m @ 8 MHz
- Propagation delay compensation (capable of handling different propagation delay of different channels in concurrent multi-channel configuration)
- Automatic estimation of propagation delay
- Receive on-the-fly CRC verification of position, parameters and additional information
- Two modes of operation - host trigger and periodic trigger
- Channel select
- Concurrent multi-channel support (up-to 3 encoders with identical part number @ 8 MHz maximum)

3.2 HIPERFACE DSL

Sitara processors currently support HIPERFACE DSL®. Evaluation and production software is available MCU+ SDK. The supported features are listed below.

- External pulse synchronization
- Safe position
- Supports up to 100m cable
- Communication status
- Register interface to be compatible with SICK HDSL FPGA IP Core. (except registers that have different functionality for read and write)
- Parameter channel communication (short message write)

3.3 Tamagawa

Tamagawa will be supported in a later release of AM64x and AM243x MCU+ SDK. Evaluation and production software is available through the industrial drives firmware add-on package for the TI-RTOS version of the Processor SDK for AM437x family of devices.

3.4 BiSS- C

BiSS will be supported in a later release of AM64x and AM243x MCU+ SDK. The BiSS® C encoder solution for AM437x is available from CouthIT. For licensing or evaluation, contact CouthIT.

4 Sitara Support for 3rd Party Protocol Stacks

For protocols supported by TI firmware with third party stack, firmware and drivers are available from TI as add-on packages that run on top of the MCU+ SDK, or come integrated as part of the Linux SDK. In addition to the protocols listed in otehr sections in thsi docuemnt firmware is available for PROFIBUS. On older TI RTOS based Processor SDK releases for AM335x, AM437x and AM57x the protocols are available from the add on package PRU-ICSS Industrial Sofware Package. Protocol stacks are typically purchased through one of TI's third party partners. Figure 4-1 shows a typical use case for industrial communications on Sitara processors and MCUs for protocols supported by TI firmware with third party stack. For a comprehensive list of all third parties supporting PRU-ICSS industrial communication, see Processors Third Party Search Tool.

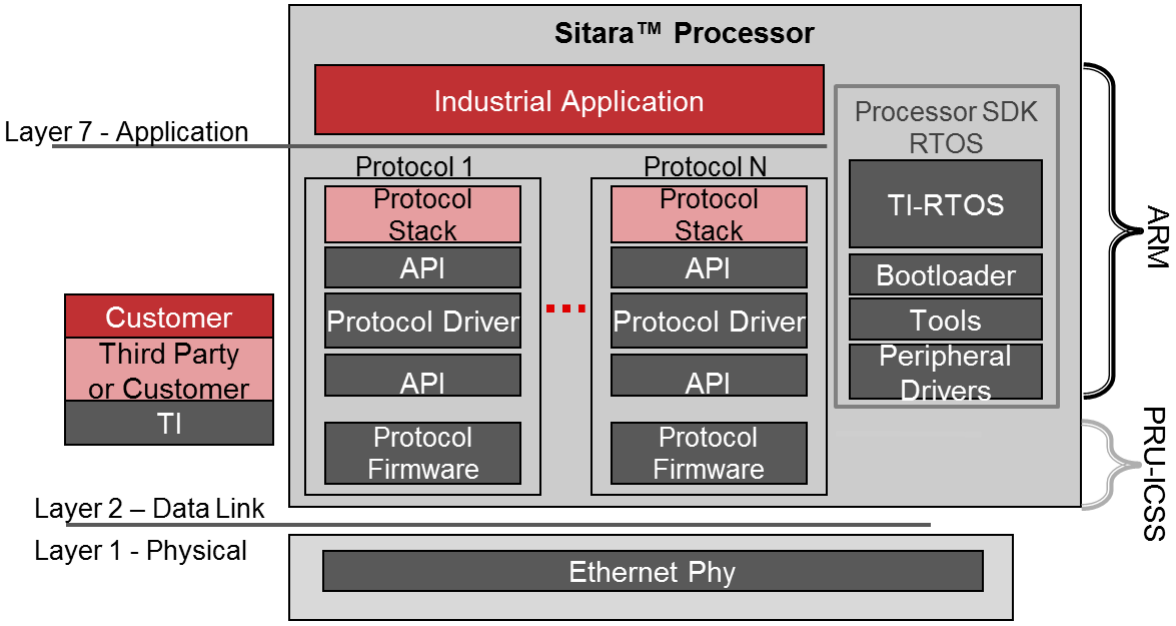

Figure 4-1. Software Implementation Using the PRU-ICSS and a Third Party or Customer Stack

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2021) to Revision E (May 2024)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Updated *Introduction* section	2

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