

# Solve the Challenge of Too Many Wires in High-speed Networking Equipment



Guilherme Borba

Top-of-rack (ToR) switches, routers, servers and storage, types of today's [high-speed communications equipment](#), are among the most sleek, powerful and meticulously designed workhorses of the data center. They contain impressive circuitry, pushing +25Gbps with scores of ports, complex switch *application-specific integrated circuits* (ASICs) and sophisticated signal-conditioning devices.

It is very easy to forget that for every high-speed port (small form-factor pluggable (SFP), quad small form-factor pluggable (QSFP), serial attached small computer system interface (SAS) and so on) there are between four and nine low-speed signals associated with that port that need managing. This means that, for a high-port-count system such as a 48-port ToR switch, there may be more than 400 low-speed signals. That's a lot of wires!

To route and manage all of these signals, typical implementations involve high-pin-count field-programmable gate arrays (FPGAs), I<sup>2</sup>C multiplexers, shift registers, LED drivers and an extra printed circuit board (PCB) layer. These approaches are difficult to implement, crowd the board and do not scale easily – that is, until now. TI's [FPC401](#) quad-port controller enables a much simpler solution to this design challenge.

The result is a system with a 100 times reduction in signal routing across the board, a 100 times reduction in FPGA pin count, the elimination of many space-consuming discrete components and an overall simplification of port management – see [Figure 1](#).

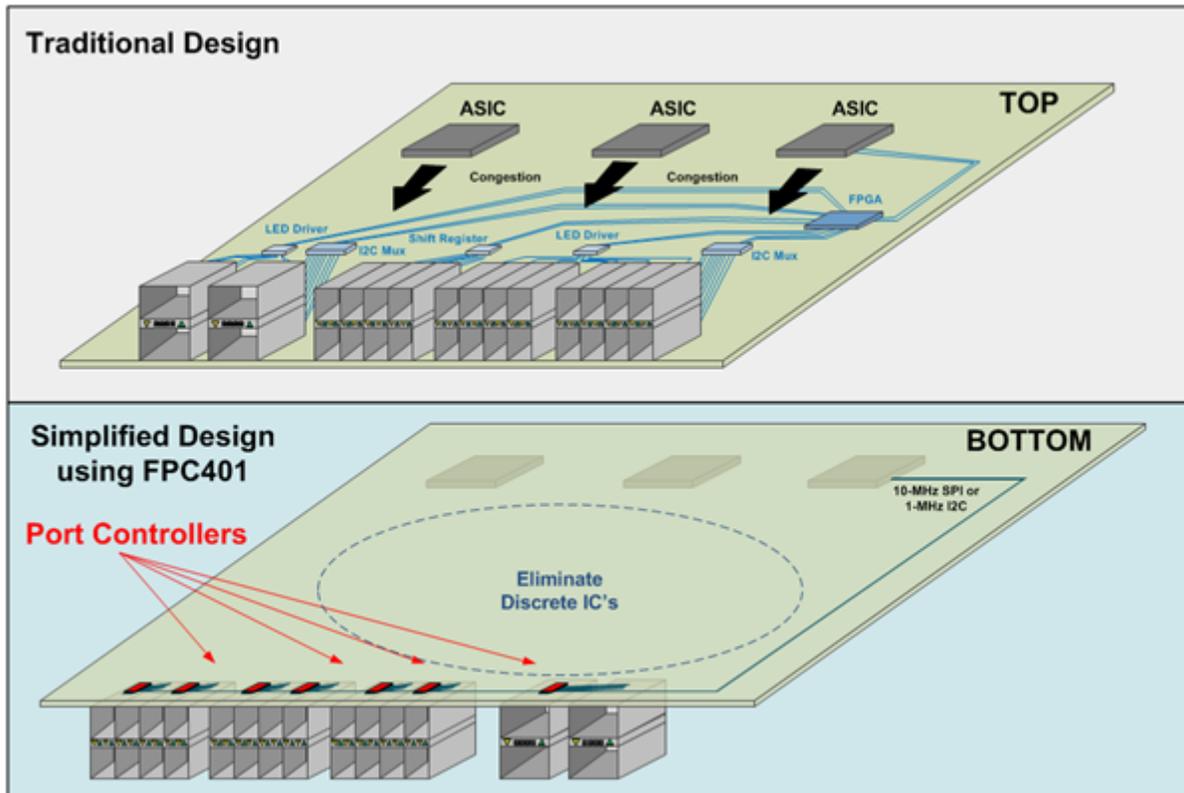
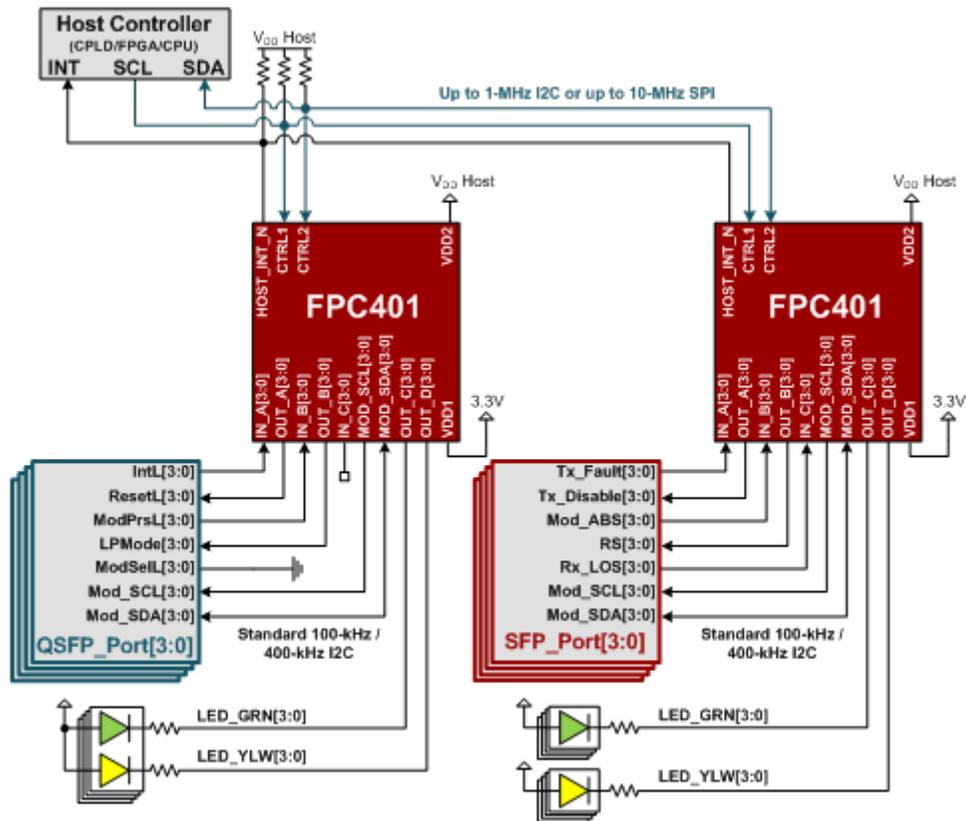


Figure 1. A traditional solution vs. an FPC401-based solution

The FPC401 aggregates all low-speed signals for up to 56 ports into a single, fast I<sup>2</sup>C bus (up to 1MHz) or a serial peripheral interface (SPI) bus (up to 10 MHz), greatly reducing routing complexity and simplifying design scalability. The FPC401 has three inputs, four outputs and an I<sup>2</sup>C master for each of the four ports, enabling full control of the downstream module. Refer to [Figure 2](#) for examples of SFP and QSFP connections.



**Figure 2. FPC401 simplified schematic for a typical application**

Each input has interrupt-generating capabilities to alert the host to important events, such as an unplugged module. There are multiple general-purpose outputs, as well as two special-purpose outputs that have advanced LED driving capabilities with blinking and brightness control. Each port's I<sup>2</sup>C master operates independently, which enables reading and writing across all ports simultaneously. The FPC401 has features to simplify your system software, such as periodic pre-fetch of module data and handling of module I<sup>2</sup>C protocol mishaps. The best part is that the FPC401 is small enough to fit underneath the SFP or QSFP cage, on the bottom side of the board.

A downloadable C function library makes the integration of the FPC401 into your system a seamless process. The [FPC401EVM](#) evaluation board allows you to test the functionality of the FPC401 with your own host controller or an on-board [MSP430™](#) microcontroller.

It may be easy to forget the numerous low-speed signals in high-speed applications, and with the FPC401's help, you can implement this part of your circuit quickly and turn your focus toward the more important high-speed portions of your design.

Heading to DesignCon? Stop by TI Booth 1234 and see the FPC401 port controller in action!

### Additional Resources

- Learn more about the [FPC401 port controller](#).
- Download the [FPC401 data sheet](#).
- Interested in high-speed systems? Check out these posts from the Eye Doctor blog series:
  - [“Eye doctor: Why too much equalization boost is bad for your serial link health”](#).
  - [“Eye doctor: Reflections and how to deal with them in high-speed systems”](#).

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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