Achieving Better Signal Integrity With Isolated Delta-Sigma Modulators in Motor Drives

Pawan Nayak

ABSTRACT

High-performance servo control is crucial to various industrial manufacturing processes which use motor drives for example, in applications like computer numerical control (CNC) machining, pick-and-place machines, and industrial robots. The performance of control algorithms implemented in a servo drive depends on accurate motor current feedback. Multiple isolated delta-sigma modulators are used on a servo drive printed-circuit board (PCB) to sense the motor currents, motor phase voltages, and the DC link voltage. The modulators require a high-frequency clock signal to send out synchronized single-bit data streams back to the micro-controller unit (MCU). Improper routing schemes of clock and data signals on the PCB can create signal-integrity issues and sample and hold violations. This application note discusses the best practices for clock and data line routing and termination when using isolated delta-sigma modulators.

Contents

List of Figures

List of Tables

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

Figure 1 shows a generic high-voltage drive inverter. Typically inside a drive, the controller and the power stage reside on two separate PCBs. The control board is common and the power-stage PCB changes across a drive platform based on its output power levels. Most often, two delta-sigma (ΔΣ) modulators are used for motor-phase current sensing while the third phase current is calculated for a balanced three-phase system. Motor-phase voltages and the inverter DC link voltage can also be sensed using voltage dividers and ΔΣ modulators depending on the control-algorithm requirements. The modulators generally reside on the power board and the clock and data signals have to be routed between the power and control boards. The two boards can either be connected through stackable connectors or through flat cables.

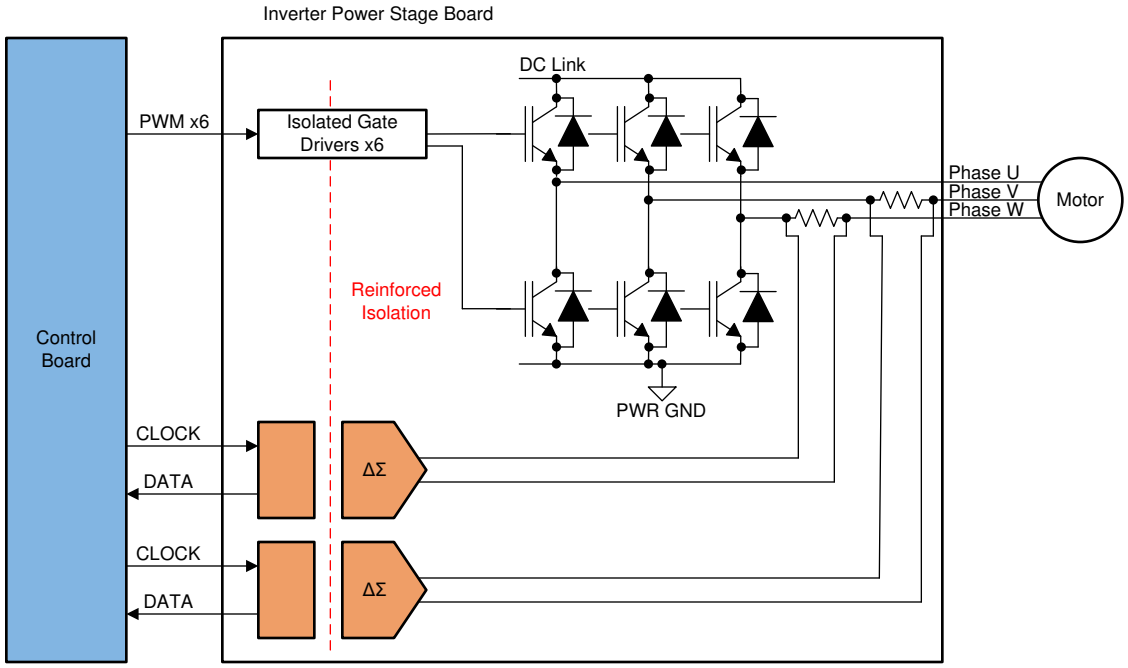

Figure 1. Generic Motor Drive Inverter

Clock and data signal routing varies from drive to drive depending on PCB rules, circuit design and layout, and connector placement. A set of general guidelines are provided in this application note to get the best possible signal integrity. This document focuses on delta-sigma modulators which are driven with an external clock signal like the AMC1306M25 device.

2 Clock Signal Routing

Depending on the placement of the delta-sigma modulators on the PCB, the clock signal may have to be routed using the daisy-chain approach (Figure 2) or star-routing approach (Figure 3). Both of these approaches face signal integrity challenges. Line termination schemes become necessary to reduce reflections and provide a proper interface between the MCU and modulators.

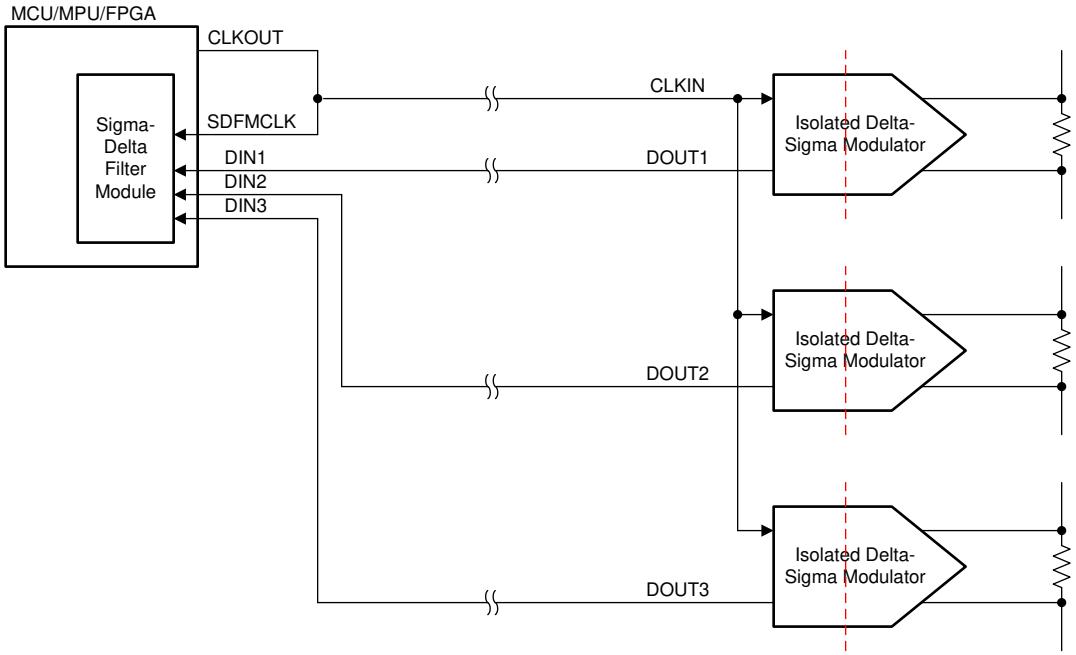

Figure 2. Daisy-Chain Clock Routing

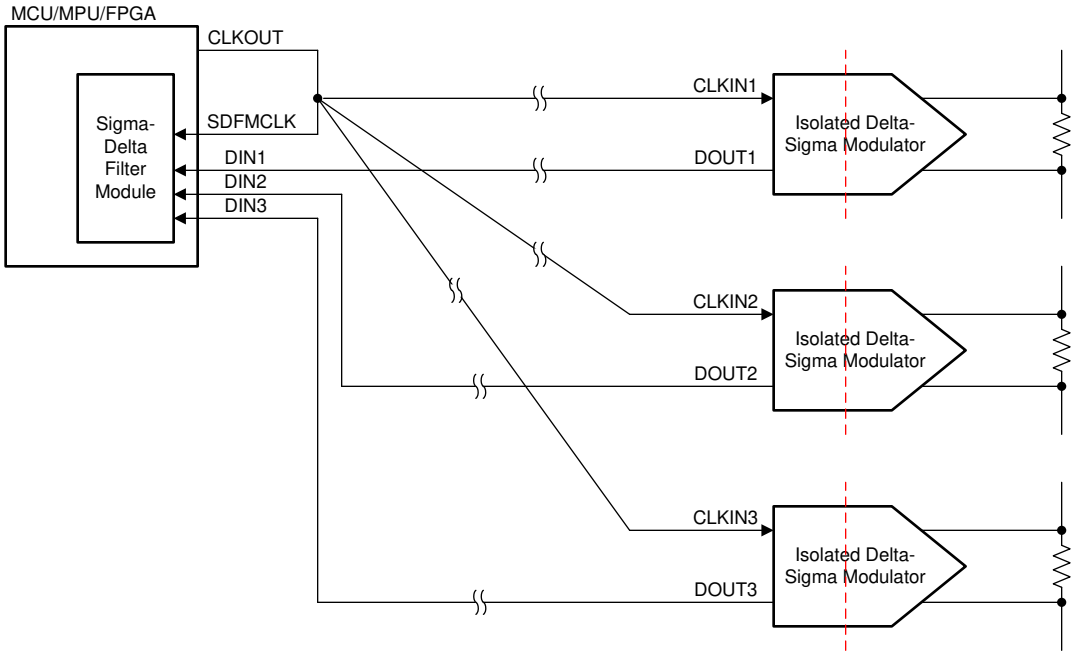

Figure 3. Star Clock Routing

The goal of termination is to match the impedance of the signal traces at the end of the transmission line so as to reduce signal reflection. Multiple termination configurations are possible such as series, parallel, Thevenin, and AC termination. Each of these termination configurations has pros and cons. This section presents the best possible termination mechanism.

2.1 Daisy-Chain Clock Routing Configuration Example

Figure 4 shows a test PCB with a TMS320F28379D MCU which generates the 20-MHz clock signal from its PWM peripheral driven into a clock buffer SN74LVC2G17D device. The output of the buffer is split into two traces; one goes back to the MCU Sigma-Delta Filter Module (SDFM) peripheral and the other drives three AMC1306 modulators in a daisy-chain routing configuration.

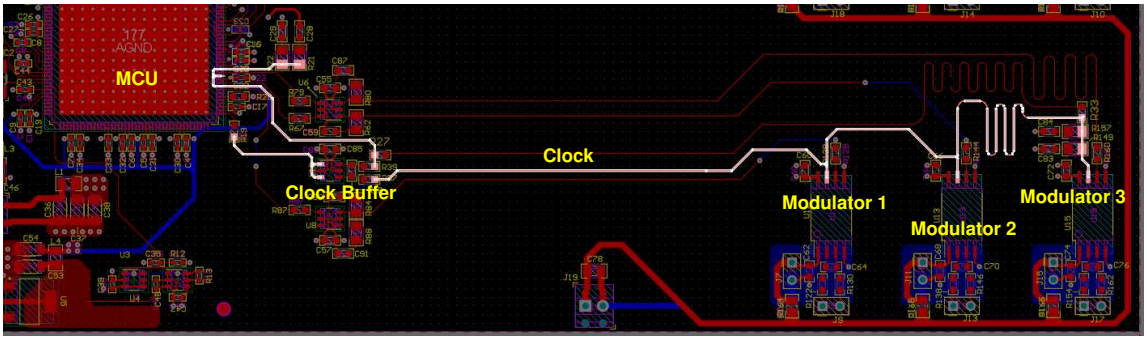

Figure 4. Daisy-Chain Routing Example

The traces on the PCB are impedance-controlled to 50 Ω. If no termination is done on the PCB, significant over- and undershoots can occur on the clock signal as Figure 5 and Figure 6 show.

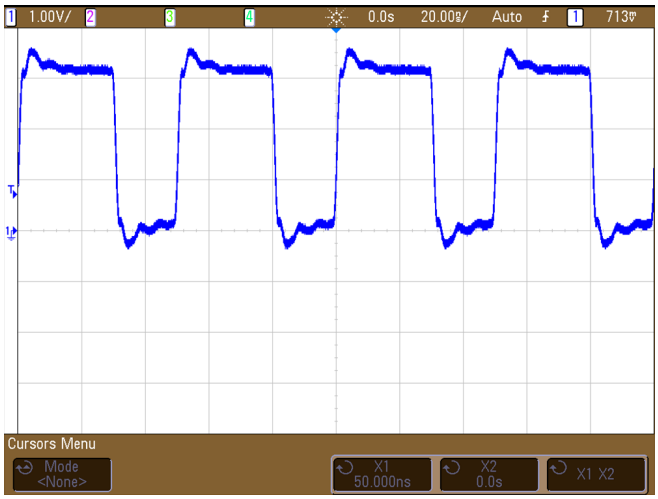

Figure 5. Clock Signal Probed at Buffer Output - No Termination

Figure 6. Clock Signal Probed at Modulator 3 - No Termination

Series resistor termination is not preferred in daisy-chain configuration. It results in modulator 3 detecting a clean clock waveform but the intermediate modulators and the MCU will observe clock signals with step rise and fall time. The Thevenin configuration is preferred. For Thevenin termination, the end of the clock traces (at modulator 3 and at MCU) are connected to GND and VDD through resistors as Figure 7 shows. The parallel equivalent of the 2 resistors should be equal to the trace impedance of 50 Ω. In this case, the resistors are 100 Ω each. Figure 8 and Figure 9 show the resulting clock signals with Thevenin termination.

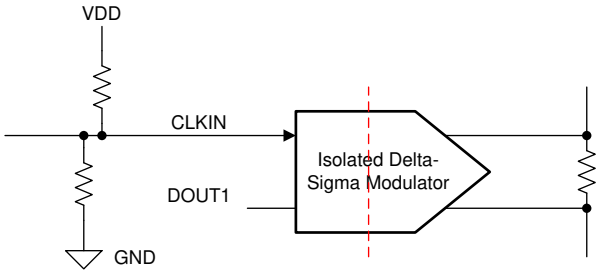

Figure 7. Thevenin Termination

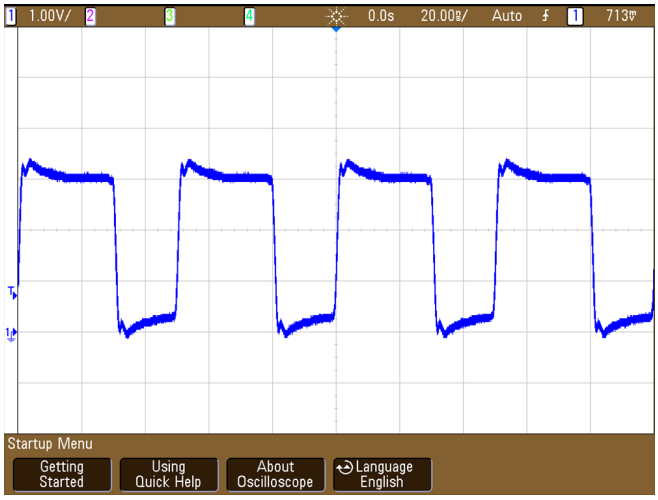

Figure 8. Clock Signal Probed at Buffer Output - Thevenin Termination

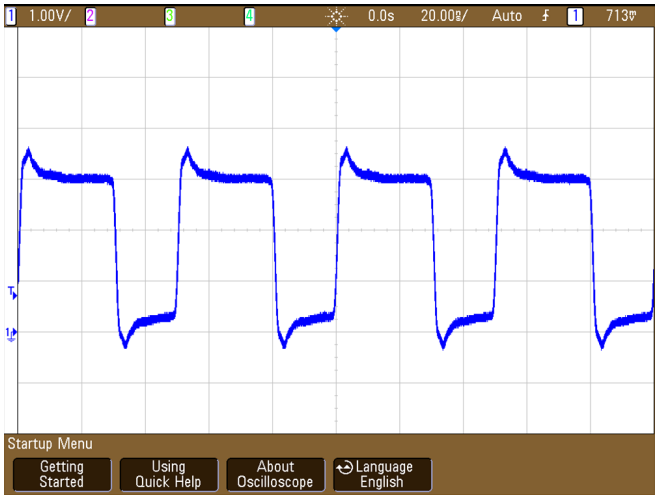

Figure 9. Clock Signal Probed at Modulator 3 - Thevenin Termination

The disadvantage with Thevenin termination is the continuous loss of power through the resistors due to the bias current. Figure 10 illustrates how the loss can be minimized by putting a small capacitor in series with the resistors. Figure 11 and Figure 12 show the resulting waveforms for the test board when a capacitor of 220 pF was put in series with a 100-Ω resistor.

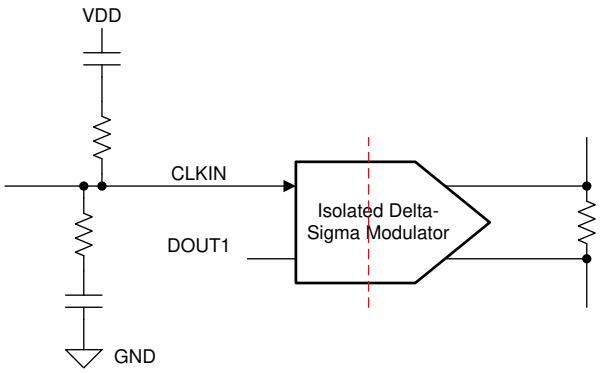

Figure 10. Thevenin AC Termination

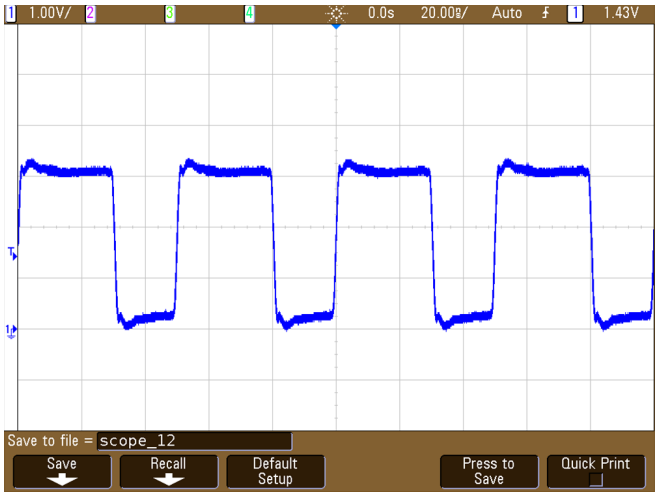

Figure 11. Clock Signal Probed at Buffer Output - Thevenin AC Termination

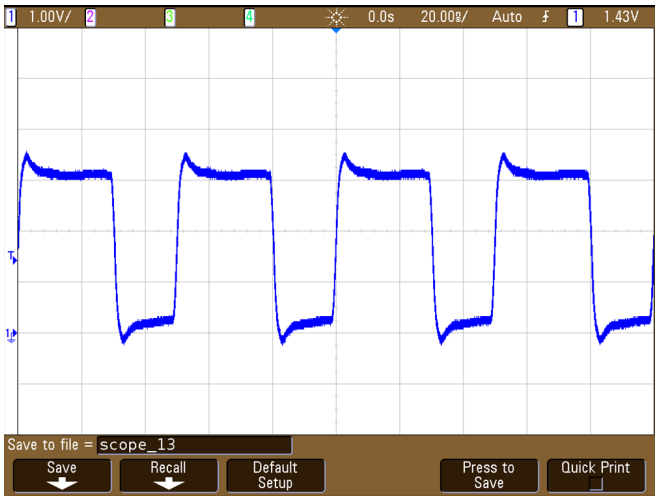

Figure 12. Clock Signal Probed at Modulator 3 - Thevenin AC Termination

2.2 Star Clock Routing Configuration Example

Figure 13 shows an alternate test PCB with a TMS320F28379D MCU which generates the 20-MHz clock signal from its PWM peripheral driven into a clock buffer SN74LVC2G17D device. The output of the buffer is split into four tracks, one goes back to the MCU SDFM peripheral and the others are connected to modulators in a star connection.

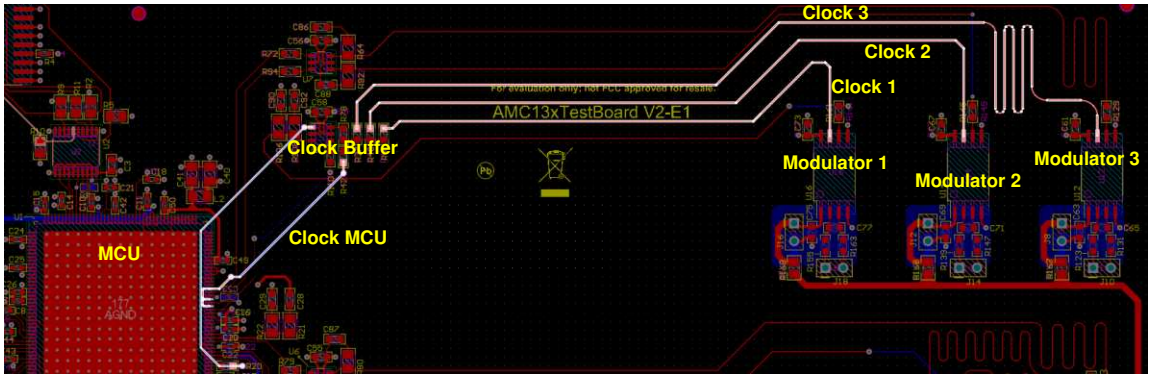

Figure 13. Star-Routing Example

The traces on the test PCB are impedance-controlled to 50 Ω. If termination is not done on the PCB, the clock signal shows significant ringing (Figure 14 to Figure 17).

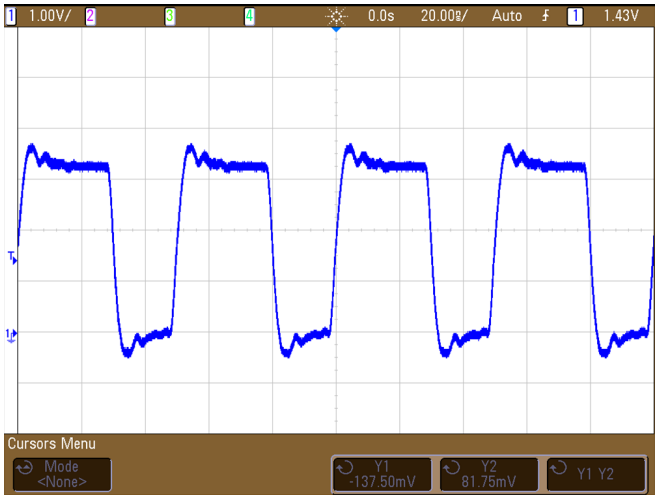

Figure 14. Clock Signal Probed At Buffer Output - No Termination

Figure 15. Clock Signal Probed At Modulator 3 - No Termination

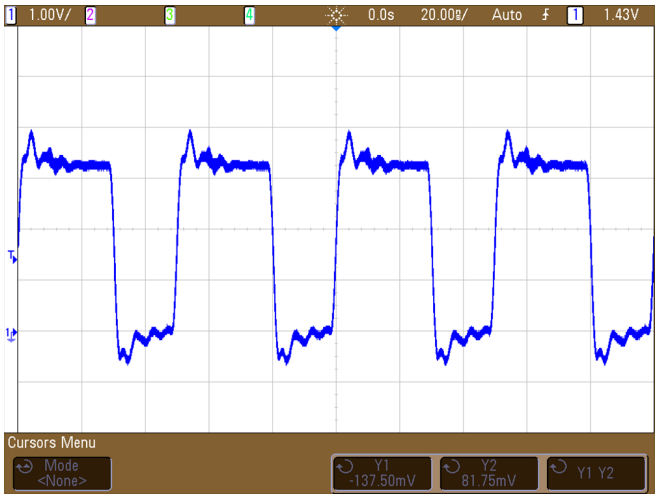

Figure 16. Clock Signal Probed At Modulator 2 - No Termination

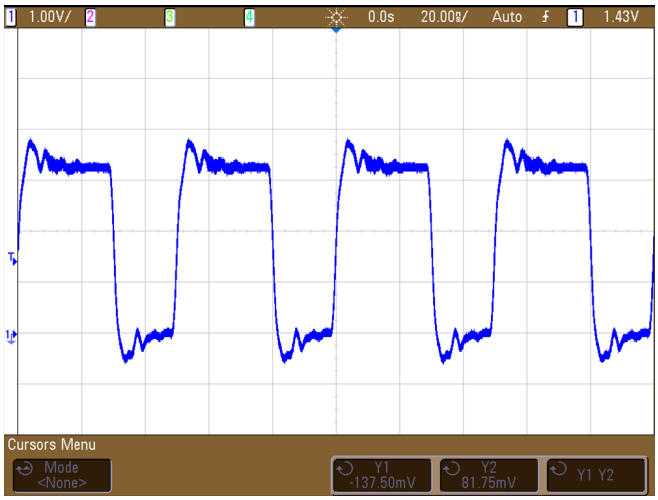

Figure 17. Clock Signal Probed At Modulator 1 - No Termination

Thevenin resistor termination is not preferred in star configuration because it must be done on all the clock ends and results in significant power dissipation and buffer drive requirements. Series-termination is preferred. For series termination, a resistor is placed in series with the driver such that the sum of the driver output impedance plus the series resistor is equal to the trace characteristic impedance. Any reflection that happens on the receiver end travels back to the driver and is attenuated at the series resistor. Figure 18 illustrates the series termination configuration at the buffer driver end.

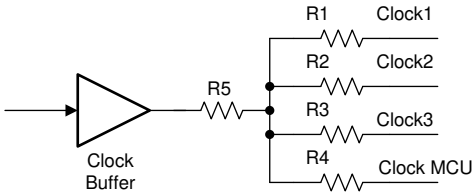

Figure 18. Series Termination Configuration

Through experimentation, it is determined that the buffer output impedance is 10 Ω and the external series resistor required is 40 Ω to match the trace impedance of 50 Ω. If a single 40-Ω resistor is used for R5 and R1, R2, R3, and R4 are 0 Ω, the clock signal integrity is not improved significantly with minor ringing as Figure 19 to Figure 22 illustrate.

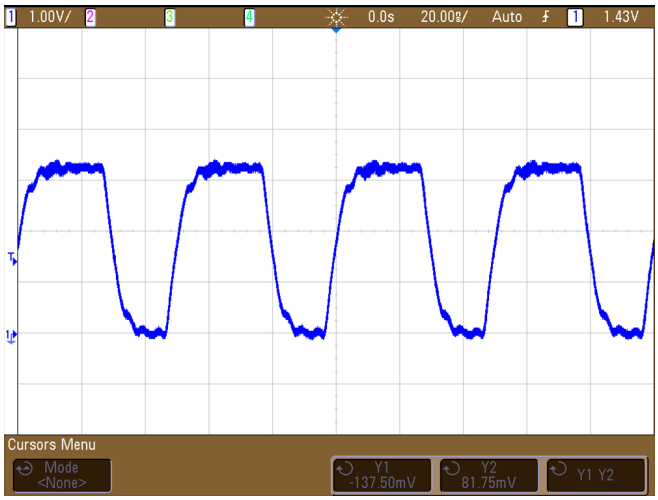

Figure 19. Clock Signal Probed At Buffer Output - Single Series Termination

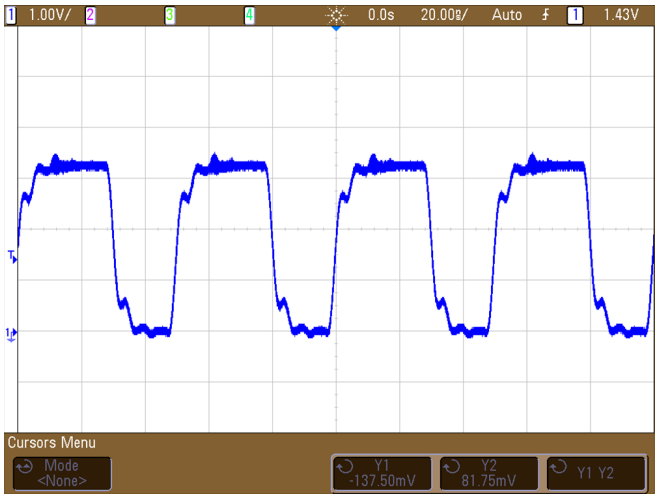

Figure 20. Clock Signal Probed At Modulator 3 - Single Series Termination

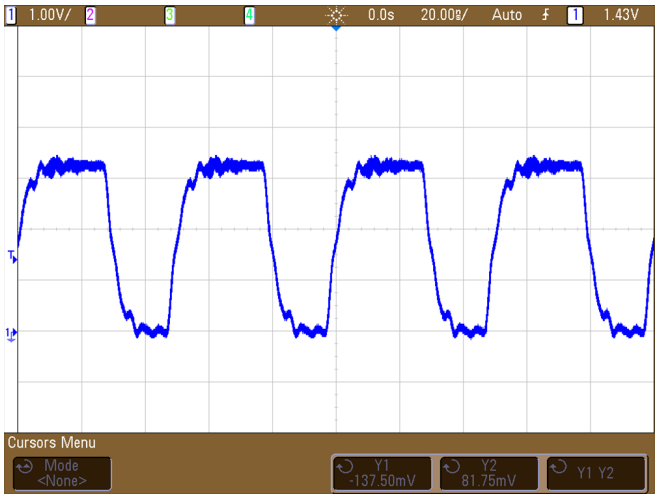

Figure 21. Clock Signal Probed At Modulator 2 - Single Series Termination

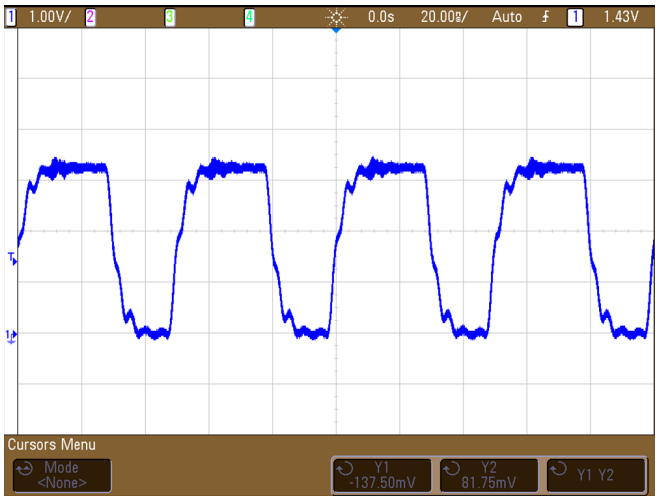

Figure 22. Clock Signal Probed At Modulator 1 - Single Series Termination

Individual 40-Ω series resistors must be used for R1, R2, R3, and R4 and R5 made 0 Ω to get clean clock signals. Figure 23 to Figure 26 show the results from the test PCB.

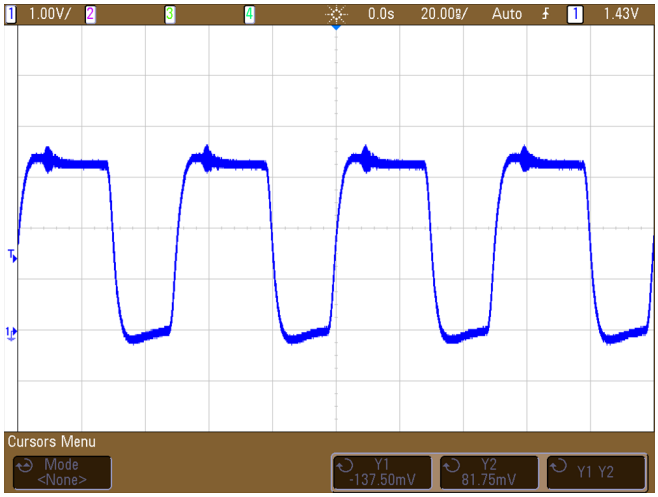

Figure 23. Clock Signal Probed At Buffer Output - Individual Series Termination

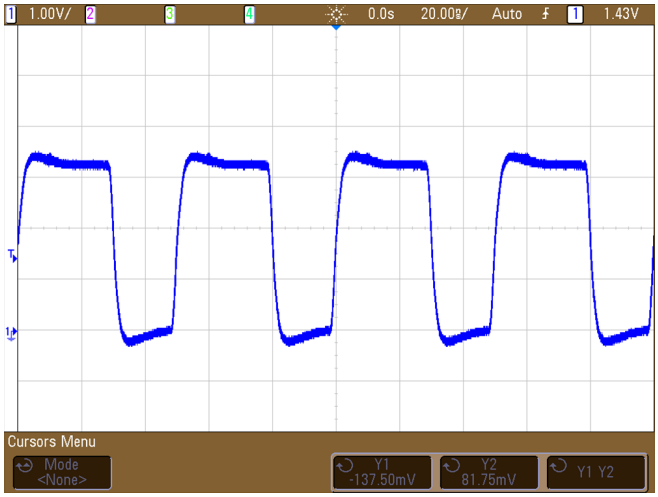

Figure 24. Clock Signal Probed At Modulator 3 - Individual Series Termination

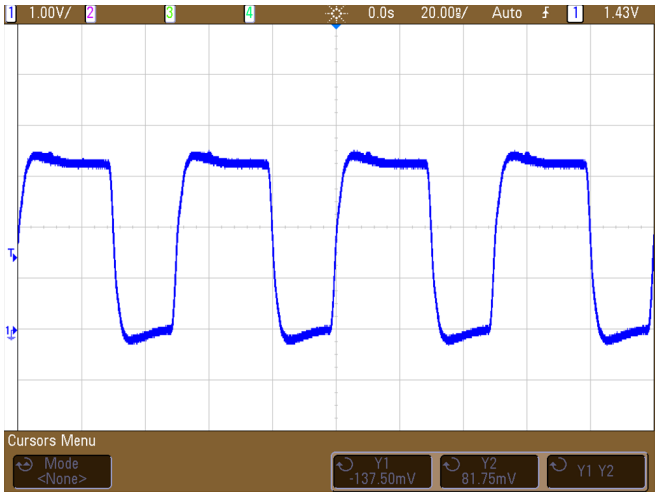

Figure 25. Clock Signal Probed At Modulator 2 - Individual Series Termination

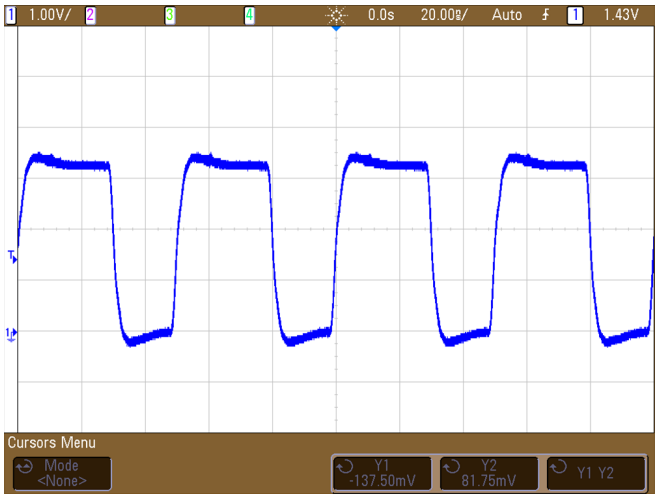

Figure 26. Clock Signal Probed At Modulator 1 - Individual Series Termination

Compared to a clock signal, modulator data signal termination is much simpler as it is a point-to-point signal and requires only one series termination resistor on the output of the AMC1306M25 device.

2.3 Effect of Connectors and Cables on Clock Signal Integrity

Typically the power and control boards are two separate PCBs and they are connected together with flat ribbon cables. To simulate this, the test PCB in Figure 27 was modified with an intermediate ribbon cable interface (Figure 28). Two cable lengths of 6 and 18 inches were chosen. Flat ribbon cables have a characteristic impedance of 100 Ω.

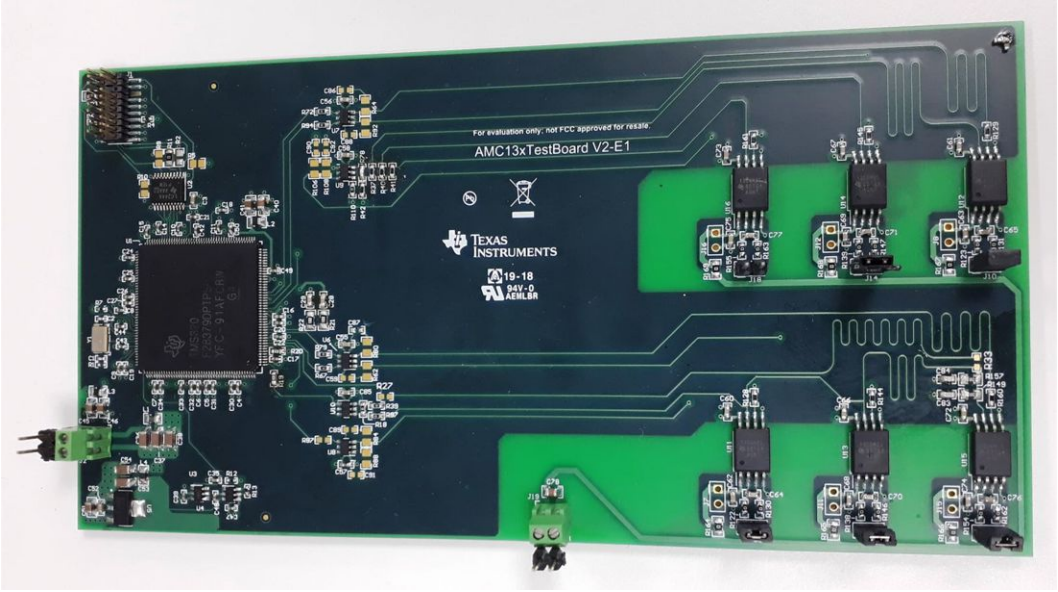

Figure 27. Test Board With no Connector and Cables

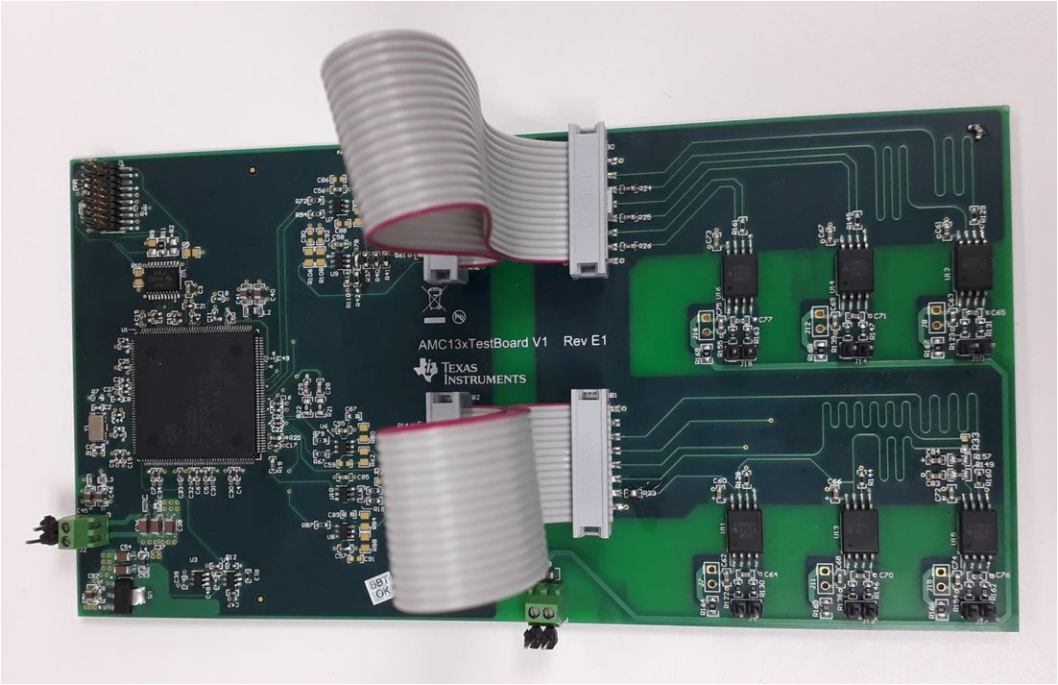

Figure 28. Test Board Modified With Intermediate Connector and Flat Ribbon Cables

2.3.1 Daisy-Chain Configuration Example With Flat Cable

The waveforms in Figure 29 to Figure 32 were routed through a 6-in flat cable along with a single ground (on the left side of Figure 33).

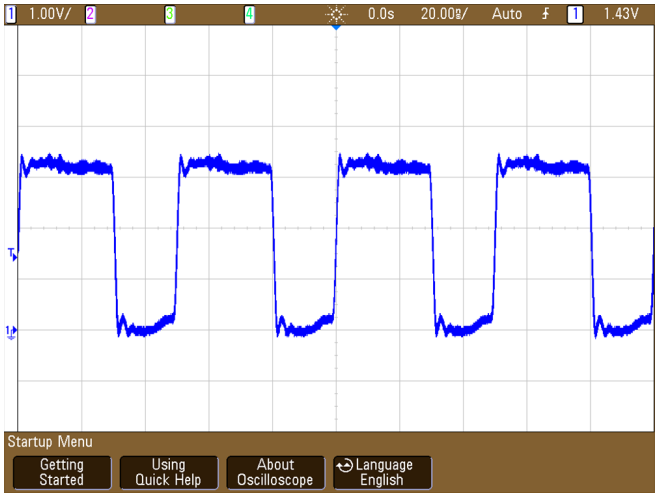

Figure 29. Clock Signal Probed At Buffer Output - No Termination

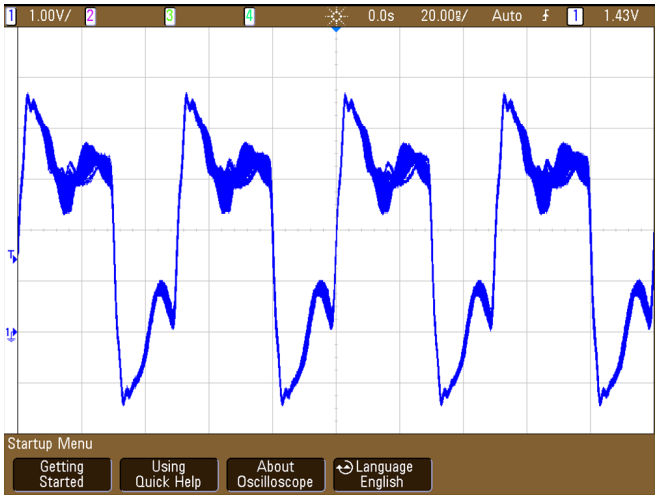

Figure 30. Clock Signal Probed At Modulator 3 - No Termination

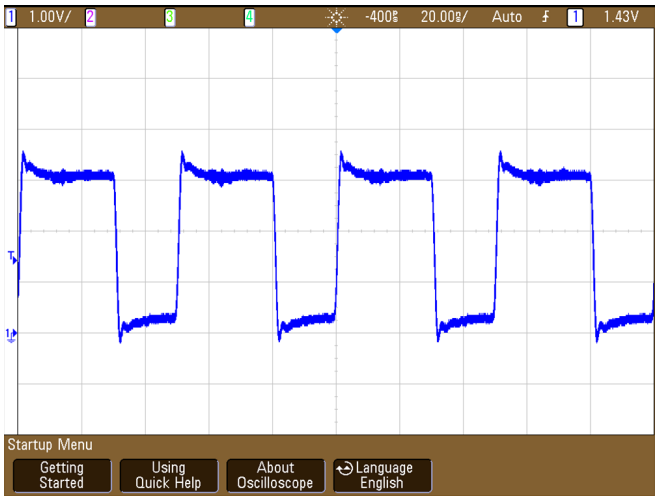

Figure 31. Clock Signal Probed At Buffer Output - Thevenin AC Termination

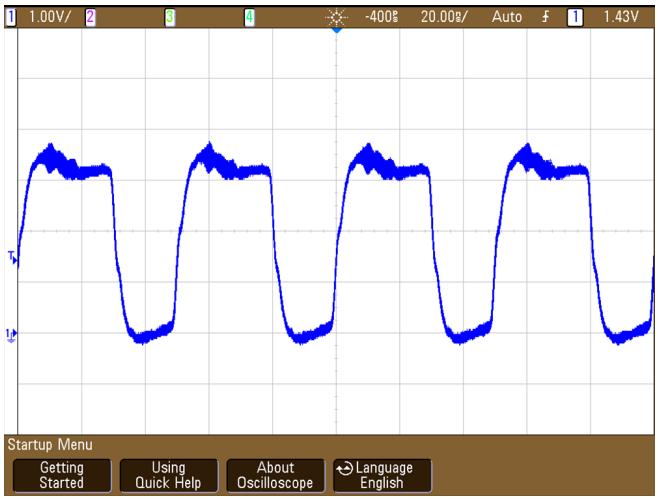

Figure 32. Clock Signal Probed At Modulator 3 - Thevenin AC Termination

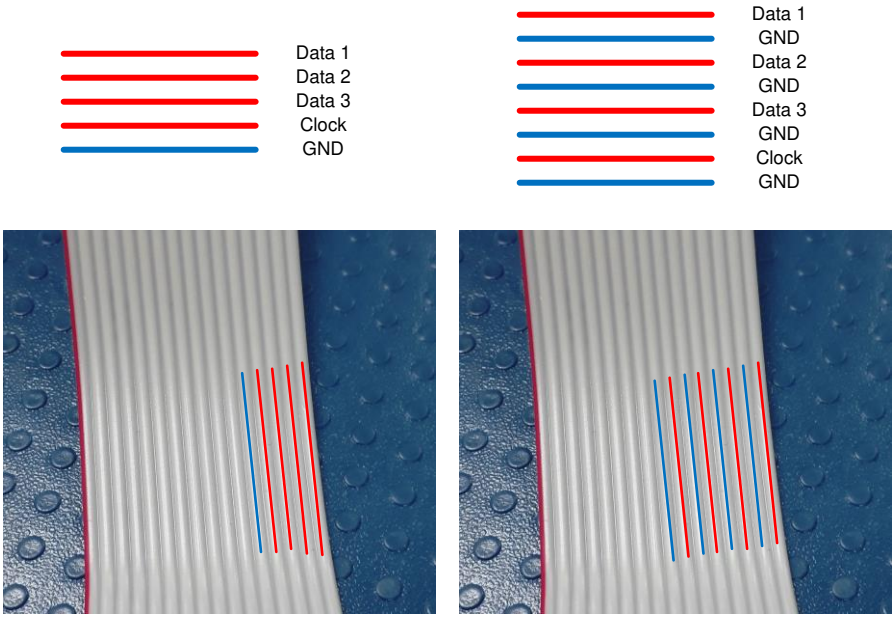

Figure 33. Ground Signal Routing in Flat Cables

Adding adjacent ground pins to each signal (on the right side of Figure 33) results in cleaner clock signals as Figure 34 and Figure 35 illustrate.

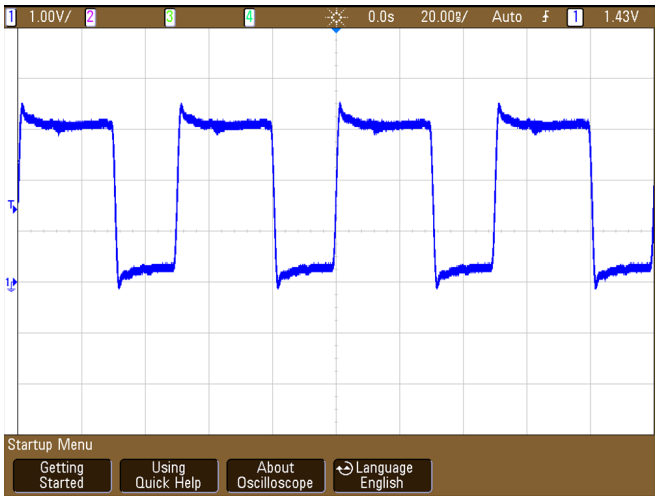

Figure 34. Clock Signal Probed At Buffer Output - Thevenin AC Termination

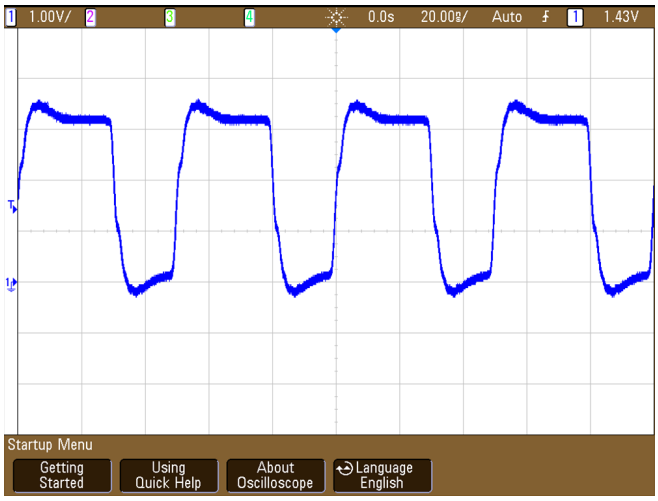

Figure 35. Clock Signal Probed At Modulator 3 - Thevenin AC Termination

Increasing the cable length by 3 times, that is from 6 inches to 18 inches, results in further signal degradation which might make the clock signal no longer usable as shown in Figure 36 and Figure 37. Clock repeaters may have to be used in such a case.

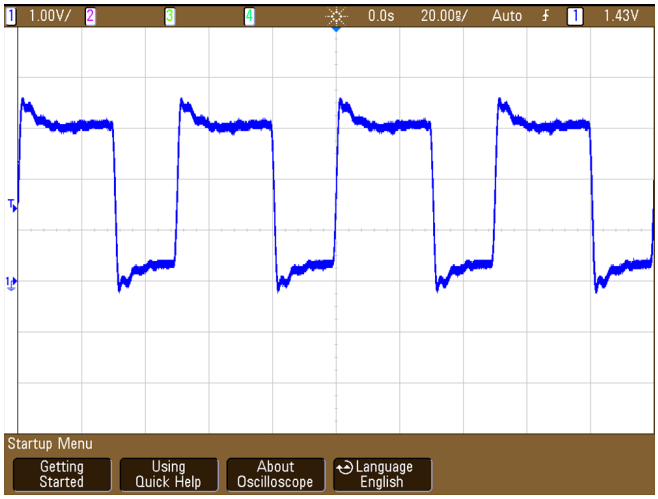

Figure 36. Clock Signal Probed At Buffer Output - Thevenin AC Termination

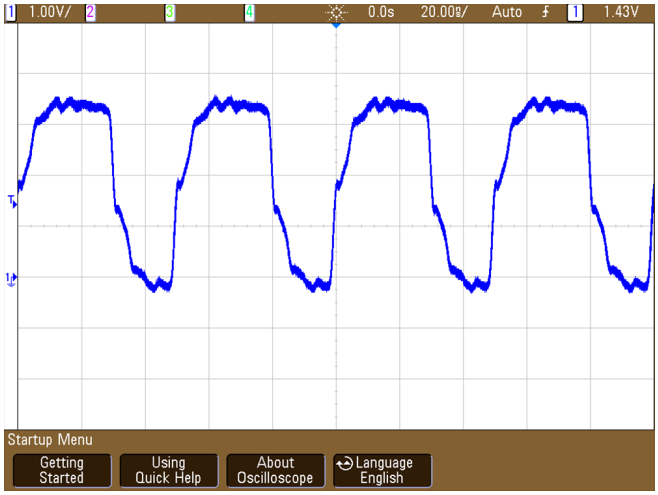

Figure 37. Clock Signal Probed At Modulator 3 - Thevenin AC Termination

2.3.2 Star-Routing With Flat Cables

For the star-routing configuration, initially the 6-inch flat cable is used. Figure 38 and Figure 41 show the signals with adjacent ground wires in the flat cable and individual series termination resistors for each line.

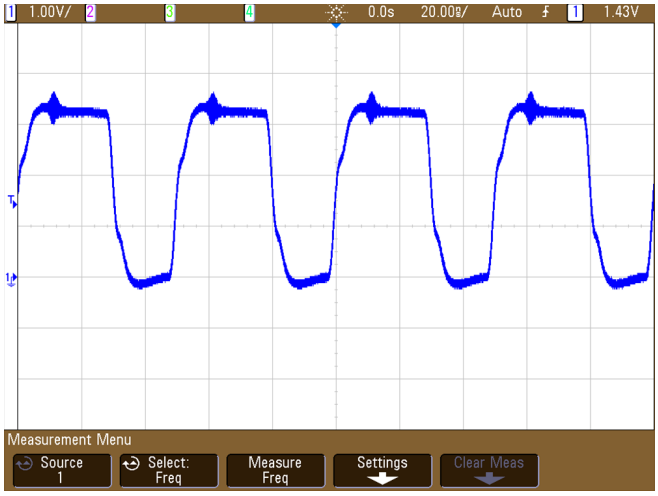

Figure 38. Clock Signal Probed At Buffer Output - Individual Series Termination

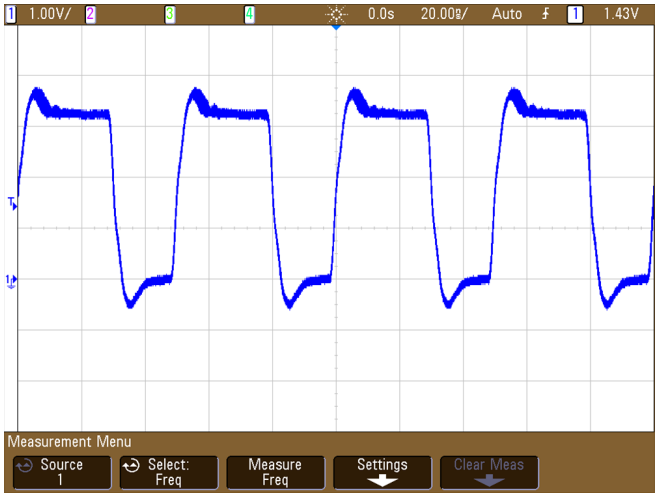

Figure 39. Clock Signal Probed At Modulator 3 - Individual Series Termination

Figure 40. Clock Signal Probed At Modulator 2 - Individual Series Termination

Figure 41. Clock Signal Probed At Modulator 1 - Individual Series Termination

Increasing the cable length by 3 times, that is from 6 inches to 18 inches, results in an increase in overshoots and undershoots as Figure 42 to Figure 45 show.

Figure 42. Clock Signal Probed At Buffer Output - Individual Series Termination

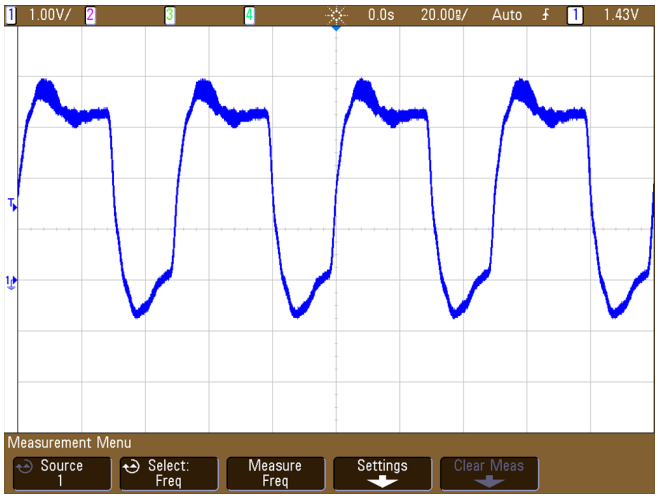

Figure 43. Clock Signal Probed At Modulator 3 - Individual Series Termination

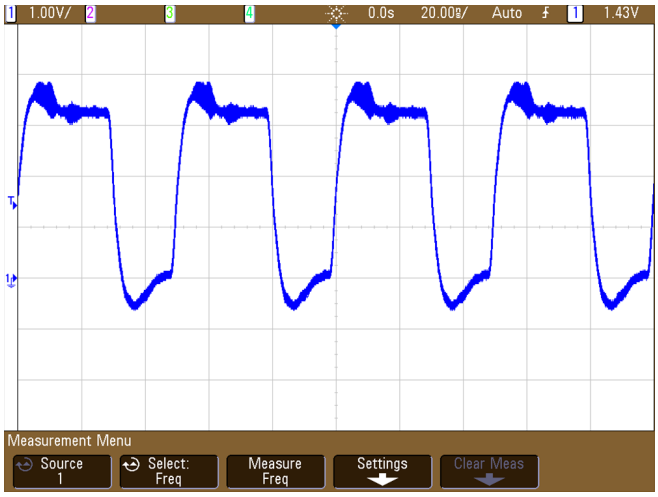

Figure 44. Clock Signal Probed At Modulator 2 - Individual Series Termination

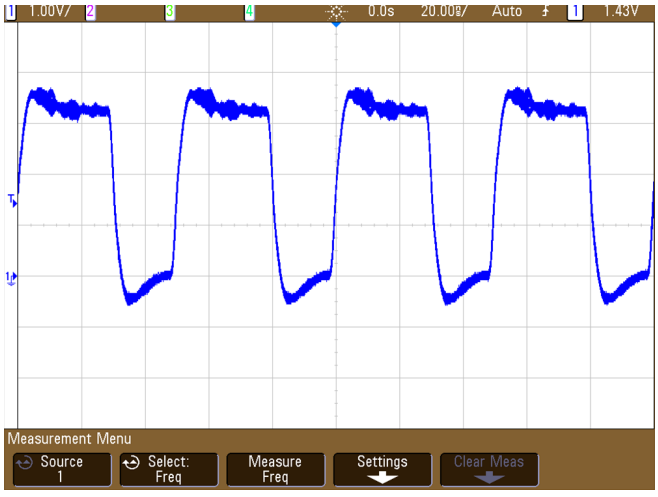

Figure 45. Clock Signal Probed At Modulator 1 - Individual Series Termination

3 Setup and Hold Timing

3.1 Case 1 - MCU, MPU, FPGA Generates the Clock Signal to the Modulator

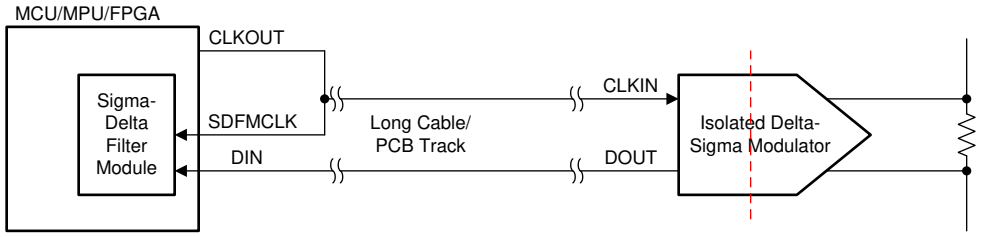

Figure 46. MCU To Modulator Interface - Clock Generated By MCU

The clock signal generated by the MCU is routed to the ΔΣ modulator with a propagation delay of t_{prop1}. The propagation delay depends on the signal trace length and PCB stackup construction. The modulator sends out a data bit synchronized to the clock edge after a modulator device specific delay time of t_D. The output data bit propagates back to the MCU with a propagation delay of t_{prop2}. The CLKOUT is looped back directly at the MCU into the SDFMCLK and hence it has a negligible propagation delay. The MCU has its own setup and hold time specifications. Setup time is the time before the clock edge for which the data should remain stable and the hold time is the time after the clock edge for which the data should remain stable. Violating setup and hold time requirements results in incorrect data being captured by the MCU.

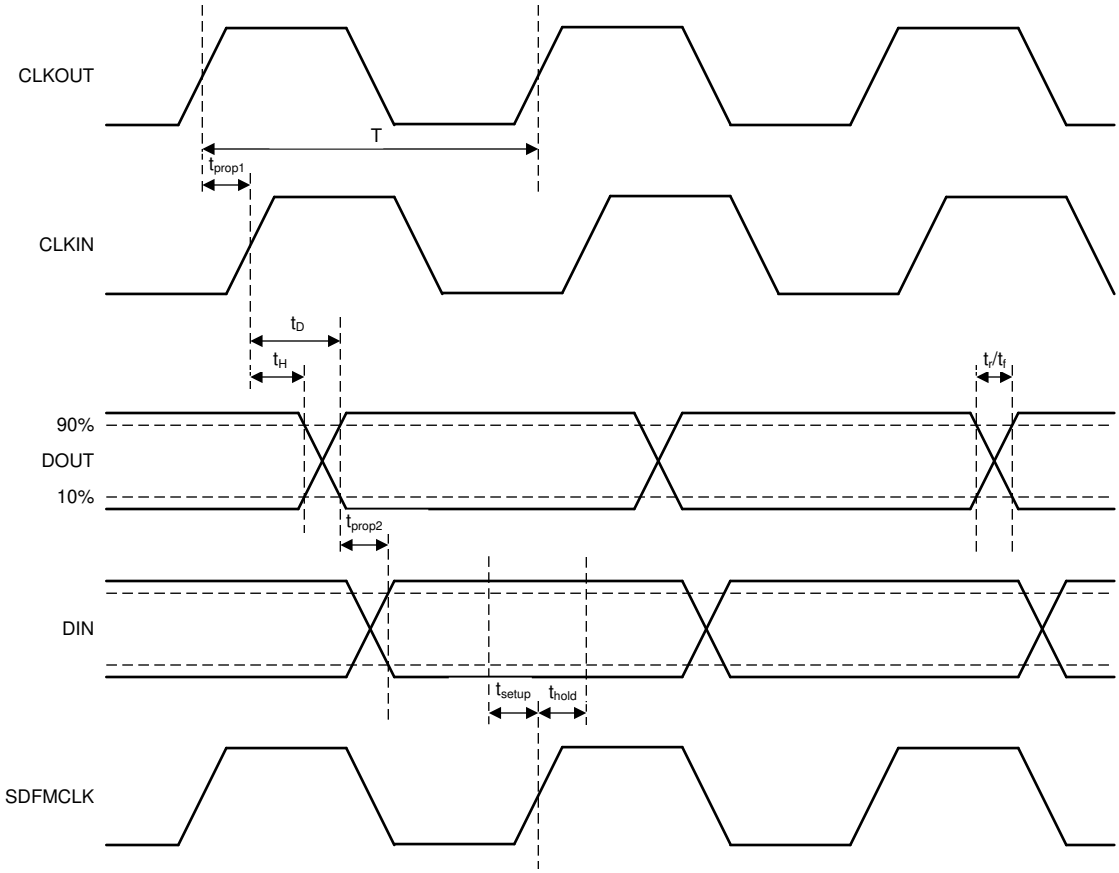

Figure 47. Hold and Data Valid Time

Use Equation 1 to calculate the total time from the CLKOUT rising edge to the modulator data DIN reaching the MCU.

$$T_{DIN} = t_{prop1} + t_D + t_{prop2} \quad (1)$$

DIN is captured by the MCU at the next rising clock edge which occurs after the period T. To avoid setup and hold time violations, keep T_{DIN} within the constraint boundaries in Equation 2.

$$T_{DIN} \le T - t_{setup}$$
$$T_{DIN} \ge t_{hold} \quad (2)$$

Consider an example of the C2000 microcontroller TMS320F28379D and modulator AMC1306M25 pair functioning at 20-MHz clock frequency. The sigma-delta filter module inside the controller is operating in mode 0 as Table 1 shows. Table 2 and Table 3 show the switching characteristics.

Table 1. SDFM Modes

MODULATOR MODE [MOD]	DESCRIPTION
0	The modulator clock is running with the modulator data rate. The modulator data is strobed at every rising edge of the modulator clock.
1	The modulator clock is running with half of the modulator data rate. The modulator data is strobed at every edge of the modulator clock.
2	The modulator clock is off and the modulator data is Manchester-encoded.
3	The modulator clock is running with double the modulator data rate. The modulator data is strobed at every other positive modulator clock edge.

Table 2. AMC1306M25 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	4.5 V ≤ AVDD ≤ 5.5 V	5		21	MHz
		3.0 V ≤ AVDD ≤ 5.5 V	5		20	
t_{CLKIN}	CLKIN clock period	4.5 V ≤ AVDD ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ AVDD ≤ 5.5 V	50		200	
t_{HIGH}	CLKIN clock high time		20	25	120	ns
t_{LOW}	CLKIN clock low time		20	25	120	ns
t_H	DOUT hold time after rising edge of CLKIN	AMC1306Mx, C_{LOAD} = 15 pF	3.5			ns
t_D	Rising edge of CLKIN to DOUT valid delay	AMC1306Mx, C_{LOAD} = 15 pF			15	ns
t_r	DOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	
t_f	DOUT fall time	90% to 10%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		90% to 10%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	

Table 3. TMS320F28379D SDFM Switching Characteristics

		MIN	MAX	UNIT
Mode 0				
$t_{c(SDC)M0}$	Cycle time, SDx_Cy	40	256 × SYSCLK period	ns
$t_{w(SDCH)M0}$	Pulse duration, SDx_Cy high	10	$t_{c(SDC)M0}$ – 10	ns
$t_{su(SDDV-SDCH)M0}$	Setup time, SDx_Dy valid before SDx_Cy goes high	5		ns
$t_{h(SDCH-SDD)M0}$	Hold time, SDx_Dy wait after SDx_Cy goes high	5		ns

$$T_{DIN} \le T - t_{setup} = 50\ ns - 5\ ns = 45\ ns$$
$$T_{DIN} \ge t_{hold} = 5\ ns$$
$$T_{DIN} = t_{prop1} + t_D + t_{prop2} = t_{prop1} + 15\ ns + t_{prop2} \ge 5\ ns \quad (3)$$

The minimum condition is easily followed due to a minimum t_H of 3.5 ns, rise and fall time of 0.8 ns typical and the t_D of 15 ns.

The maximum round trip propagation delay possible is calculated from Equation 4:

$$T_{DIN} \le T - t_{setup} = 50\ ns - 5\ ns = 45\ ns$$
$$t_{prop1} + t_D + t_{prop2} \le 45\ ns$$
$$t_{prop1} + t_{prop2} \le 30\ ns \quad (4)$$

The round trip propagation delay is a property of the PCB construction (Dielectric constant Er of the FR4 prepreg material used):

$$t_{prop} \sim 85\sqrt{(0.64Er + 0.36)} = 154\ ps / in \quad (5)$$

The maximum roundtrip trace length allowed is approximately 200 inches. For all practical PCB implementations, trace length is not a constraint towards setup and hold issues.

Some controller implementations will capture the data at the falling edge of the clock signal while the AMC1306 device always transmits data at the rising edge. In such cases the maximum allowed round trip trace length is 32 inches calculated using Equation 6:

$$T_{DIN} \le \frac{T}{2} - t_{setup} = 25\ ns - 5\ ns = 20\ ns$$
$$t_{prop1} + t_{prop2} \le 5\ ns \quad (6)$$

3.2 Case 2 - Clock is Generated by an External Chip and not by MCU, MPU, and FPGA

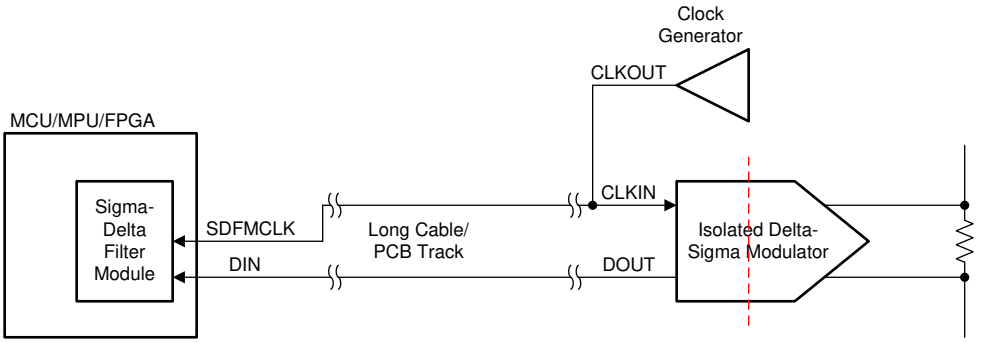

Figure 48. MCU to Modulator Interface - Clock Generated by External IC

Some implementations can have an external clock source instead of being generated by the MCU. In such cases the clock source is typically placed near the ΔΣ modulators to eliminate any propagation delay in clock signal t_{prop1}.

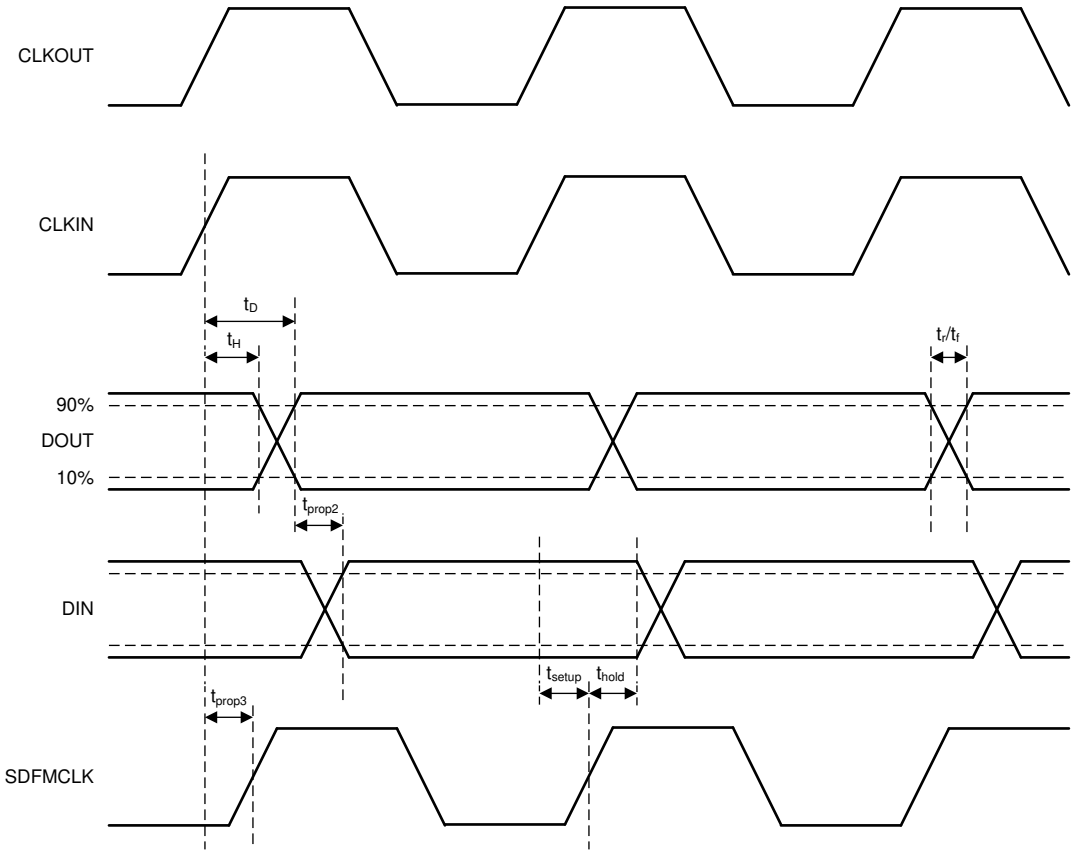

Figure 49. Hold and Data Valid Times

$$t_D + t_{prop2} - t_{prop3} \leq T - t_{setup} \quad (7)$$

t_{prop3} is the delay of the clock signal from the clock generator to MCU. If the clock signal and the data signal are routed back to the MCU close to each other with matched distance, then $t_{prop2} = t_{prop3}$.

$$t_D \leq 50\ ns - 5\ ns = 45\ ns$$
$$t_D \geq t_{hold} = 5\ ns$$
$$T_{DIN} = t_D + t_{prop2} = 15\ ns + t_{prop2} \geq 5\ ns \quad (8)$$

The minimum and maximum conditions are easily followed due to t_D = 15 ns.

4 Summary

Based on modulator placement on the PCB, both star- and daisy-chain clock routing can be used. For star-routing series termination is used and for daisy-chain Thevenin ac termination is used. Using short flat cables between the control and power PCB does not severely impact the signal integrity. If it is not possible to avoid cables, the cable length must be kept to as short as possible.

Alternate solutions are to use modulators with Manchester-encoded data output like the AMC1306Ex devices or modulators with internal clock generation like the AMC1303x devices. These devices make clock and data routing, termination, and design for setup and hold times much simpler. It is also possible to use one to many output clock buffer devices which allows for the use of simple series termination for each output.

5 References

1. Texas Instruments, *TMS320F2837xD Dual-Core Delfino™ Microcontrollers Data Sheet*
2. Texas Instruments, *TMS320F2837xD Dual-Core Delfino Microcontrollers Technical Reference Manual*
3. Texas Instruments, *AMC1306x Small, High-Precision, Reinforced Isolated Delta-Sigma Modulators With High CMTI Data Sheet*

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265