

Simplify Isolation Designs Using an Enhanced-SPI ADC Interface

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In applications such as power supplies, inverters, protection relays, etc. the system controller is isolated from the high-voltage circuit. In a high voltage system, the analog-to-digital converter (ADC) can be placed closer to the sensor for improved performance. The ADC data output, typically SPI communication, is interfaced to the system controller using a digital isolator. Isolators are typically chosen to ensure compliance with safety and regulatory standards. However, an isolator which meets the safety and regulatory standards may not always meet the timing requirements of a high-speed SPI interface at low cost; this is common in protection relays and power quality monitoring systems.

An ADC is a slave entity on the SPI bus which sends data in response to \overline{CS} and SCLK from the system controller. When working with an isolator, as shown in Figure 2, the propagation delay causes the ADC to receive the serial clock later than when the processor sent it, as shown in Figure 3.

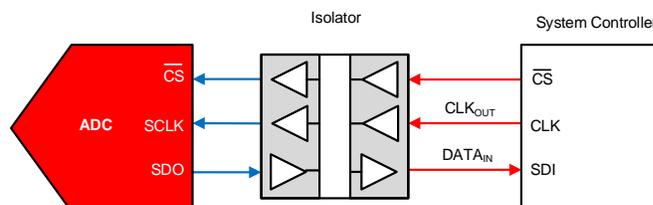


Figure 2. ADC SPI Interface with Isolator

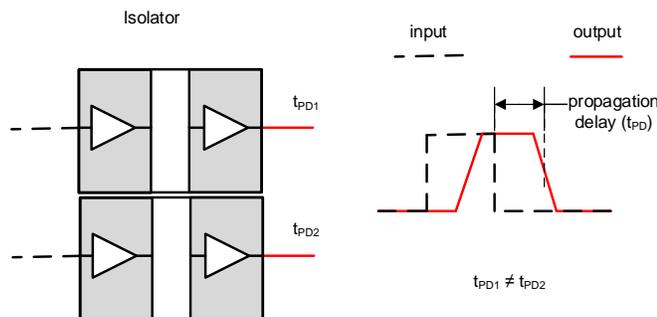


Figure 1. Effect of Isolation on Digital Lines

An isolator can have propagation delays of several nano-seconds, as shown in Figure 1, and are prone to have significant timing variation across channels. Thus the isolator can limit the maximum SPI clock speed for reliable timing, which in turn may limit the ADC sampling rate. It may not be possible to operate the ADC at full sampling rate if the SPI interface clock speed is limited. Hence the system design must factor in the propagation delay and channel-to-channel variation of the isolator to avoid limiting the ADC throughput.

Effects of Propagation Delay

The propagation delay of an isolator is the time it takes for a logic change at the input to be reflected at the output. The propagation delay of isolators can be of the order of 10s of nano-seconds.

The ADC sends data bits with respect to the serial clock at the ADC clock input. This data output of the ADC is connected through an isolator channel to the processor. In Figure 3 it can be seen that the data output also gets shifted by an amount equal to the propagation delay of the isolator. From the processor's perspective, there is 2x the t_{PD} delay between CLK_{OUT} and $DATA_{IN}$ because of the propagation delay on serial clock and data path.

$$t_{DELAY} = 2 \times t_{PD} \tag{1}$$

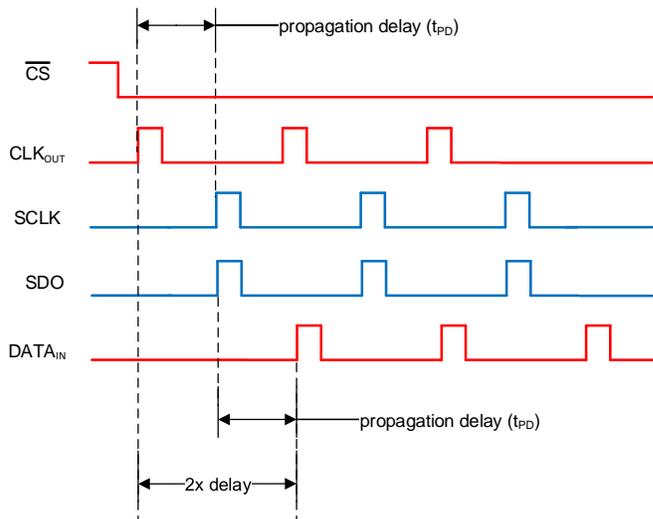


Figure 3. Effect of Propagation Delay on SPI Timings

The delay in receiving data $DATA_{IN}$ with respect to CLK_{OUT} can lead to data bits being lost or latched incorrectly. The minimum SCLK period cannot exceed the total propagation delay between $DATA_{IN}$ and CLK_{OUT} i.e. t_{DELAY} . Hence the isolator's propagation delay imposes a maximum clock speed limit on the SPI data bus.

$$t_{SPL_CLK} \geq t_{DELAY} \quad (2)$$

$$f_{SPL_CLK} \leq (t_{SPL_CLK})^{-1} \quad (3)$$

There can be other sources of propagation delay such as routing delay caused by the printed circuit board. All these propagation delays put together impose an upper limit on the maximum clock speed in the system.

Using Long Data Read Time of Enhanced-SPI Devices

Table 1 lists the device families which support the Enhanced-SPI interface. Figure 4 shows the ADS8920B's 3-wire SPI interface with an isolator. The ADC's CONV (conversion start) and \overline{CS} pins can be tied together and driven by the \overline{CS} line of the SPI bus.

The Enhanced-SPI interface allows the conversion data to be read out from the ADC during an on-going conversion, as shown in Figure 5.

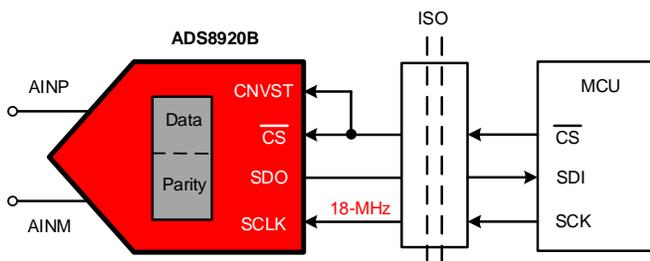


Figure 4. ADS8920B Isolated 3-wire SPI

Table 1 lists the ADC device families which support the Enhanced-SPI interface. The Wide Read Cycle using Enhanced-SPI interface allows for a 18-MHz SPI clock when the ADC sampling rate is 1-MSPS. This reduction in clock speed is achieved by pulling \overline{CS} low after start of conversion and reading data, as shown in Figure 5.

The reduction in SCLK speed enables the use of high-speed ADCs with an isolated digital interface having significant propagation delays. As there is no register configuration required to achieve low SCLK speeds, the SDO line of ADC can be left unconnected. Only SCLK, CS, and SDO pins of the ADC need to be interfaced using an isolator. As the SPI clock speeds are very low, there is no need to route an additional SCLK back from the isolator to compensate for delays.

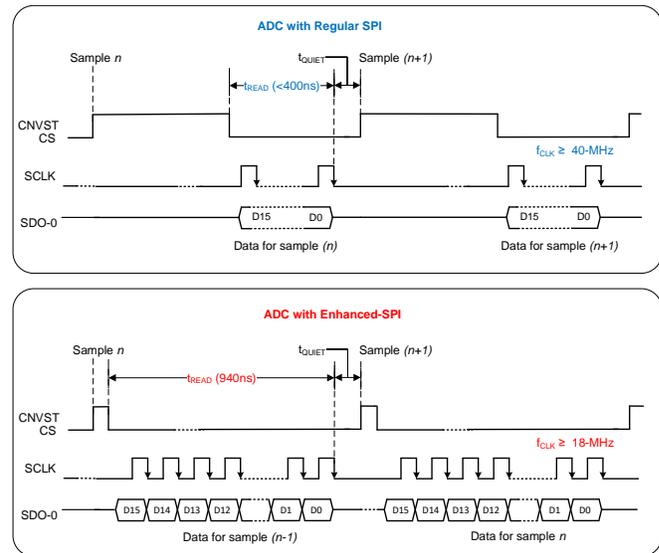


Figure 5. Enhanced-SPI vs. Regular SPI Comparison

Hence the Enhanced-SPI interface with Wide Read Cycle enables 3-wire SPI communication over generic isolators that may not have the low propagation delays or channel-to-channel delay matching that are often required for ADCs that require faster SCLK rates.

Resources

- [20-Bit, 1-MSPS Isolated Data Acquisition Reference Design Optimizing Jitter for Maximum SNR and Sample Rate](#)
- [20-bit, 1-MSPS Isolator Optimized Data Acquisition Reference Design Maximizing SNR and Sample Rate](#)
- [TI Precision Labs – Comprehensive ADC Trainings](#)

Table 1. High Speed Devices with Wide Read Cycle Feature of Enhanced-SPI

Device	Description	Regular SPI SCLK Speed	Enhanced-SPI SCLK Speed
ADS8920B	16-bit, 1-MSPS	52-MHz	18-MHz
ADS8910B	18-bit, 1-MSPS	58-MHz	20-MHz
ADS8900B	20-bit, 1-MSPS	70-MHz	22-MHz
ADS9120	16-bit, 2.5-MSPS	200-MHz	45-MHz
ADS9110	18-bit, 2-MSPS	140-MHz	40-MHz

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