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Two-wire PT100 RTD measurement circuit with low-side reference

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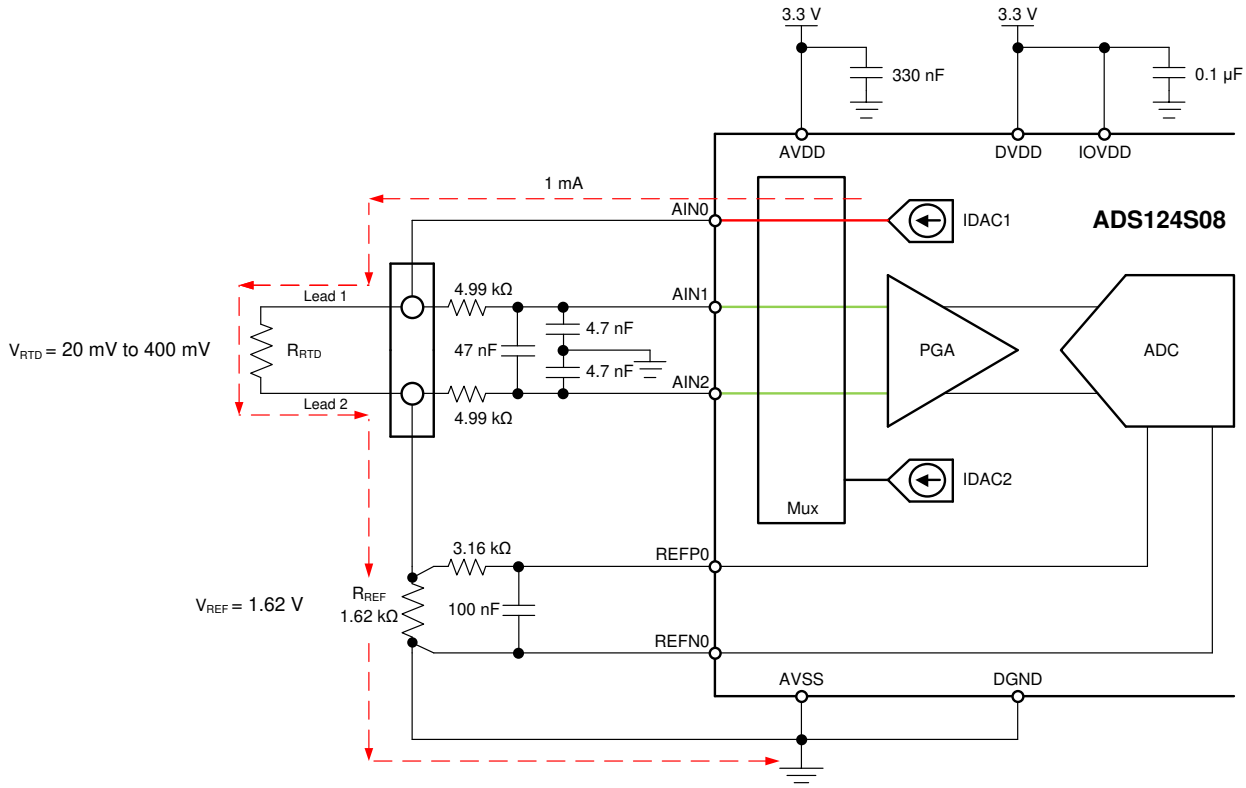
Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a two-wire RTD using the ADS124S08. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.
7. This design shows connections to three input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The two-wire RTD measurement is the least accurate of RTD measurements because the lead resistance error cannot be removed. For measurements with more accurate RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01˚C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations.

   $V_{AIN1} = I_{IDAC1} \bullet (R_{RTD} + R_{REF}) = 1mA \bullet (400Ω + 1620Ω) = 2.02V$

   $V_{AIN2} = I_{IDAC1} \bullet R_{REF} = 1mA \bullet 1620Ω = 1.62V$

   $V_{INMAX} = 1mA \bullet 400Ω = 400mV$
3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that

AVDD is 3.3V and AVSS is 0V. As the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet shows, the absolute input voltage must satisfy the following:

$AVSS + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

$0V + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

$0.75 < V_{AIN1}, V_{AIN2} < 2.55V$

Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02 V and 1.62 V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

$AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

$0V < V_{AIN0} < 2.7V$

With the previous result, the output compliance of the IDAC is satisfied.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 / [2 \bullet \pi \bullet C_{IN\_DIFF} (R_{RTD} + 2 \bullet R_{IN})]$

   $f_{IN\_CM} = 1 / [2 \bullet \pi \bullet C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330 Hz and the common-mode filter bandwidth to 5kHz.

   The bandwidth for the reference input filtering is approximated in the following equation.

   $f_{REF} = 1 / [2 \bullet \pi \bullet C_{REF} \bullet (R_{REF} + R_{IN\_REF})]$

   For the reference input filtering, R_{IN_REF} = 3.16kΩ and C_{REF} = 100nF. This sets the reference filter bandwidth to 330 Hz. Because REFN0 is set to ground, the common-mode filtering is removed. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} / V_{REF}) = 2^{23} \bullet \text{Gain} \bullet (I_{IDAC1} \bullet R_{RTD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} / R_{REF}) \quad (1)$$

$$R_{RTD} = R_{REF} \bullet [\text{Output Code} / (\text{Gain} \bullet 2^{23})] \quad (2)$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Two-Wire PT100 RTD Measurement Circuit with Low-Side Reference Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	12h	Positive reference buffer enabled, negative reference buffer disabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    // RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    05    // Write to 6 registers
    12    // Select AINP = AIN1 and AINN = AIN2
    0A    // PGA enabled, Gain = 4
    14    // Continuous conversion mode, low-latency filter, 20-SPS data rate
    12    // Positive reference buffer enabled, negative reference buffer disabled
          // REFP0 and REFN0 reference selected, internal reference always on
    07    // IDAC magnitude set to 1 mA
    F0;    // IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low;     // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    05    // Read from 6 registers
    00 00 00 00 00 00;    // Send 6 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    }
Set CS low;
    Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements Application Report*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2018) to A Revision	Page
• Changed schematic to remove filtering from REFN0.	1
• Changed bandwidth calculation for reference input filter.	3
• Changed Register Settings Table to disable negative reference buffer.	4
• Changed Pseudo Code Example to disable negative reference buffer.	5

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