Application Report

Reducing Phase Delay by Averaging on ADS8686S with Burst Sequencer Mode

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ABSTRACT

This application note describes a simple solution by averaging the samples with Sequencer or Burst Sequencer mode on the ADS8686S. This method can significantly reduce the phase delay caused by the channel switching. Also, this technique is integrated in the ADS8686SEVM Graphical User Interface (GUI) software with a Fast Fourier Transform (FFT) algorithm which is used to calculate the phase angle and phase difference between the signals applied on the input channels of the ADC. The Phase Analysis page in the GUI is specifically developed for showing the phase difference between channels with and without averaging technique.

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Trademarks

1 Introduction

In a grid infrastructure application, measuring the phase difference between different signals is critical to ensure the safety of the power grid. The simultaneous sampling, multiple-channels inputs analog-to-digital converter (ADC) is ideal for the kind of application. However, to reduce the channel count and the cost, a non-simultaneous sampling, multiple-channels inputs ADC with internal multiplexer can be used.

When multiple input channels are sampled in a sequential manner as in a multiplexed ADC, an additional phase delay is introduced between the channels because of channel switching. The measured phase value of the signal includes this additional phase delay which is not expected by the design engineer and will lead to an inaccurate phase difference measurement. The reference design of Phase-Compensated, 8-Ch, Multiplexed Data Acquisition System for Power Automation Reference Design introduces a method how to compensate the additional phase delay caused by the channel switching on the internal multiplexer.

ADS8686S is a 16-channel, 16-bit, 1Msps, Dual simultaneous sampling successive approximation register (SAR) based ADC, the integrated analog front-end (AFE) with 1MΩ input impedance eliminates the requirement of ADC driver. The 16-channel inputs can meet the requirement in most multi-phase power measurement systems and make it possible to design a compact system. However, the channel switching on each ADC A/B of ADS8686S will introduce an additional phase delay.

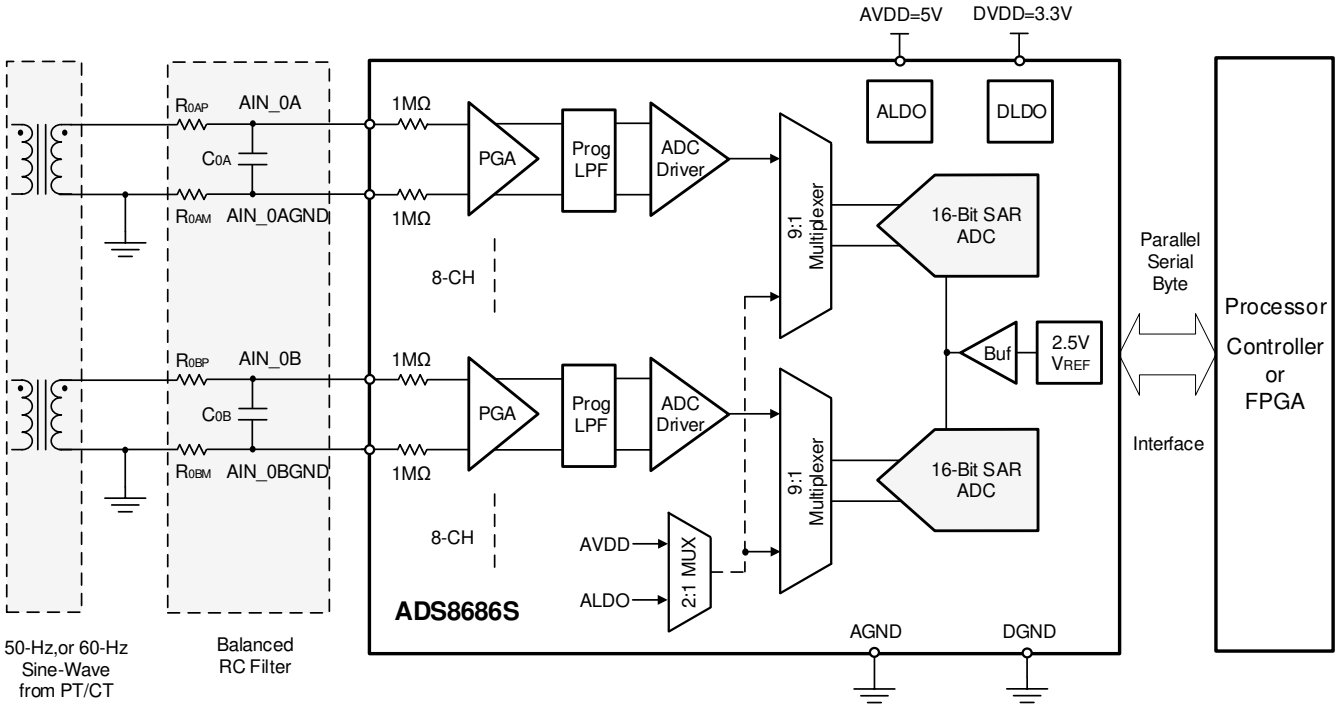

Figure 1-1. Typical Application Circuit Using ADS8686S in Grid Infrastructure System

2 Phase Delay and Non-Simultaneous Sampling

The terminology non-simultaneous sampling suggests that all input channels of a multi-channel system are not sampled at the same time instant by the ADC. This limitation is very typical in the case of a multiplexed input ADC, as the converter sequentially scans through the multiple input channels. An example of two alternating signals such as a voltage (V) and a current (I) is shown in Figure 2-1.

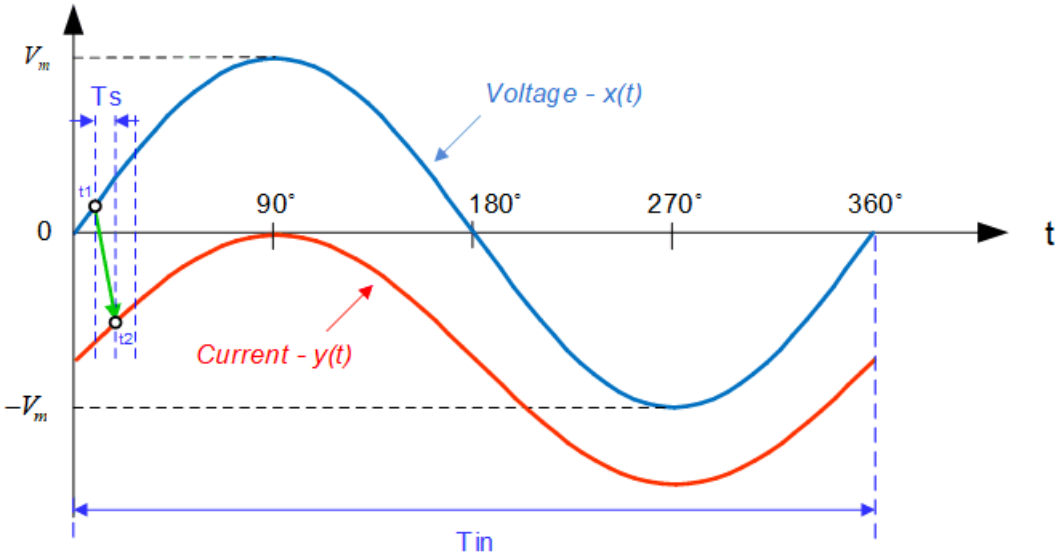

Figure 2-1. Phase Delay between Sinusoidal Waveforms

To only consider the phase delay between two channels due to the ADC's channel switching, we assume that the initial phase angle and the frequencies of these two signals are exactly same. The conversion cycle time of the ADC is Ts (inverse of sampling frequency fs), so the additional time delay between two consecutive channels is Ts.

If the initial phase angle of two signals applied to different channels of a non-simultaneous sampling ADC is zero, then the theoretical additional phase delay in degree between the two consecutive channels can be calculated below:

$$\Delta\Phi_{Delay} = \frac{T_S}{T_{in}} \times 360° = \frac{f_{in}}{f_S} \times 360° \tag{1}$$

Where, fin is the signal frequency of input periodic signal (fin=1/Tin), fadc is the sampling frequency for ADC (fs=1/Ts), 360° is the phase angle of a full cycle. Note that one degree is equal to 60 minutes of arc (arcminute) or 3600 seconds of arc (arcminute).

When ADS8686Soperates on its maximum sampling frequency 1MHz and two 50Hz sinusoidal signals with the same initial phase angle are applied to two consecutive channels, the theoretical phase delay is:

$$\Delta\Phi_{Delay\_CH} = \frac{f_{in}}{f_S} \times 360° = \frac{50Hz}{1MHz} \times 360° = 0.018° \tag{2}$$

If all 8 channels on one ADC of ADS8686S are selected and used, the maximum phase delay in theory between first (1st) and last (8th) channel is:

$$\Delta\Phi_{Delay\_8CH} = 7 \times \Delta\Phi_{Delay\_CH} = 0.126° \tag{3}$$

This phase delay is equal to one complete conversion cycle of the ADC and hence, while such multiplexed systems introduce an additional phase delay between the input channels, the value of this phase delay is deterministic and small if the ADS8686S operates at a fast sampling rate.

3 Averaging with Sequencer and Burst Sequencer mode

3.1 Averaging with Sequencer

The ADS8686S has a highly configurable channel sequencer to reduce the overhead of switching channels on the backend controller or processor, refer to section 7.4.2.5 Sequencer for details in ADS8686S data sheet. By configuring ADS8686S in a certain sequential order to scan the channels, the sample averaging per channel can be achieved to minimize the phase delay as much as possible. The Sequencer mode on the ADS8686S can be used to flexibly configure the sequence of channel switching to perform this operation.

As a 4-channel example shown in Figure 3-1, the sequencer for sample averaging is configured as: AIN0 -> AIN1-> AIN2 - > AIN3 -> AIN2 -> AIN1 -> AIN0. The conversion data displayed at S0,S1…S6 are captured and converted at a t0,t1…t6 for each channel, the time interval between them is determined by the sampling rate of ADC(fs=1/Ts), the time interval between two samples is constant when the sampling rate of ADC is not changed.

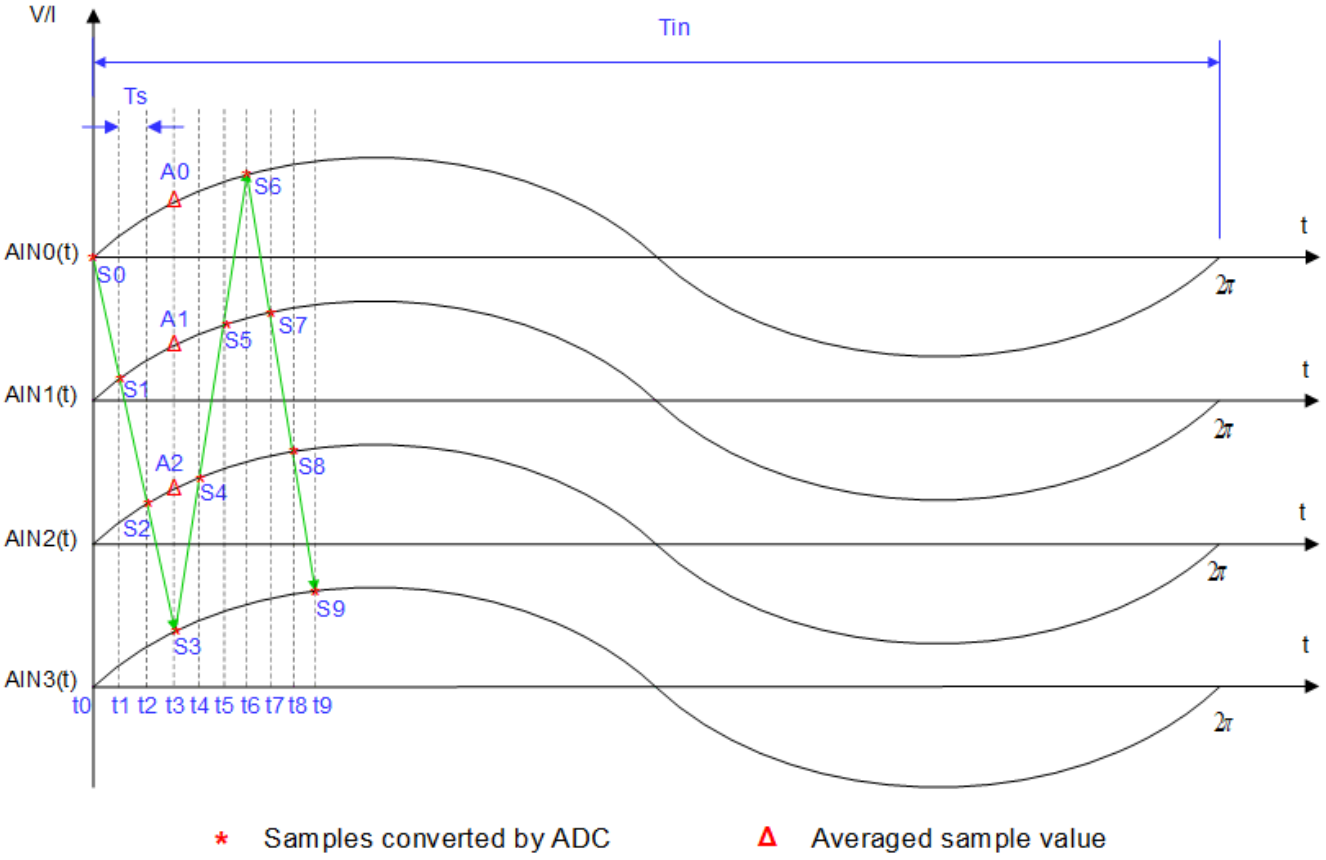

Figure 3-1. Averaged samples aligned with the sample on AIN3

The sample averaging is implemented by averaging the samples on each channel, for example, the averaged data SA0 on channel AIN0 is got by averaging the captured data S0 and S6, A0 = (S0+S6)/2, the same calculation can be used for the rest of channels, AIN1 and AIN2, so A1 = (S1+S5)/2 and A2 = (S2+S4)/2. Because the sampling interval is exactly same, so these averaged data (A0,A1 and A2) and the original sampled data(S3) are located at the same time position t3, all averaged values are highly close to the sample value S3 on the AIN3 channel if the same sinusoidal signal signal is applied on all input channels of the ADC. Hence, the phase delay between channels due to channel switching on the internal multiplexer is reduced and minimized with sample averaging.

3.2 Averaging with Burst Sequencer

The Sequencer mode is very flexible to select the channels in the specific order, while the ADS8686S also offers an additional Burst mode; the Burst feature is applicable only when the sequencer mode is enabled.

When the Burst mode is enabled, only one CONVST pulse can initiate the conversions for all input channels configured in the sequencer instead of more CONVST pulses required in the Sequencer only mode. By using the Burst Sequencer mode, the sample averaging method can significantly save the resource on the host controller or processor.

The Burst Sequencer can operate at either hardware mode or software mode. In hardware mode, the Burst Sequencer mode is enabled by setting the BURST and SEQEN pins on ADS8686S to high. The CHSEL[2:0] are logic pins to select input channels or program the hardware mode sequencer, the logic levels of CHSEL[2:0] pins are launched when the /RESET pin is released these levels determine the channel sequence selected for the conversion and averaging in the Burst Sequencer mode. Refer to the *ADS8686S16-Channel, 16-Bit, 1-MSPS, Dual, Simultaneous Sampling ADC with Integrated Analog Front-End* Hardware Mode Burst Sequencer section 7.4.2.6.1 data sheet for the details.

The timing for the Burst Sequencer in hardware mode is shown in Figure 3-2, and only one CONVST pulse is required for the data conversion on all input channels.

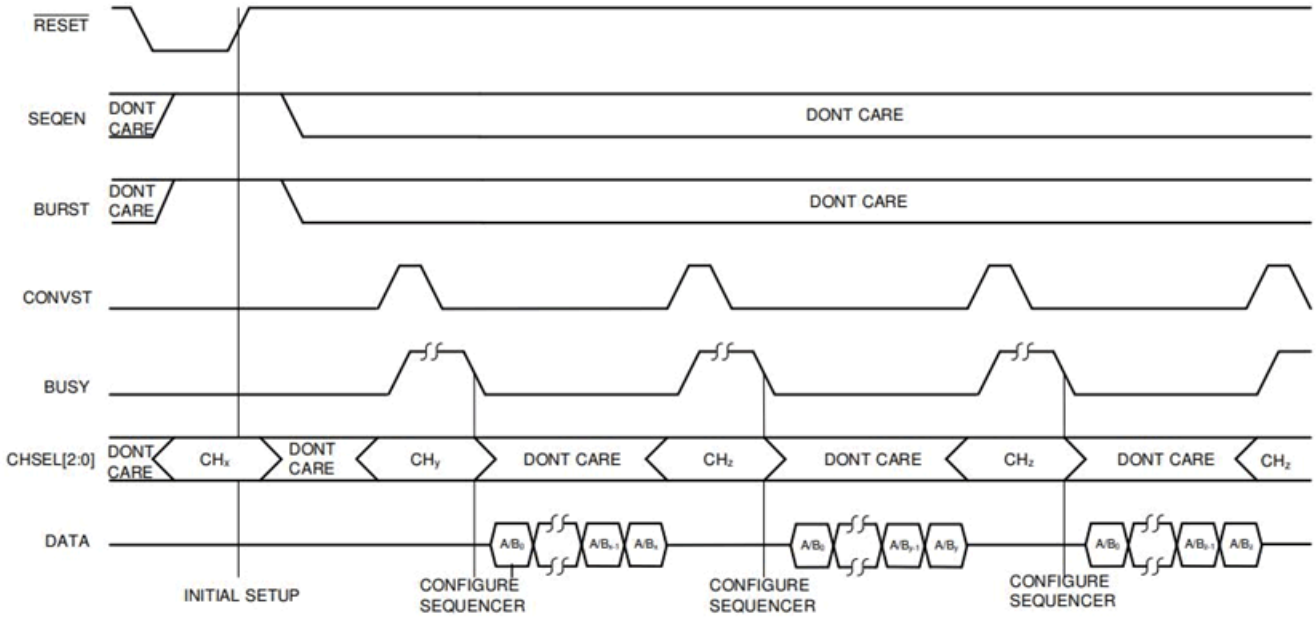

Figure 3-2. Timing for Burst Sequencer, Hardware Mode

In software mode, setting the BURST bit in the Configuration Register to 1 can enable the Burst function. Also, setting the SEQEN bit in the Configuration Register to 1 can enable the Sequencer function. The ADS8686S offers a 32-stack, configurable sequencer. The sequencer stack registers are used to select the channels for data conversion in a certain order according to the channel sequence introduced in the section 3.1 for sample averaging. Refer to the *ADS8686S16-Channel, 16-Bit, 1-MSPS, Dual, Simultaneous Sampling ADC with Integrated Analog Front-End* section 7.4.2.6.2 data sheet for further details about Software Mode Burst Sequencer.

4 Verification and Measured Result

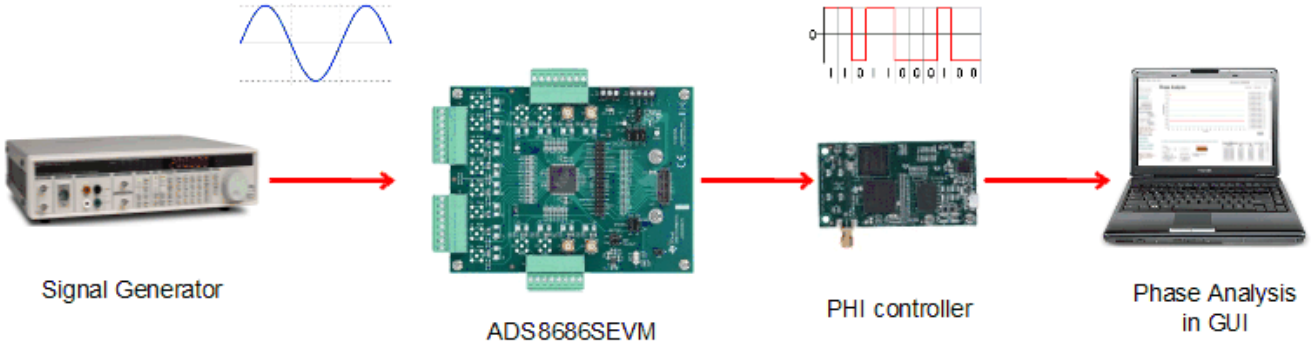

Figure 4-1. Test Setup

The test setup is shown in Figure 4-1. The precision signal generator provides a clean sinusoidal test signal to all input channels of the ADS8686S on the EVM board. Applying the same test signal to all input channels of the ADC ensures that the measured phase delay does not contain any phase differences between different signal sources. Therefore, the measured phase deference between different channels can truly reflect the phase delay caused by the channel switching on the multiplexer of the ADC.

The standard ADS8686SEVM has total 16 inputs for 2x8-ch ADCs on the ADS8686S. As an example, only the 8 input channels on ADC A are used in the test. The ADS8686SEVM board interfaces with a computer through an interface module called the Precision Host Interface (PHI) controller card, which is a part of the ADS8686SEVM-PDK package. The GUI software runs on the computer for data capture, processing and the Phase Analysis software integrated in the EVM GUI is designed and mainly used in the test.

4.1 Phase Delay Measurement

4.1.1 Measured Phase Delay without Averaging – 50Hz Sinusoidal Fundamental Signal

In this case, one pure sinusoidal signal with ±10V signal amplitude and 50Hz signal frequency from the signal generator, which is the fundamental signal of power line in grid infrastructure application, is applied to all 8 input channels of ADS8686S on the EVM board.

To get closer to the real system in grid infrastructure application, the sequencer is programed to sample all signals applied to the 8 input channels of the ADS8686S ADC. When the Phase Analysis page in the GUI software is selected, the sequencer is configured with the sequence introduced in Section 3.1 and Figure 3-1 by choosing the AINxA channels on the top right of the Phase Analysis page.

By default, the phase unit is degree also the Burst mode is checked and enabled in the Phase Analysis page, however the Sampling Averaging option is not enabled. Selecting Continuous in the Capture menu enables continuous data capture and process. The Phase Analysis software can be executed by clicking the Capture button, then the phase delay between channels are shown. Also, the Phase Analysis can quickly track any change of signal frequency with minimum cycles of sampled data on reference channel.

The default reference channel is AIN0A, however other channels can be also chosen. When the AIN7A is selected as reference channel, the phase delay are negative because the ADC scans the channels from AIN0A to AIN7A, thus the phase angle of AIN7A channel is lagging the phase angle of the rest of channels.

The measured phase delay between channels without averaging is shown in Table 4-1.

Table 4-1. Measured Phase Delay without Sample Averaging (50Hz Sinusoidal input)

	Theoretical Delay Δθ (°)	Measured Phase Delay Δθ (°)	
		Phase Delay	Mean
Phase difference (AIN0A – AIN7A)	- 0.126°	- 0.125900°	0.000065°
Phase difference (AIN1A – AIN7A)	- 0.108°	- 0.107756°	0.000056°
Phase difference (AIN2A – AIN7A)	- 0.090°	- 0.089921°	0.000066°
Phase difference (AIN3A – AIN7A)	- 0.072°	- 0.071813°	0.000064°
Phase difference (AIN4A – AIN7A)	- 0.054°	- 0.053747°	0.000058°
Phase difference (AIN5A – AIN7A)	- 0.036°	- 0.035725°	0.000063°
Phase difference (AIN6A – AIN7A)	- 0.018°	- 0.017733°	0.000069°
Reference Channel – AIN7A	0°	0°	

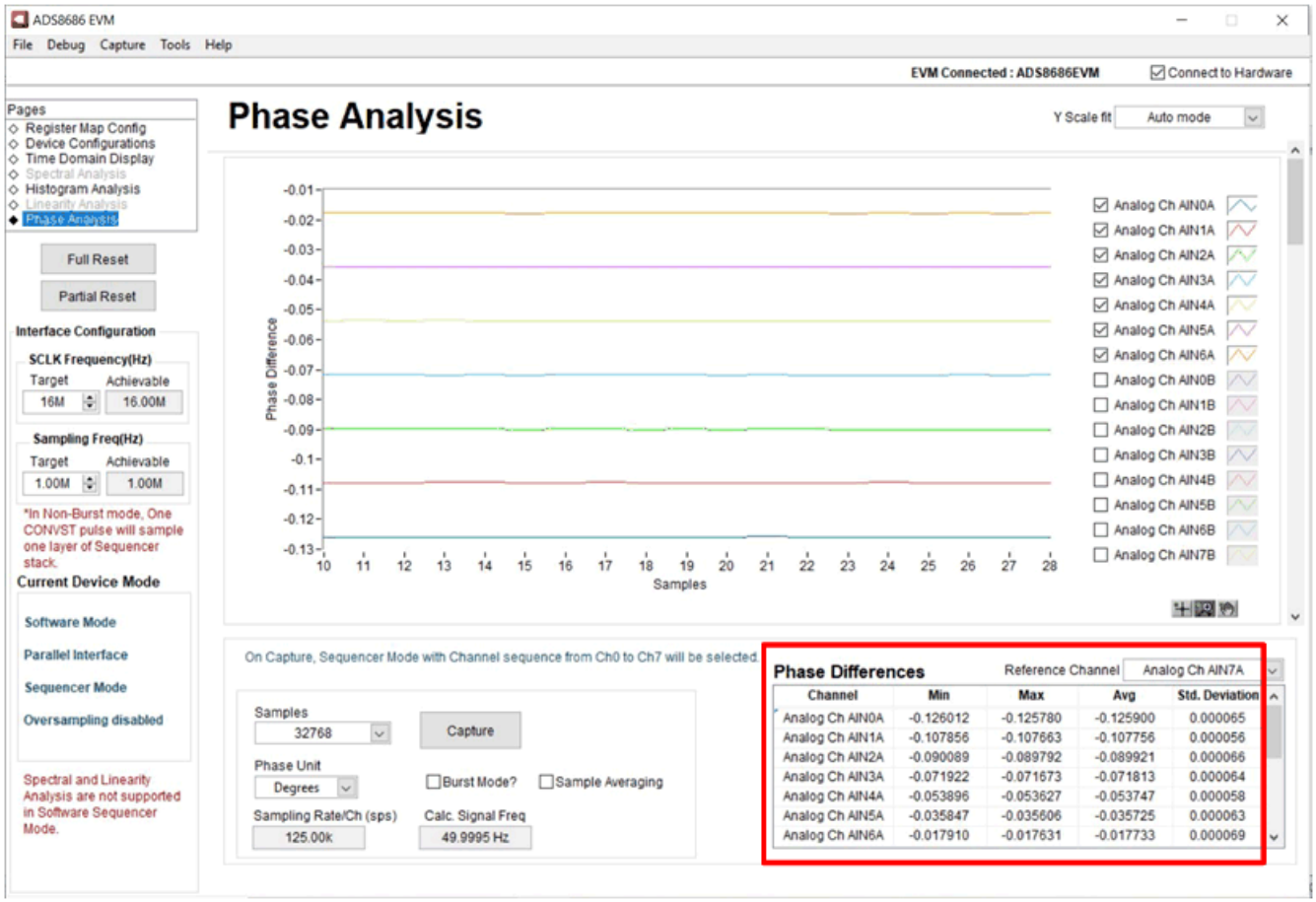

Figure 4-2. Phase Analysis - Phase Delay without Sample Averaging

4.1.2 Measured Phase Delay with Averaging – 50Hz sinusoidal fundamental signal

The measured phase delay between channels with sample averaging can be found in Table 4-2.

Table 4-2. Measured Phase Delay with Sample Averaging (50Hz Sinusoidal input)

	Theoretical Delay Δθ (º)	Measured Phase Delay Δθ (º)	
		Phase Delay	Mean
Phase difference (AIN0A – AIN7A)	- 0.126º	0.000127º	0.000071º
Phase difference (AIN1A – AIN7A)	- 0.108º	0.000281º	0.000061º
Phase difference (AIN2A – AIN7A)	- 0.090º	0.000082º	0.000085º
Phase difference (AIN3A – AIN7A)	- 0.072º	0.000206º	0.000070º
Phase difference (AIN4A – AIN7A)	- 0.054º	0.000246º	0.000075º
Phase difference (AIN5A – AIN7A)	- 0.036º	0.000295º	0.000081º
Phase difference (AIN6A – AIN7A)	- 0.018º	0.000284º	0.000069º
Reference Channel – AIN7A	0º	0º	

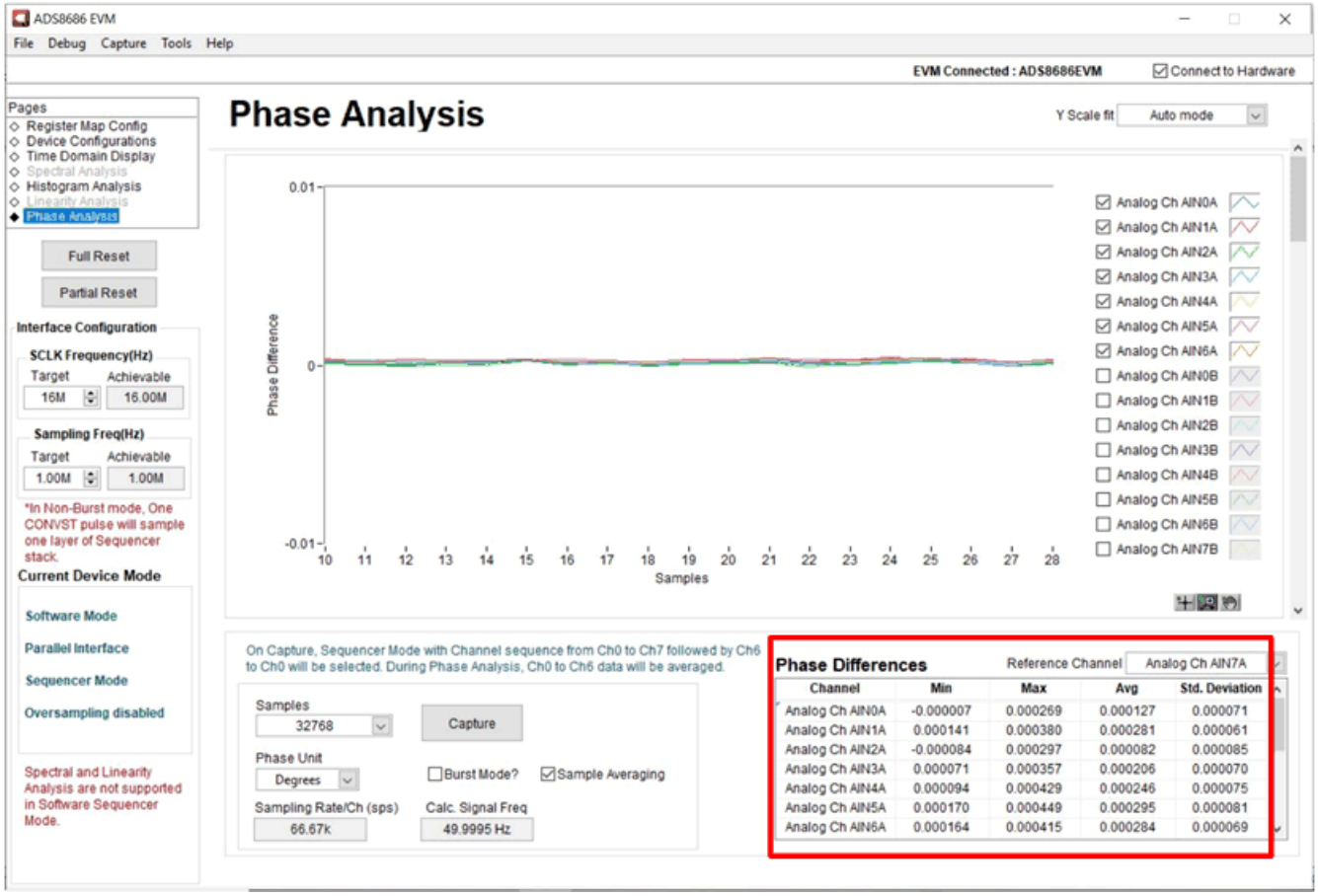

Figure 4-3. Phase Analysis - Phase Delay with Sample Averaging

4.1.3 Comparison

The tests demonstrate that the maximum phase delay between channels is less than 0.005º after sample averaging, which makes ADS8686S able to meet most of requirements on phase measurement application.

4.2 AC Performance

The Phase Analysis integrated in ADS8686SEVM GUI does not have an ability to calculate and show the AC performance including signal-to-noise ratio (SNR) and total harmonic distortion (THD) directly since it is a real-time running software for phase analysis. However, the sample data for each channel can be saved to a .csv file by selecting *Load Data to File* from the menu *Tools -> Data Log* in Time Domain. The data file can be imported to *Analog Engineer Calculator* tool to get SNR and THD. Table 4-3 shows measured results with averaged sample data.

This test shows that the SNR on the averaged channels is better than the reference channel as expected because the noise is reduced by averaging technique. The THD is still maintained in the reasonable range.

Table 4-3. Measured AC Performance with Averaged Samples

Channel	SNR (dB)	THD (dB)	Sample Data
AIN0A	92.24	-104.01	Averaged
AIN1A	92.23	-104.14	Averaged
AIN2A	92.18	-104.19	Averaged
AIN3A	92.11	-104.12	Averaged
AIN4A	91.92	-103.93	Averaged
AIN5A	91.75	-103.67	Averaged
AIN6A	91.44	-103.80	Averaged
AIN7A	90.76	-109.23	No Average on Reference CH

Test condition and procedure

1. Apply - 0.5dBFS, 1kHz sinusoidal signal to all input channels on ADS8686SEVM.
2. Set Load Data to File from the menu Tools -> Data Log in Time Domain page in the GUI.
3. Select Burst Mode and Sample Averaging in Phase Analysis in the EVM GUI.
4. Capture the data with proper number samples. The sample data can be found in the .csv file.
5. Use the Analog Engineer Calculator tool to load the averaged data and check AC performance.

5 Summary

By using the simple averaging technique introduced in this article, the phase delay between channel-to-channel due to channel switching on the multiplexed ADC, ADS8686S, can be significantly reduced. Therefore, the ADS8686S ADC can achieve specified performance like a simultaneous sampling ADC with minimal impact on phase measurement, and is applied in most power protection systems in grid infrastructure application.

6 References

1. Texas Instruments, Phase-Compensated, 8-Ch, Multiplexed Data Acquisition System for Power Automation Reference Design.
2. Texas Instruments, ADS8686S: 16-channel 16-bit 1-MSPS Dual Simultaneous-sampling ADC with Integrated Analog Front End data sheet.
3. Texas Instruments, ADS8686SEVM-PDK and GUI.

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