Application Report

Optimizing On-Board and Wireless Charger Systems Using Logic and Translation

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ABSTRACT

Logic and translation devices are a common addition to any electronic system, and On-board Chargers (OBC) are no different. The primary focus for an OBC system designer is efficient power conversion, which will require communication among several digital control subsystems. With common supply domains of 3.3 V and 5 V, its possible these communications will require some voltage level shifting. Additionally, there is often a need for strengthening microcontroller (MCU) output drive to operate isolated gate drivers that use an opto-couple topology. These use cases, as well as others shown in the *Block Diagram* and *Logic and Translation Use Cases* sections of this document, can be used to optimize system design requirements and enable a functional OBC.

Logic gates, voltage translators, and other logic devices are utilized for many purposes throughout modern electronic systems. This document provides example solutions for common design challenges that can be solved using logic and translation. Not all of the solutions here appear in every system, however all solutions shown are commonly used and effective.

There are dozens of logic families available from Texas Instruments, and it can be difficult to select the right one for the application. OBC's can vary in design topologies, but the key parameters remain the same making it easier to identify an appropriate family for this application. Refer to *Recommended Logic and Translation Families for On-Board and Wireless Chargers* in this document for help finding the right logic family for your use case.

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Trademarks

1 Block Diagram

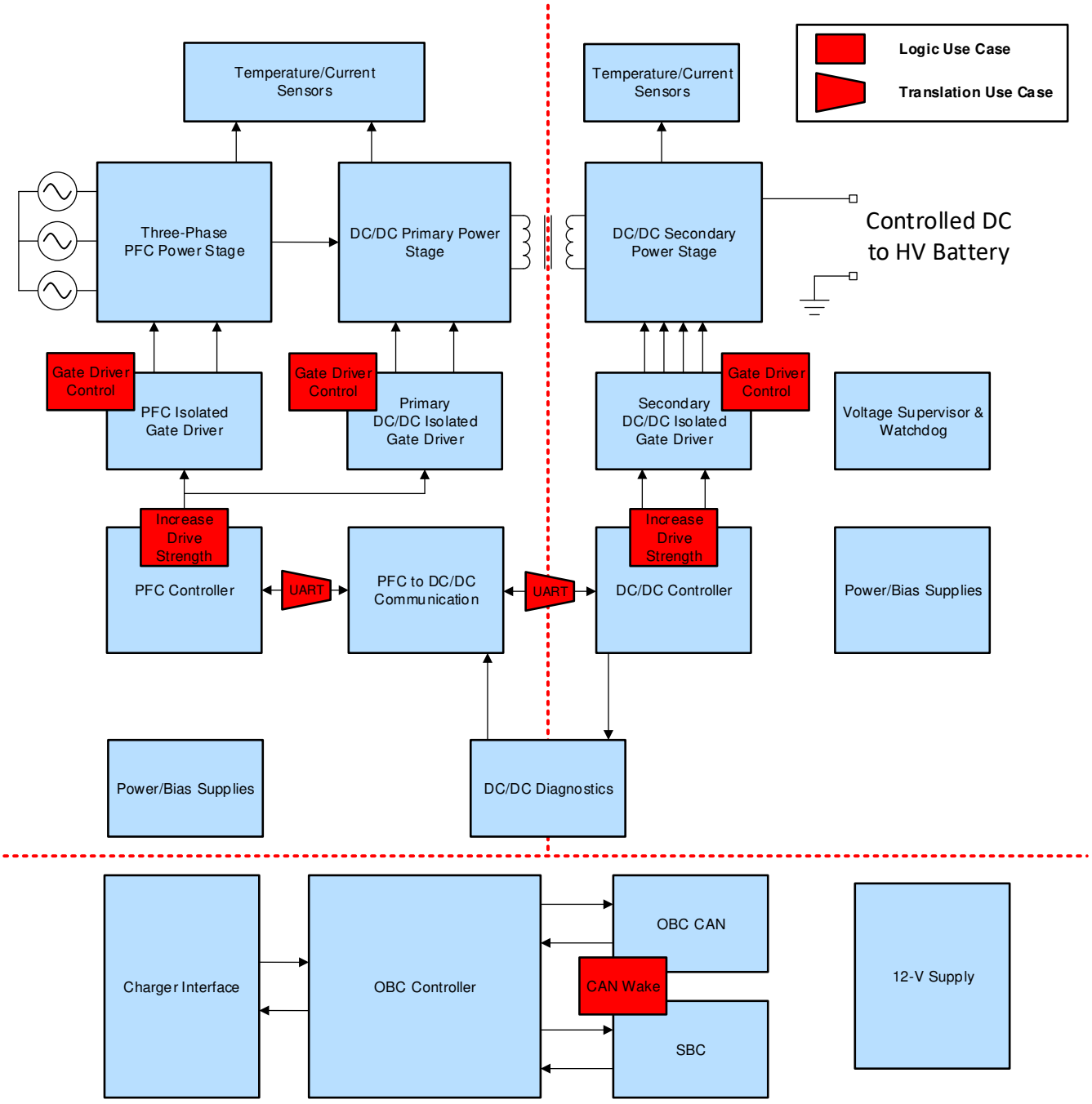

Figure 1-1. Simplified Block Diagram for On-Board and Wireless Charger Systems

See *On-Board and Wireless Chargers* for a more complete view of the interactive online End Equipment Reference Diagram.

2 Optimizing Gate Driver Control and MCU Communication

OBC systems typically contain several isolated gate driver devices to control FETs responsible for the power regulation. Depending on the isolation topology, these gate drivers can require a current drive of up to 20 mA. This may not be an issue if a dedicated PFC controller is used as they typically can source the required current; however, it is common to see other topologies used that utilize a simple MCU or DSP to control the gate drivers for the PFC side and DC/DC side of the system. In this case, it is more likely that additional drive strength is needed and possibly translation up to 5 V from the lower I/O voltage of the MCU.

Figure 2-1 shows an in depth view of how the SN74LVC1G125-Q1 buffer can be used to control an isolated gate driver that uses a opto-couple topology.

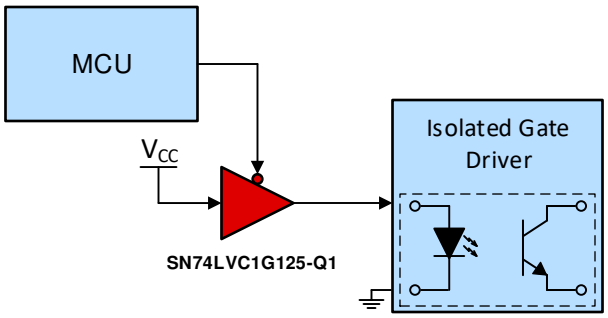

Figure 2-1. Example of Logic Buffer Controlling Isolated Gate Driver

In this example, the $\overline{OE}$ pin of the buffer is being used to control the forward current through the LED. This is one of many different implementations that can be used with a buffer to control the isolated gate driver. This added flexibility is a benefit to adapt to design architecture changes for the ever evolving EV space.

If the signal to the gate driver also needs to be shifted up, this can be done with a voltage translator in the LVC family like the SN74LVC2T45-Q1. Translators in these families have higher drive and can shift up to the 5 V typically required. These voltage translators can also be used for any UART, SPI, or SCI communication between the primary and secondary MCUs if isolation is not required. If isolation is required, the level shifting functionality is typically integrated in the digital isolators from Texas Instruments so additional devices will not be required.

3 Logic and Translation Use Cases

3.1 Logic Use Cases

3.1.1 Increase Drive Strength

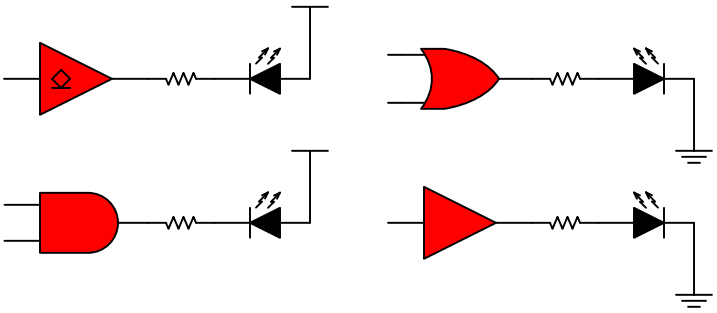

Figure 3-1. Using Logic to increase LED Drive Strength.

- Provide additional drive to MCUs with a small form factor
- Drive low current LEDs (1 mA to 25 mA) with most logic gates
- See Section 3.1.2 for more information about how logic functions add configurability
- See *online parametric search tool* to find the right buffer or inverter

3.1.2 Gate Driver Control

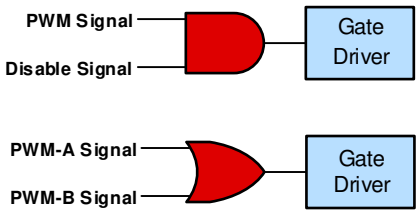

Figure 3-2. Using Combinational Logic for Additional Gate Driver Control

- Add simple PWM disable control
- Create PWM signal from other signal combinations
- Logic functions add flexibility for system adaptations
- See *online parametric search tool* to find the right gate

3.1.3 Low-Power CAN Wake

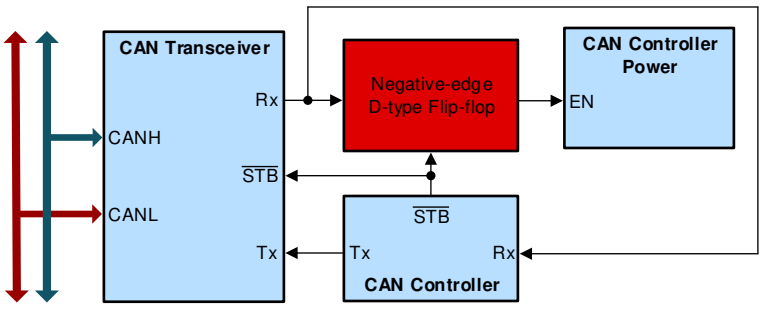

Figure 3-3. Using Logic to Enable CAN Controller Power With Wake-Up Pattern

- Conserve power leaving the CAN controller in a power down state
- Flexible solution to accommodate any active high or active low enables
- Trigger immediately after the wake-up pattern is read
- Look here to find more information about the negative-edge D-type flip-flop

3.2 Voltage Translation Use Cases

3.2.1 Non-Isolated SPI Communication

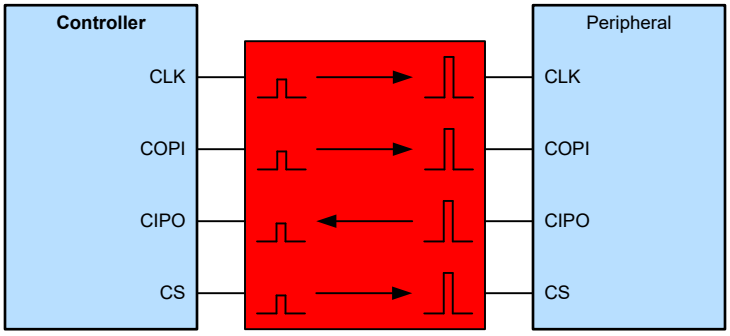

Figure 3-4. Using Voltage Translation with a SPI-Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provide protection from disconnected peripherals
- See *online parametric search tool* to find the right voltage level translator

3.2.2 Non-Isolated UART Communication

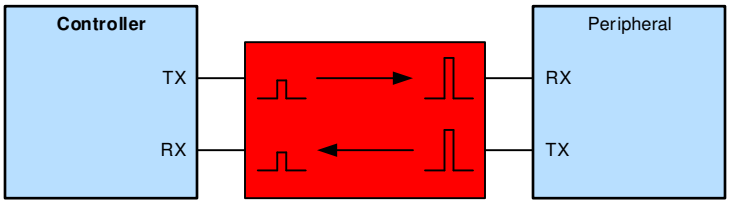

Figure 3-5. Using Voltage Translation with UART Communication

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect the controller while peripheral is not connected
- See *online parametric search tool* to find the right voltage level translator

4 Recommended Logic and Translation Families for On-Board and Wireless Chargers

4.1 LVC: Low-Voltage CMOS Logic and Translation

Key features: SN74**LVC**xxxx

- Huge portfolio of logic functions
- LVC: 4+ channels per package
- Over-voltage tolerant inputs allow unidirectional down-translation with any function
- High-drive outputs (up to 32 mA)
- Up to 250 Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging options: SOIC, TSSOP, VQFN, SOP, and SSOP

Key features: SN74**LVCxG**xxxx

- Put 1, 2, or 3 channels of any logic function right where you need them
- Configurable gates available ('57, '58, '97, '98, and '99 functions)
- Over-voltage tolerant inputs allow unidirectional down-translation with any gate or buffer
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging options: SOT-23, SC70, X2SON, SOT-5X3, SON, and DSBGA

Key features: SN74**LVCxT**xxxx

- LVCxT: up and down translation across 1.65 V to 5.5 V
- 1, 2, 8, or 16 channels per device
- High-drive outputs (up to 32 mA)
- Up to 250-Mbps operation
- I_{off} supports partial-power-down mode operation

See *online parametric search tool* to find the right LVC family logic and voltage level translation devices.

4.2 HCS: Schmitt-Trigger Integrated High-Speed CMOS Logic

Key Features:

- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power with maximum I_{CC} of 2 µA
- Wide voltage operating range of 2 V to 6 V
- Contains new function not found in other logic families
- Inputs and output include positive and negative clamp diodes
- Packaging Options: SOIC and TSSOP

See *online parametric search tool* to find the right HCS family logic devices.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (April 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Updated the *Using Voltage Translation with a SPI-Communication Bus* figure for inclusive SPI terms	5

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