Application Report
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Migration from the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family to the MSP430FR4xx and MSP430FR2xx family

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ABSTRACT

This application report enables easy migration from the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family to the MSP430FR4xx and MSP430FR2xx family. This report describes programming, system, and peripheral considerations when migrating firmware. The intent is to highlight key differences between the two families. For more information on the use of the MSP430FR4xx and MSP430FR2xx devices, see the MSP430FR4xx and MSP430FR2xx family user's guide.

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Trademarks

1 Introduction

The MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx devices and the MSP430FR4xx and MSP430FR2xx devices are FRAM-based MCUs that are part of TI's MSP430™ ultra-low-power sensing & measurement MCUs portfolio.

- Most of the MSP430FR4xx and MSP430FR2xx devices are part of the MSP430 value line & general purpose microcontrollers portfolio.
- The MSP430FR25xx and MSP430FR26xx devices are part of the MSP430 capacitive touch sensing microcontrollers portfolio. Migrating to these devices is similar to other family members except for the use of CapTIvate™ technology. For information about this technology and its ecosystem, visit the capacitive touch sensing portfolio.
- Some MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx devices are also part of the MSP430 value line & general purpose microcontrollers portfolio, while other devices are part of the MSP430 ultrasonic & rotary flow sensing microcontrollers portfolio.

This application report describes the key differences between the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family and the MSP430FR4xx and MSP430FR2xx family to ensure a smooth migration. This document is divided into system-level considerations (such as power management) and peripheral modifications. With respect to the instruction set, the MSP430FR4xx and MSP430FR2xx family is completely code compatible with all other MSP430 families. Any code migration is therefore affected only by register or peripheral feature changes and slight variations in instruction cycle times, while the instruction set remains the same. Driver library is supported in both the MSP430FR4xx and MSP430FR2xx family and the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family. Use of driver library can avoid register changes in most cases.

For specific information on the MCUs, see the device-specific data sheets, errata, and family user's guides.

NOTE: For the purpose of this application report, the term "FR4xx" indicates the MSP430FR4xx and MSP430FR2xx devices, and the term "FR59xx" indicates the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx devices.

2 Configuration of MSP430FR4xx and MSP430FR2xx Devices

Table 1 summarizes the primary differences among the FR4xx devices.

Table 1. F4xx Family Device Comparison

Feature or Module	FR413x, FR203x	FR2433, FR263x, FR253x	FR231x	FR21xx, FR2000	FR235x, FR215x	FR267x, FR247x
CPU	16-MHz MSP430	16-MHz MSP430	16-MHz MSP430	16-MHz MSP430	24-MHz MSP430	16-MHz MSP430
Program FRAM	15.5KB or 8KB	15.5KB or 8KB	3.75KB or 2KB	3.75KB, 2KB, 1KB, or 0.5KB	32KB or 16KB	64KB or 32KB
Information FRAM	512 bytes	512 bytes	N/A	N/A	512 bytes	512 bytes
SRAM	2KB or 1KB	4KB, 2KB, or 1KB	1KB	1KB or 0.5KB	4KB or 2KB	8KB or 6KB
Maximum GPIOs	60	19	16	12	44	43
Interrupt pins	16 (P1 and P2)	16 (P1 and P2)	12 (8 pins of P1 and 4 pins of P2)	8 (4 pins each of P1 and P2)	32 (P1, P2, P3 and P4)	All GPIOs
USCI	1 eUSCI_A, 1 eUSCI_B	2 eUSCI_A, 1 eUSCI_B	1 eUSCI_A, 1 eUSCI_B	1 eUSCI_A	2 eUSCI_A, 2 eUSCI_B	2 eUSCI_A, 2 eUSCI_B
ADC	ADC10 (10 channel)	ADC10 (8 channels)	ADC10 (8 channels)	ADC10 (8 channels)	ADC12 (12 channels)	ADC12 (12 channels)
Comparator	N/A(1)	N/A	1	1	1 LP eCOMP, 1 HS eCOMP	1 LP eCOMP
Analog features	N/A	N/A	1 SAC-L1 (OA), 1 TIA	N/A	4 SAC-L3	N/A
Timer	2 Timer_A with 3CC(2), RTC counter, WDT	2 Timer_A with 3CC, 2 Timer_A with 2CC, RTC counter, WDT	2 Timer_B with 3CC, RTC counter, WDT	1 Timer_B with 3CC, RTC counter, WDT	3 Timer_B with 3CC, 1 Timer_B with 7CC, RTC counter, WDT	4 Timer_B with 3CC, 1 Timer_B with 7CC, RTC counter, WDT
Additional features	Temperature sensor, brownout reset, capacitive touch I/O, LCD in FR4133	Temperature sensor, brownout reset, MPY32, CapTIvate™ technology in FR263x and FR253x	Temperature sensor, brownout reset, capacitive touch I/O	Temperature sensor, brownout reset, capacitive touch I/O	Shared voltage reference for ADC, DAC, and eCOMP, low-power REFO selectable, temperature sensor, brownout reset, capacitive touch I/O	Shared voltage reference for ADC, DAC, and eCOMP, low-power REFO selectable, temperature sensor, brownout reset, MPY32, CapTIvate technology in FR267x
BSL	UART	I^2C, UART	I^2C, UART	UART	I^2C, UART	I^2C, UART
V_{CC}	1.8 V to 3.6 V	1.8 V to 3.6 V	1.8 V to 3.6 V	1.8 V to 3.6 V	1.8 V to 3.6 V	1.8 V to 3.6 V
Active power	126 µA/MHz	126 µA/MHz	126 µA/MHz	126 µA/MHz	142 µA/MHz	135 µA/MHz
Operating temperature	–40°C to 85°C	–40°C to 85°C	–40°C to 85°C	–40°C to 85°C	–40°C to 105°C	–40°C to 105°C
Package	LQFP64, TSSOP56, TSSOP48	VQFN24	TSSOP20, TSSOP16, QFN16	TSSOP16, QFN24	LQFP48, QFN40, TSSOP38	LQFP48, VQFN40, VQFN32

(1) N/A = not available

(2) CC = capture/compare registers

Table 2 summarizes the memory maps of example FR4xx MCUs.

Table 2. Comparison of Memory Maps

	Access	FR4133	FR2633	FR2311	FR2111	FR2355	FR2676
Memory (FRAM)	R/W Optional write protect	15KB	15KB	3.75KB	3.75KB	32KB	64KB
Main: interrupt vectors and signatures		FFFFh to FF80h	FFFFh to FF80h	FFFFh to FF80h	FFFFh to FF80h	FFFFh to FF80h	FFFFh to FF80h
Main: code memory		FFFFh to C400h	FFFFh to C400h	FFFFh to F100h	FFFFh to F100h	FFFFh to 8000h	17FFFh to 8000h
Information memory (FRAM)	R/W Optional write protect	512B 19FFh to 1800h	512B 19FFh to 1800h	N/A	N/A	512B 19FFh to 1800h	512B 19FFh to 1800h
RAM	R/W	2KB 27FFh to 2000h	4KB 2FFFh to 2000h	1KB 23FFh to 2000h	1KB 23FFh to 2000h	4KB 2FFFh to 2000h	8KB 3FFFh to 2000h
ROM BSL	R	1KB 13FFh to 1000h	2KB 17FFh to 1000h 1KB FFFFFh to FFC00h	2KB 17FFh to 1000h 1KB FFFFFh to FFC00h	1KB 13FFh to 1000h	2KB 17FFh to 1000h	2KB 17FFh to 1000h 1KB FFFFFh to FFC00h
Peripherals	R/W	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h	4KB 0FFFh to 0020h
ROM library	R	N/A	CapTIvate libraries and driver libraries, 12KB 6FFFh to 4000h	N/A	N/A	CapTIvate libraries, FFT and driver libraries, 20KB FFBFFh to FAC00h	CapTIvate libraries, FFT and driver libraries, 16KB C3FFFh to C0000h

The registers of the SYS module differ by device. For details, see the MSP430FR4xx and MSP430FR2xx family user's guide.

3 In-System Programming of Nonvolatile Memory

3.1 Ferroelectric RAM (FRAM) Overview

Both the FR4xx MCU and FR59xx MCU support FRAM nonvolatile memory. Using FRAM is very similar to using static RAM (SRAM). The introduction of FRAM as an embedded memory in a general-purpose ultra-low power MCU was in the Texas Instruments 16-bit MSP430 product line, in the MSP430FR57xx MCUs.

Some of the key attributes of FRAM are:

- FRAM is nonvolatile. It retains its contents on loss of power.
- The embedded FRAM on MSP430 devices can be accessed (read or write) at up to a maximum speed of 8 MHz. Above 8 MHz, wait states are used when accessing FRAM.
- Writing to FRAM and reading from FRAM requires no setup or preparation such as pre-erase before write operation.
- FRAM is not segmented and each bit is individually erasable, writable, and addressable.
- FRAM segments do not require an erase before a write.
- FRAM write accesses are low power, because writing to FRAM does not require a charge pump.
- FRAM writes can be performed across the full voltage range of the device.
- FRAM write speeds can reach up to 8 MBps with a typical write speed of approximately 2 MBps. The high speed of writes is inherent to the technology and aided by the elimination of the erase bottleneck that is prevalent in other nonvolatile memory technologies. In comparison, typical MSP430 flash write speed including the erase time is approximately 14 kBps.

3.2 FRAM Cell

A single FRAM cell can be considered a dipole capacitor that consists of a film of ferroelectric material (ferroelectric crystal) between two electrode plates. Storing a 1 or 0 (writing to FRAM) simply requires polarizing the crystal in a specific direction using an electric field. This makes FRAM very fast, easy to write to, and capable of meeting high endurance requirements.

Reading from FRAM requires applying an electric field across the capacitor similar to a write. Depending on the state of the crystal, it may be repolarized, thereby emitting a large induced charge. This charge is then compared to a known reference to estimate the state of the crystal. The stored data bit 1 or 0 is inferred from the induced charge. In the process of reading the data, the crystal that is polarized in the direction of the applied field loses its current state. Every read must be accompanied by a write-back to restore the state of the memory location. With TI's MSP430 FRAM MCUs, this is inherent to the FRAM implementation and is completely transparent to the application. The write-back mechanism is also protected from power loss and completes safely under all power-fail events.

The FR59xx power management system achieves this by isolating the FRAM power rails from the device supply rails in the event of a power loss. The FRAM power circuitry also uses built-in low dropout regulator (LDO) and a capacitor that store sufficient charge to complete the current write-back in the event of a power failure.

3.3 Protecting FRAM Using Write Protection Bits in FR4xx Family

In FR4xx family, because FRAM is very easy to reprogram, it also makes it easy for erroneous code execution to unintentionally overwrite application code, just as it would if executing from RAM.

To safeguard against erroneous overwriting of FRAM, memory write protection is provided. FR4xx provides two separate write protection bits:

- SYSCFG0.PFWP: User program FRAM protection
- SYSCFG0.DFWP: User data FRAM (information memory 1800h to 19FFh) protection
- SYSCFG0.FRWPOA: Program FRAM write protection offset address from the beginning of Program FRAM. The offset increases by 1KB resolution

When writing the SYSCFG0 register, write the protection password (SYSCFG0.FRWPW = 0xA5) in a word with the other bits.

Table 3 summarizes protecting FRAM features in the typical device of MSP430FR4xx and MSP430FR2xx family.

Table 3. F4xx FRAM Protection Comparison

Feature	FR2033	FR4133	FR2433	FR2311	FR2111	FR2355	FR2476
Protection password (SYSCFG0.FRWPPW)	N	N	Y	Y	Y	Y	Y
The program FRAM write protection (SYSCFG0.PFWP)	Y	Y	Y	Y	Y	Y	Y
The data FRAM protection (SYSCFG0.DFWP)	Y	Y	Y	N	N	Y	Y
Program FRAM write protection offset address (SYSCFG0.FRWPOA)	N	N	N	N	N	Y	Y

In the FR59xx family, a memory protection unit (MPU) is provided. It is recommended to set boundaries between code and data memory to increase code security and protect against accidental writes or erasures. The MPU allows users to separate blocks of FRAM and assign unique privileges to each block based on the application's requirement. For example, if a memory block is assigned read only status, any write access to that block is prevented and an error is flagged. This is useful for storing constant data or application code that is not expected to change over the device lifetime

3.4 FRAM Memory Wait States

Both the FR4xx MCU and FR59xx MCU are FRAM based MCU. The maximum FRAM memory access speed is 8 MHz. If the MCLK is operating faster than 8 MHz, wait-states are required to ensure reliable FRAM access. When using MCLK ≥ 8 MHz, configure the FRAM wait states in software before configuring the MCLK frequency.

1. Configure the appropriate wait states.

```
FRCTL0 = FRCTLPW | NWAITS_x
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2. Configure MCLK ≥ 8 MHz

For more information, see the *Wait State Control* section of the *FRAM Controller (FRCTRL)* chapter in the MSP430FR4xx and MSP430FR2xx family user's guide and the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family user's guide.

3.5 Bootloader (BSL)

The BSL is software that is used to reprogram the MCU, for example, during field firmware updates. On the FR4xx family of devices, the BSL uses a Timer_A-based UART and is located in ROM. The BSL is not erasable or customizable by the user.

Both the FR4xx MCU and FR59xx MCU use the hardware eUSCI_A module to implement UART communication in BSL. Hence, the module pins UCA0TXD and UCA0RXD are used for BSL communication. And the $\overline{\text{RST}}$/NMI/SBWTDIO pin and TEST/SBWTCK pin are used for BSL entry sequence.

The BSL on the FR2433, FR263x, FR253x, FR231x, FR235x, FR215x, FR267x, and FR247x devices support both UART and I^2C communications. The BSL scans the UART and I^2C peripherals to detect which interface is used by the host programmer. When a transmission is detected on one of the peripherals, that interface is selected and the other is disabled by the BSL. For details, see the MSP430 FRAM device bootloader (BSL) user's guide.

FR59xx device variants using an I^2C hardware interface for the BSL are also available. However, for a given device variant, only the factory-configured interface can be used.

Blank device detection function is supported in some FR4xx device. For details, see the MSP430 FRAM device bootloader (BSL) user's guide.

The BSL in both the FR4xx MCUs and FR59xx MCUs can be disabled by programming a specific signature to the BSL signature location. For detailed on the FR4xx setting, see Table 4.

3.6 JTAG and Security

On the FR4xx devices, the JTAG/SBW is locked by programming a specific signature into the device's FRAM memory at JTAG/SBW signature address of FF80h to FF83h.

When JTAG/SBW is locked by programming the JTAG/SBW signature, access to the device is only possible through the BSL (using the BSL password). However, when the BSL is not disabled and the BSL password is supplied, it is possible to clear the JTAG/SBW signature and make JTAG communication available again. Hence, on the FR4xx devices, locking the JTAG/SBW is reversible if the BSL password is known and BSL is not disabled.

Table 4 describes the FR4xx device password, BSL signature, and JTAG/SBW signature.

Table 4. FR4xx Device Password, BSL Signature, and JTAG/SBW Signature

Name	Address	Value	Device Security	BSL or SBW Behavior After Reset
Device password	FFE0h to FFFFh	Depending on vector table configuration		The value is used to protect BSL.
BSL signature	FF84h to FF87h	5555_5555h	Secured, password not required	BSL is bypassed. User code starts immediately.
		Any other values	Secured, password required through the BSL	BSL is invoked before user code starts if BSL is triggered.
JTAG/SBW signature	FF80h to FF83h	FFFF_FFFFh	Not secured	JTAG/SBW is not locked.
		0000_0000h		
		Any other values	Secured	JTAG/SBW is locked.

On the FR59xx devices, a fuse is used. Securing the device involves writing a specific signature to the JTAG signature location. When the fuse is programmed, access to the device is possible only through the BSL (using the BSL password). However, when the BSL password is supplied, it is possible to clear the JTAG fuse and make JTAG communication available again. Hence, on the FR59xx devices, blowing the JTAG fuse is reversible if the BSL password is known. The FR59xx family also provides an addition feature: JTAG lock with password. The password is located at FRAM location 0xFF88 and can be one to four words in length. To be able to access JTAG, the tool chain needs to first provide the password, following which JTAG access is granted. Any access with an incorrect password prevents JTAG access. When a password is verified, complete JTAG access is possible until the next BOR event.

3.7 Production Programming

MSP-GANG430 does not support either FR4xx or FR69xx devices. The MSP-GANG production programmer supersedes the MSP-GANG430 and supports both.

4 Hardware Migration Considerations

- For JTAG and SBW connections on both the FR4xx and FR59xx devices, see the MSP430 Hardware Tools User's Guide. Note the parallel capacitor on the pin $\overline{\text{RST}}$/NMI/SBWTDIO should be less than 1.1 nF when using SBW for debug or firmware download.
- Both the FR4xx and FR59xx devices provide an internal pullup resistor on the reset line, which eliminates the need for an external reset resistor. For details, see the Special Function Register (SFR) (SFRRPCR) in the MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family user's guide.
- Neither the FR4xx nor the FR59xx devices provide internal load capacitors on the LFXT oscillator. External load capacitors are required if the LFXT oscillator is used. For layout, the external crystal must be as close as possible to FR4xx pins XIN and XOUT. The load capacitors must be placed close to crystal pins. The capacitor values must be matched with crystal specification and PCB layout. For more guidance about crystal selection, layout concerns and crystal oscillator testing, see MSP430 32-kHz crystal oscillators.
- Compared to the FR59xx family, the FR4xx clock system is quite different. There is an FLL and an internal trimmed REFO in FR4xx devices that can generate a REFO clock at 32.768 kHz with accuracy of ±3.5% in the full temperature range. For detailed information, see Section 7.2.2 and the *Clock System* chapter of the MSP430FR4xx and MSP430FR2xx family user's guide

- The FR231x, FR235x, and FR215x MCUs support a high-frequency clock source on the XT1 oscillator. The FLL reference divider FLLREFDIV is available only when XT1 HF mode is supported in the device. The FR59xx devices do not support a high-frequency clock source on the LFXT oscillator. If a high frequency clock source is used, it must be connected to the secondary crystal oscillator (XT2).
- F59xx devices have analog voltage supply pins (AVCC and AVSS) and digital voltage supply pins (DVCC and DVSS). FR4xx devices have only one pair of power supply pins (DVCC and DVSS).
- FR235x and FR215x MCUs support –40°C to 105°C operating temperature. –40°C to 105°C system requirement can be matched using the devices.

5 Device Calibration Information

The TLV information on both FR4xx and FR59xx devices are stored in protected FRAM where it cannot be erased by in-application or external access (such as through the BSL). For details on the location and access of the TLV, see the device-specific data sheet.

NOTE: Another information memory area at 1800h to 19FFh is available for application use on the FR4xx devices, except MSP430FR231x and MSP430FR211x

The TLV structure contains calibration values can be used to improve the measurement accuracy of various functions. The calibration values available on a given device are shown in the TLV structure of the device-specific data sheet. In the FR4xx data sheets, ADC offset and gain calibration data, and temperature sensor calibration data are provided.

The TLV in the FR59xx family includes an extra field to store a random number seed that is generated on a per device basis at production. The random number is not included in the FR4xx TLV

6 Important Device Specifications

Table 5 lists important differences in device-level electrical specifications. [4] [5]

Table 5. Device-Level Electrical Specifications

Parameter	FR4xx	FR59xx
Supply voltage range	1.8 V to 3.6 V(1)(2)	1.8 V to 3.6 V(1)
Maximum system frequency, f_{SYSTEM}(3)	16 MHz at V_{CC} = 1.8 V, 24 MHz at V_{CC} = 1.8 V	16 MHz at V_{CC} = 1.8 V
Minimum supply voltage for nonvolatile memory programming	1.8 V	1.8 V
Minimum analog supply voltage for ADC operation	2.0 V	1.8 V

(1) The minimum operating voltage depends on the SVSH voltage levels.
(2) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range.
(3) See the device-specific data sheet for the specified operating conditions.

7 Core Architecture Considerations

7.1 Power Management Module (PMM)

7.1.1 Core LDO and LPM3.5 LDO

The FR4xx family uses a single voltage supply. However unlike FR59xx, there are no AVCC and AVSS pins, only DVCC and DVSS. The external voltage supply on the DVCC pin is fed to an internal low-dropout voltage regulator (LDO) (see Figure 1).

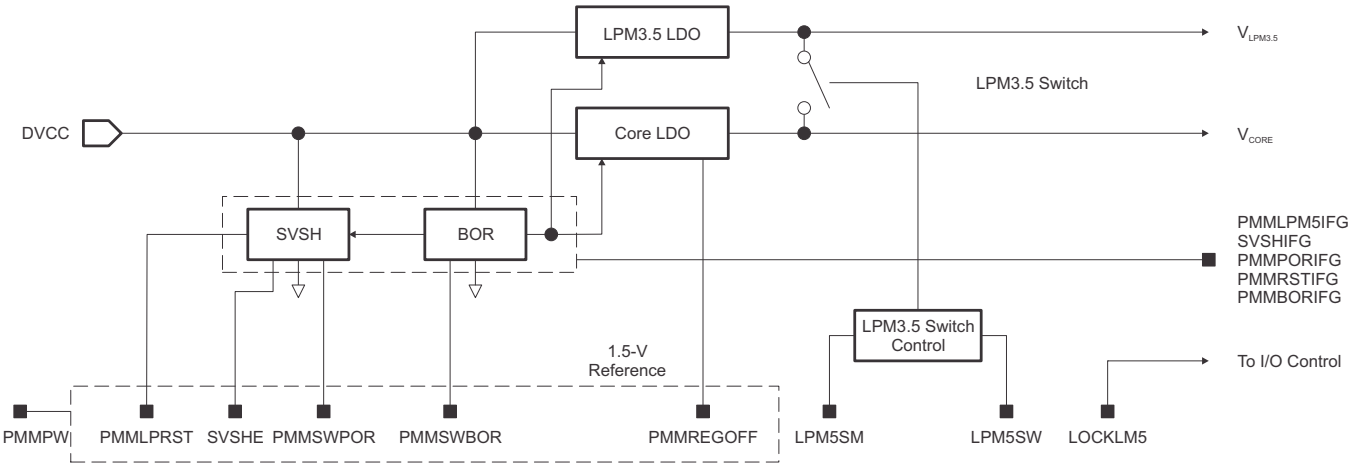

Figure 1. FR4xx PMM Block Diagram

The PMM manages all functions related to the core voltage and its supervision. Its primary functions are, first, to generate a supply voltage for the core logic and, second, to provide several mechanisms for the supervision of both the voltage supplied to the device (DVCC) and the voltage generated for the core (VCORE).

Using the PMM is especially advantageous as it allows the core to operate at a lower voltage, which brings significant power savings. It also ensures that the core receives a stable and regulated voltage over a wide supply range.

There is a second LDO integrated in FR4xx, the LPM3.5 LDO. This LDO supplies the current for the LPM3.5 power domain logic, which contains the RTC and LCD modules (only the MSP430FR4xx MCUs have the LCD module). In LPMx.5 low-power modes, the Core LDO is turned off. When entering LPM3.5, the LPM3.5 switch is turned off to save power consumption. When exiting LPM3.5 power mode, the LPM3.5 switch is turned on so that the core LDO can supply power to the LPM3.5 domain logic to support high-frequency operation (see Figure 1).

7.1.2 SVS

Because supply voltage supervision (SVS) is an important aspect of providing a stable supply or a notification in case of power failure, the FR4xx provides the high-side supply voltage supervision (SVSH) block The SVSH supervises of the external chip supply (DVCC), and the PMM internally supervises the low-side supply to the core.

In both FR4xx and FR59xx devices, the SVS threshold tracks directly with the device minimum supply of 1.8 V. Also, the SVSH block in the FR4xx is highly simplified. It is on by default at power up and stays on. It can trigger a BOR reset when the supply falls below the SVS level. It can be turned off in LPM3, LPM4, and LPMx.5 modes by setting SVSHE = 0, if required.

7.1.3 VREF

Unlike REF_A in FR59xx, the FR4xx includes a VREF generation block and a high-accuracy bandgap in the PMM module designed for low-power applications. Two voltage references are generated for internal use and external use (1.2-V VREF) (see Figure 2).

In the FR235x, FR215x, FR267x and FR247x, the shared reference VREF is connected to the ADC module and can be used as a reference voltage for the ADC. It is also internally connected to the ADC channel 13. This makes a possible to monitor the DVCC voltage by using ADC sampling 1.5-V, 2.0-V, or 2.5-V VREF (with DVCC as the ADC reference) without the support of any external components. For detailed information, see the sections *Power Management Module (PMM)* and *On-Chip Reference Voltages* in the device-specific data sheet.

The low-power reference 1.2-V VREF can be used as input to eCOMP.

The low-power reference 1.2-V VREF can be buffered and output to a pin when the ADC channel on that pin is selected as the function. For which pin the 1.2-V can be output to, see the device-specific data sheet. The 1.2-V VREF has only 1-mA drive capability (see Figure 2). For more detailed information, see the PMM and ADC chapters in the MSP430FR4xx and MSP430FR2xx family user's guide.

In FR59xx, the internal shared VREF voltages can be output through an external pin. In FR59xx, the internal shared VREF voltages are different from FR4xx. The FR59xx does not support a low-power 1.2-V VREF like FR4xx supports.

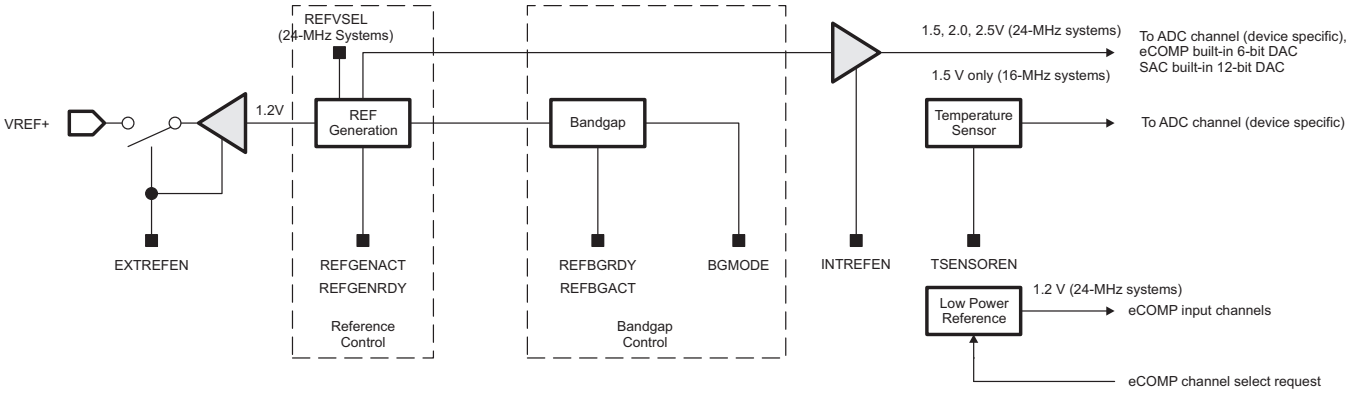

Figure 2. FR4xx Internal Reference Block Diagram

7.2 Clock System

7.2.1 DCO Frequencies

Unlike the FR59xx Clock System (CS), which uses an internal digitally controlled oscillator (DCO) to provide precalibrated frequencies (the fixed frequency points), the FR4xx clock system (CS) uses an internal digitally controlled oscillator (DCO) plus a frequency-locked loop (FLL) to provide frequencies.

A significant difference in the FR4xx DCO with FLL is that it can be configured only to the factory-provided frequencies and does not provide the in-between frequency steps that are available on the FR59xx DCO.

If an in-between frequency is necessary when using an FR4xx MCU, there is a workaround to implement it using the DCOFTRIMEN and DCOFTRIM bits in user code.

The FR4xx devices provide all of the same clock source options and system clocks as the FR59xx family. However the clock distribution system is simplified. For example, SMCLK is always derived from MCLK. There is a SMCLK divider (DIVS) between MCLK and SMCLK. However, the MCLK divider DIVM also affects SMCLK.

FR59xx clock distribution is more flexible than FR4xx. For example, the VLO can be the ACLK source in FR59xx, but in the FR4xx family this feature is available on only FR235x, FR215x, FR267x, and FR247x devices. It is not available on the rest of the FR4xx devices.

For more detailed information, see the *Clock System* chapter in the MSP430FR4xx and MSP430FR2xx family user's guide. Each FR4xx device can have differences in its clock distribution system (see the clock distribution table in the device-specific data sheet for details).

7.2.2 FLL, REFO, and DCO Tap

Another significant difference in the FR4xx CS module is that it has the frequency-locked loop (FLL) and internal trimmed low-frequency reference oscillator (REFO), which are not integrated in the FR59xx clock system module.

The FLL stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency of FLLREFCLK/n. The FLL reference frequency can be XT1CLK (external crystal plus internal XT1 oscillator), or the internal 32-kHz reference oscillator REFOCLK. The value of n is defined by the FLLREFDIV bits (n = 1, 2, 4, 8, 12, or 16). The default is n = 1. On the devices that support only low frequency on XT1, FLLREFDIV is always read and written as 0 (n = 1).

For applications in which accurate frequency is needed, the FLL should be checked to determine if it is locked or not. The FLL lock status can be detected by reading the FLLUNLOCK bits. When changing clock frequency or changing FLL reference clock, FLL locks again if it is not disabled.

There are two types of DCO trim values. If the DCO range is selected as the maximum valid value, the DCO factory trim (default) value is applied. If the DCO range is any value other that the maximum valid value, the DCO software trim process is needed. Otherwise, the FLLUNLOCK bit might always be 1. In the DCO software trim process, DCOFTRIMEN and DCOFTRIM are adjusted by software to achieve a suitable DCO trim value, FLLUNLOCK is set to 0, and the FLL is locked. For a detailed description of how to perform software trimming of the DCO, see the DCO section of the clock system chapter in the MSP430FR4xx and MSP430FR2xx family user's guide.

For a detailed guide on how to check the FLL lock status, see the FLL unlock detection section in the MSP430FR4xx and MSP430FR2xx family user's guide. Code examples that show how to set clock frequency and check the FLL lock status are available in the device-specific product folders on www.ti.com.

Nine of the integrator bits (CSCTL0 bits 8 to 0) set the DCO frequency tap. The nine DCOx bits divide the DCO range selected by the DCORSEL bits into 512 frequency steps, separated by approximately 0.1% (FR59xx supports 8 fixed trimmed DCO frequencies selectable on DCOFSEL. CSCTL1). One benefit from the nine DCOx bits is that the jitter performance for the DCOCLK is much better. See specific data sheet for detailed specification.

The modulator mixes two adjacent DCO frequencies to produce fractional taps. When FLL operation is enabled, the modulator settings and DCOx are controlled by the FLL hardware. When FLL operation is not desired, the modulator settings and DCOx control can be configured with software.

The DCO modulator is disabled when DISMOD is set. When the DCO modulator is disabled, the DCOCLK is adjusted to the DCO tap selected by the DCOx bits.

7.2.3 FRAM Access at 16 MHz and 24 MHz and Clocks-on-Demand

While most FR4xx devices can source MCLK at a maximum frequency of 16 MHz, the FR235x and FR215x devices can source MCLK at 24 MHz. FRAM access is limited to 8 MHz by the FRAM controller, and wait states are required when MCLK is greater than 8 MHz. For configuring wait states, see Section 3.4. Code execution from RAM and accesses to peripherals can be carried out at 16 MHz.

The clock system on FR4xx and FR59xx devices supports the 'clocks-on-demand' feature. This feature allows the LPM settings to be overridden by a clock request. As long as there is an active request for a clock from a peripheral, the clock remains on, regardless of the LPM setting. It is left to the user to disable any modules that request the clock source and prevent the device from entering the required LPM. As an option, this feature can be disabled using the Clock System Control 8 (CSCTL8) in FR4xx device and Clock System Control 6 (CSCTL6) in FR59xx devices. Hence, FR4xx devices can achieve the same outstanding low-power performance on the clock system.

Table 6 lists important differences between the clock systems.

Table 6. Comparison of FR4xx and F59xx Clock Systems

Parameter or Feature	FR4xx	FR59xx
Maximum system frequency	24 MHz	16 MHz
XT1 oscillator	Supports LF or LF and HF modes(1)	Supports only LF mode
XT2 oscillator	Not available	Supports up to 24 MHz
DCO range	Factory-provided frequencies only with software trimming	Calibrated frequencies only
FLL	Available	Not available
REFO	Available/Low power mode	Not available
LFMODCLK (MODOSC/128)	Not available	Available
VLO control	Available with VLOAUTOOFF.CSCTL5	Available with VLOOFF.CSCTL4
Production calibrated frequencies	None	1 MHz, 2.66 MHz, 3.5 MHz, 4 MHz, 5.3 MHz, 7 MHz, 8 MHz, 16 MHz, 21 MHz, and 24 MHz
Clock sources for MCLK	DCOCLKDIV, XT1CLK, REFOCLK, VLOCLK	HFXTCLK, LFXTCLK, VLOCLK, LFMODCLK, DCOCLK, MODCLK
Clock sources for SMCLK	MCLK	HFXTCLK, LFXTCLK, VLOCLK, LFMODCLK, DCOCLK, MODCLK
Clock sources for ACLK	XT1CLK, REFOCLK, VLO (supported in the enhanced clock system devices including FR235x, FR215x, FR267x, and FR247x)	LFXTCLK, VLOCLK, LFMODCLK (MODOSC/128)
External crystal fail-safe operations	XT1 LF: defaults to REFOCLK,XT1, HF: defaults to DCOCLKDIV	XT1 LF: defaults to LFMODCLKXT2, HF: defaults to MODOSC
Registers	CSCTL0 to CSCTL8	CSCTL0 to CSCTL6
DCO bits	9	Fixed
Internal load capacitors for XT1 oscillator	Not available	Not available

(1) Some FR4xx MCUs support XT1 HF mode. See the device-specific data sheet for details.

7.3 Operating Modes, Wakeup, and Reset

Table 7 compares the operating modes that are available and the wake-up times from LPMs.

Table 7. Comparison of Operating Modes and Wake-up Times

Parameter or Feature	FR4xx	FR59xx
LPM0, LPM1, LPM2, LPM3, LPM4	Available except LPM1 and LPM2	Available
LPM3.5, LPM4.5	Available	Available
Wake-up time from LPM0	$0.2 + 2.5 / f_{DCO} \approx 2.7$ µs (f_{DCO} = 1 MHz) (max)	$1.5 \times f_{DCO} \approx 1.5$ µs (f_{DCO} = 1 MHz)
Wake-up time from LPM1 or LPM2	Not applicable	6 µs
Wake-up time from LPM3 or LPM4	10 µs	7 µs
Wake-up time from LPM3.5	350 µs	250 µs
Wake-up time from LPM4.5	350 µs (SVSHE = 1) 1 ms (SVSHE = 0)	250 µs (SVSHE = 1) 1 ms (SVSHE = 0)
Wake-up time from BOR event	1 ms	1.5 ms (max)

The code flow for entry into and exit out of low-power modes LPM0 to LPM4 remains the same in the

FR4xx family as in the FR59xx family. There are differences in functionality between the low-power modes on the FR59xx compared to the FR4xx devices. These differences are described in the *SYS* chapter of the MSP430FR4xx and MSP430FR2xx family user's guide.

7.3.1 LPMx.5

The LPM3.5 and LPM4.5 low-power modes are supported in both FR4xx family and FR59xx family. In both modes, the VCORE LDO is turned off, which powers down the digital core, RAM, and peripherals. To wake up from LPM3.5, RTC interrupts, LCD interrupts, oscillator fault, or port interrupts are required. All other system interrupts are not available. The RTC module and LCD module on the FR4xx device are powered from the LPM3.5 LDO rail and can, therefore, stay functional even when the core LDO is turned off. In LPM4.5, only port interrupts can be used to wake up the device.

It is important to understand that the LPMx.5 modes are inherently different from the typical LPMs (LPM0 through LPM4) in that a wakeup from these modes constitutes a device reset. Because RAM is not retained (except backup memory and LCD memory in LPM3.5), the state of the application (if stored in variables located in RAM) and register initialization are lost.

LPM3.5 is different from LPM4.5 for entering low-power mode and RAM retention.

- The register setting is the same for entering LPM3.5 and LPM4.5. If the RTC or LCD is active, the FR4xx enters LPM3.5. If the RTC and LCD are off, the FR4xx enters LPM4.5. Power supply current can be checked to know the current FR4xx power mode.
- In LPM3.5, backup memory (32 bytes) and LCD memory (40 bytes) are retained (some device in FR4xx has backup memory and LCD memory). If there is requirement in application to retain some data after wakeup from LPM3.5, these 72 bytes can be used. In addition, FRAM can also be used for storing data, because FRAM is nonvolatile (see FRAM special features in Section 3.1).

These LPMx.5 modes are suited for applications that spend large amounts of time in 'deep sleep' and where wake-up time is not critical. To decide which power mode is appropriate for the application, the frequency of wakeup needs to be considered, because there is an energy penalty associated with the time spent during wakeup.

7.3.2 Reset

In both FR4xx and FR59xx device, a deeper level of reset such as POR or BOR executes a boot code that is present in protected ROM. This boot code sets up the device and loads calibration settings that are essential to establish device functionality. Because the clock setting in boot code is different, the time to start from a POR or BOR is different between these two families. For details, see the device-specific data sheet.

Both the FR4xx and FR59xx devices can initiate all levels of reset in software. The resets are initiated by setting the PMMSWBOR or PMMSWPOR bit in the PMMCTL0 control register.

7.4 Determining the Cause of Reset

In both the FR4xx and FR59xx devices, all sources of reset are combined into one System Reset Vector (SYSRSTIV) register, and it is not necessary to check multiple registers to determine the cause of reset. This register is useful when debugging and lists all sources from all levels of reset (PUC, POR, and BOR).

7.5 Interrupt Vectors

In the FR4xx family, the FR235x and FR215x devices support the interrupt compare controller (ICC) feature, which is not supported in FR59xx family.

7.6 FRAM and the FRAM Controller

The FR4xx and FR59xx devices have the same FRAM and FRAM Controller. For details on the difference between FRAM and flash, see Migrating from the MSP430F2xx and MSP430G2xx families to the MSP430FR4xx and MSP430FR2xx family.

7.7 RAM Controller (RAMCTL)

FR4xx devices do not have a RAM controller.

In FR59xx, the RAM is partitioned in one to four sectors, depending on the device. See the device-specific data sheet for sector allocation and size. Each sector can be individually powered down in LPM3 and LMP4 to save leakage. Note that data is lost when sectors are powered down in LPM3 and LPM4.

The FR5962, FR5964, FR5992, and FR5994 MCUs have 8KB of SRAM. The SRAM has three sectors. Sector 0 = 2KB, Sector 1 = 2KB, and Sector 2 = 4KB. The 4KB of Sector 2 is shared with the Low-Energy Accelerator (LEA) peripheral when the LEA module is activated. When the LEA module is not activated, Sector 2 SRAM can be used normally. See the device-specific data sheets for more information.

8 Peripheral Considerations

Some of the peripherals in FR4xx and FR59xx are different. Some peripherals are available only in the FR4xx devices, and others are available only in the FR59xx devices. This section describes the peripheral differences and focuses on the FR4xx peripherals.

8.1 Overview of the Peripherals on the FR4xx and FR59xx Families

Table 8 compares the peripherals in the FR4xx and FR59xx families.

Table 8. FR4xx and FR59xx Peripherals

Peripheral	FR4xx	FR59xx
Backup memory	BAKMEM	Not available
Interrupt compare	ICC	Not available
Direct memory access (DMA)	Not available	DMA
Ports	Digital I/O	Digital I/O
	Capacitive touch I/O	Capacitive touch I/O
CapTIvate technology	CapTIvate module	Not available
CRC	CRC	CRC
		CRC32
Watchdog	WDT_A	WDT_A
Timer	Timer_A	Timer_A
	Timer_B	Timer_B
RTC	Real-Time Clock (RTC) Counter	RTC_B
		RTC_C
32-bit hardware multiplier	MPY32	MPY32
LCD	LCD_E	LCD_C
Communication module	eUSCI	eUSCI
AES	Not available	AES256
Low-energy accelerator	Not available	LEA
Internal reference	In PMM	REF_A
Comparator	eCOMP	COMP_E
Operational amplifiers	TIA	Specified use in USS
	SAC_L1 to SAC_L3	
DAC	SAC_L3	Specified use in USS
ADC	ADC (can be configured to 8 bit, 10 bit, or 12 bit)	ADC12_B
Ultrasonic sensing solution (USS)	Not available	USS including UUPS, HPPLL, SDHS
		USS_A including UUPS, SAPH_A, SDHS
Metering test interface	Not available	MTIF
Extended scan interface	Not available	ESI

8.2 Ports

8.2.1 Digital Input/Output

The main differences in the FR4xx general-purpose I/O (GPIO) pins are:

- P1 and P2 ports support interrupt inputs in the FR4xx devices, the same as in the FR59xx devices. In MSP430FR231x devices, P2.2, P2.3, P2.4, and P2.5 do not support interrupts. In FR211x devices, P1.4, P1.5, P1.6, and P1.7 do not support interrupts. In FR235x and FR215x devices, P1, P2, P3, and P4 ports support interrupt. In FR267x and FR247x devices, all GPIOs including P1, P2, P3, P4, P5, and P6 support interrupts. As the comparison, P1, P2, P3, and P4 ports support interrupt in FR59xx family
- Peripheral function select in the FR413x and FR203x devices uses one register for Port x function selection: PxSEL0. Other FR4xx devices use two registers for Port x function selection: PxSEL0 and PxSEL1. FR59xx devices also use Port x Function Selection Register 0 (PxSEL0) and Port x Function Selection Register 1 (PxSEL1). See the device-specific data sheet for details.
- In the FR4xx and FR59xx families, the high-impedance leakage current is ±20 nA
- Configuration of digital I/O after BOR reset

  In the FR4xx and FR59xx families, to prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, first configure the ports, and then clear the LOCKLPM5 bit.
- Configuration for LPMx.5 power modes

  During LPMx.5 the I/O pin states are held and locked based on the settings before entry to LPMx.5, regardless of the default I/O register settings. Note that only the pin conditions are retained. All port configuration register settings such as PxDIR, PxREN, PxOUT, PxIES, and PxIE contents are lost and must be reconfigured after exit from LPMx.5. After wake from LPMx.5, the LOCKLPM5 bit can be cleared to release I/O pin conditions and I/O interrupt configuration. For details, see the *Configuration for LPMx.5 Low-Power Modes* section in the *Digital I/O* chapter of the MSP430FR4xx and MSP430FR2xx family user's guide.
- Configuration of unused port pins

  To prevent a floating input and to reduce power consumption, unused I/O pins should be configured as I/O function, output direction, and left unconnected on the PCB. Alternatively, the integrated pullup or pulldown resistor can be enabled by setting the PxREN bit of the unused pin to prevent a floating input.
- Configuration of unbonded pins

  In the FR413x and FR203x MCUs, some pins are not bonded out in packages with fewer pins than the 64-pin PM package. Configure these unbonded pins as unused port pins.

8.2.2 Capacitive Touch I/O

In the FR4xx family, some MCUs do not have the capacitive touch feature shared on GPIO pins. See the device-specific data sheet for details.

8.3 Communication Modules

Both FR4xx and FR59xx families have the eUSCI module. Table 9 compares the features of the eUSCI on the two families.

Table 9. Comparison of eUSCI Modules on FR4xx and FR59xx

Parameter or Feature	eUSCI (FR4xx)	eUSCI (FR59xx)
UART		
Enhanced baud rate generation	Yes	Yes
TXEPT interrupt (similar to USART)	Yes	Yes
Start edge interrupt	Yes	Yes
Selectable glitch filter	Yes	Yes
Interrupt vector generator	Yes	Yes
SPI		
Enhanced baud rate generation	Yes	Yes
Maximum baud rate	5 MHz(1)	7 MHz(2)
Interrupt vector generator	Yes	Yes
I^2C		
Preload of transmit buffer	Yes	Yes
Clock low timeout	Yes	Yes
Byte counter	Yes	Yes
Multiple slave addressing	Yes	Yes
Address bit mask	Yes	Yes
Hardware clear of interrupt flags	Yes	Yes
Interrupt vector generator	Yes	Yes

(1) Calculated based on SPI timing with another MSP430FR4133 device in slave mode. For the formula to calculate the maximum baud rate, see device-specific data sheet.
(2) Calculated based on SPI timing with another MSP430FR5969 device in slave mode. For the formula to calculate the maximum baud rate, see device-specific data sheet.

The eUSCI_A module provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA. The eUSCI_B module provides support for SPI (3 or 4 pin) and I^2C.

The eUSCI module in most FR4xx devices (except for the FR231x, FR235x, FR215x, FR267x, and FR247x) does not support ACLK for the clock source. If the eUSCI clock source does not support ACLK, the eUSCI cannot work in LPM3 mode. See the clock distribution table in the device-specific data sheet for details. A workaround to allow UART or I^2C to work in LPM3 mode is to route the ACLK output to the UCA0CLK or UCB0CLK pin externally. This workaround costs two GPIO pins, and it is available only with packages that include an output for the ACLK signal. The clock distribution in the FR231x, FR235x, FR215x, FR267x, and FR247x devices makes ACLK available for the eUSCI module.

The FR4xx devices have eUSCI_A and eUSCI_B modules. See the device-specific data sheet for the number of instances of each module. Table 10 summarizes the pin configurations for the communication interfaces.

In FR231x devices, a pin remapping function is available for eUSCI_B0. The USCIBRMP bit in SYSCFG2 register controls eUSCI_B0 pins remapping from P1.0 to P1.3 to P2.2 to P2.5. Only one port can be selected and valid at one time.

In MSP430 FR21xx and FR2000 devices, the pin remapping functions are available for eUSCI_A and Timer_B. The USCIARMP bit in the SYSCFG3 register controls eUSCI_A pin remapping from P1.4 to P1.7 to P1.0 to P1.3. The TBRMP bit in the SYSCFG3 register controls Timer_B output pin remapping from P1.6 to P1.7 to P2.0 to P2.1. Only one port can be selected and valid at one time.

Table 10. FR4xx eUSCI Pin Configurations

eUSCI_A0	**Pin of FR413x or FR203x**	**Pin of FR2433, FR263x, or FR253x**	**Pin of FR231x**	**Pin of FR21xx or FR2000**	**Pin of FR235x or FR215x**	**Pin of FR267x or FR247x**	**UART**	**SPI**
	P1.0	P1.4	P1.7	P1.7, P1.3	P1.7	P1.4[1], P5.2[2]	TXD	SIMO
	P1.1	P1.5	P1.6	P1.6, P1.2	P1.6	P1.5[1], P5.1[2]	RXD	SOMI
	P1.2	P1.6	P1.5	P1.5, P1.1	P1.5	P1.6[1], P5.0[2]	–	SCLK
	P1.3	P1.7	P1.4	P1.4, P1.0	P1.4	P1.7[1], P4.7[2]	–	STE
eUSCI_A1	**Pin of FR413x or FR203x**	**Pin of FR2433, FR263x, or FR253x**	**Pin of FR231x**	**Pin of FR21xx or FR2000**	**Pin of FR235x or FR215x**	**Pin of FR267x or FR247x**	**UART**	**SPI**
	Not available	P2.6	Not available	Not available	P4.3	P2.6	TXD	SIMO
		P2.5			P4.2	P2.5	RXD	SOMI
		P2.4			P4.1	P2.4	–	SCLK
		P3.1			P4.0	P3.1	–	STE
eUSCI_B0	**Pin of FR413x or FR203x**	**Pin of FR2433, FR263x, or FR253x**	**Pin of FR231x**	**Pin of FR21xx or FR2000**	**Pin of FR235x or FR215x**	**Pin of FR267x or FR247x**	**I²C**	**SPI**
	P5.0	P1.0	P1.0, P2.2	Not available	P1.0	P1.0[1], P5.6[2]	–	STE
	P5.1	P1.1	P1.1, P2.3		P1.1	P1.1[1], P5.5[2]	–	SCLK
	P5.2	P1.2	P1.2, P2.4		P1.2	P1.2[1], P4.6[2]	SDA	SIMO
	P5.3	P1.3	P1.3, P2.5		P1.3	P1.3[1], P4.5[2]	SCL	SOMI
eUSCI_B1	**Pin of FR413x or FR203x**	**Pin of FR2433, FR263x, or FR253x**	**Pin of FR231x**	**Pin of FR21xx or FR2000**	**Pin of FR235x or FR215x**	**Pin of FR267x or FR247x**	**I²C**	**SPI**
	Not available	Not available	Not available	Not available	P4.4	P2.7[1], P5.4[2]	–	STE
					P4.5	P3.5[1], P5.3[2]	–	SCLK
					P4.6	P3.2[1], P4.4[2]	SDA	SIMO
					P4.7	P3.6[1], P4.3[2]	SCL	SOMI

(1) This is the mappable default function that is controlled by the USCIBRMP or USCIARMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.

(2) This is the mappable function that is controlled by the USCIBRMP or USCIARMP bit of the SYSCFG2 or SYCFG3 register. Only one selected port is valid at any time.

8.4 Timer and IR Modulation Logic

Except for the clock source difference described in the following paragraph, there are few differences in the timer modules for the F59xx and FR4xx families. Unlike FR413x and FR203x devices that implement Timer_A, FR231x, FR21xx, FR2000, FR235x, FR215x, FR267x, and FR247x devices implement Timer_B. For the Timer_B in FR231x, FR21xx, FR2000, FR235x, and FR215x, the control bits TBxTRGSEL are added for TBxOUTH trigger source selection. TI recommends stopping the timer before modifying its operation. A delay of at least 1.5 timer clocks is required to resynchronize before restarting the timer if the timer clock source is asynchronous to MCLK.

The VLO is not a clock source for ACLK in FR4xx devices, and VLO cannot be a clock source and capture input for the timer module in FR4xx devices. This is a significant difference for the Timer_A clock source and capture input between FR4xx and FR59xx. Therefore, the VLO cannot be calibrated and used to output accurate pulse as described in Using the VLO library. Because the FR4xx devices have the RTC counter output routed to the timer capture input, there is a workaround to implement the same function in FR4xx devices:

1. Set the VLO as the RTC clock source. The RTC outputs a pulse based on the VLO frequency.
2. Configure the RTC output as the timer capture input.
3. Set the timer clock to ACLK or SMCLK, which provide good accuracy.
4. Measure the VLO frequency with the accurate ACLK or SMCLK.
5. Adjust the RTCMOD register so that an accurate period interrupt can be triggered for the MCU to generate an accurate pulse on a GPIO. See the details in VLO calibration on MSP430FR4xx and MSP430FR2xx family.

New IR modulation logic has been added to the SYS module of the FR4xx family. This logic combines two timers' outputs to easily generate accurately modulated IR waveforms. Both ASK and FSK modulations can be implemented. Two other inputs to this logic are UCA0TXD/UCA0SIMO and the IRDATA bit in the SYSCFG1 register. This makes it possible to generate the modulation data by hardware using eUSCI_A or by software using IRDATA.

For more information, see the infrared modulation function section in the MSP430FR4xx and MSP430FR2xx family user's guide and Infrared remote control implementation with MSP430FR4xx.

8.5 Backup Memory

A Backup Memory module is available in the FR413x, FR203x, FR2433, FR263x, and FR253x devices. The backup memory provides up to 256 bytes that are retained during LPM3.5. The size of the backup memory varies by device (see the device-specific data sheet for details). The backup memory can be used for data storage when LPM3.5 power mode is used in the application. In MSP430FR4xx devices, the LCD memories are also retained during LPM3.5, which can be regarded as the extra backup memory if application needs more memory retained. See Section 7.3.1 for details.

8.6 RTC Counter

The RTC_B or RTC_C module is used in the FR59xx family, depending on the specific device. The real-time clock (RTC) counter module is used in FR4xx devices. The RTC counter is a 16-bit counter that is functional in active mode (AM), LPM0, LPM3, and LPM3.5. The RTC counter accepts multiple clock sources, selected by control register settings, to generate timing from less than 1 µs up to many hours.

One example use of the RTC counter module is for a software calendar. Combined with the LFXT clock and LPM3.5, an ultra-low-power RTC application can be achieved. The base address for the RTC registers is different for FR413x and FR203x devices compared to other FR4xx devices. See the device-specific data sheet for details.

MSP430FR231x, FR21xx, FR2000, FR235x, FR215x, FR267x, and FR247x devices support the control bit RTCCKSEL in the SYSCFG2 register. This bit is not available in other FR4xx devices. The RTCCKSEL bit can select ACLK as the clock source for the RTC.

8.7 LCD

The LCD_E module is supported in the FR4xx family, and the LCD_C module is supported in the FR59xx family. For the detailed design difference on the LCD module, see Designing with MSP430™ MCUs and segment LCDs.

Table 11 summarizes the key difference between LCD_E and LCD_C.

Table 11. LCD_E and LCD_C Comparison

Parameter	LCD_E (FR4xx)	LCD_C (FR59xx)
Supported types of LCDs	Static, 2-, 3-, 4-, 5-, 6-, 7, 8-mux	Static, 2-, 3-, 4-, 5-, 6-, 7, 8-mux
LCD bias modes	1/3 bias	1/2 bias and 1/3 bias
Flexible configuration for COM and Segment pins	Yes	No
LCD clock selection	ACLK, XT1, VLO	ACLK, VLO
Interrupt capabilities	Yes (3 sources)	Yes (4 sources)
Dual memory display	Yes	Yes
Charge pump voltage with external voltage reference	Programmable (15 Levels)	Programmable (15 Levels)
Low-power waveforms mode	Yes	Yes
LCD blinking memory	Yes	Yes
External pins	R13, R23, R33, LCDCAP0, LCDCAP1	R03, R13, R23, R33
LPM3.5	Supported	Not supported
Maximum LCD voltage ($V_{LCD,typ}$)	3.44 V	3.44 V
Number of LCD pins	Up to 4×60 or 8×56	Up to 4×50 or 8×46

8.8 Interrupt Compare Controller (ICC)

In The FR4xx family, FR235x devices support the ICC module. The ICC supports a hardware-based nested interrupt mechanism. The ICC allows all maskable interrupts to be served based on both software configured priority and vector table priority.

The ICC module features include:

- Four-level configurable priority for each maskable interrupt source
- Real-time hardware nested interrupt capability
  - Lower-priority interrupt requests cannot preempt higher-priority interrupts
  - Higher-priority interrupts can preempt lower-priority interrupts
- Reduces design effort to develop a preemptive scheduler or RTOS
- ICC can be enabled and disabled in the control register in the SYS module

8.9 Analog-to-Digital Converters

8.9.1 ADC12_B to ADC

In FR4xx family**,** The ADC module supports fast 10-bit or 12-bit analog-to-digital conversions. The module implements a 10-bit or 12-bit SAR core together with sample select control and a window comparator.

In FR59xx family, The ADC12_B module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, and up to 32 independent conversion-and-control buffers. The conversion-and-control buffer allows up to 32 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

- In FR4xx, up to 10 input channels are available externally and 2 channels available internally. The 1.2-V VREF can be output to a device-specific external channel. The on-chip temperature sensor can be internally connected to channel A12. The 1.5-V VREF can be internally connected to channel A13. For detailed connection, see the analog-to-digital converter (ADC) section in the device-specific data sheet.

- ADC12_B on the FR59xx supports 8 differential and 16 single-ended external inputs. ADC12_B has a dedicated memory control register for each input channel. This allows the user to set unique properties such as voltage reference input and provides a separate memory buffer for each channel of the ADC. For the ADC12_B on the FR59xx, 32 such memory control registers are provided. When a group of channels is sampled, the conversions results are stored sequentially and can be read after all the channels have completed sampling.
- In both ADC and ADC12_B, 8, 10, 12-bit resolution can be set, In ADC module, ADCRES.ADCCTL2 register is used and the default setting is 10-bit. In ADC12_B module, ADC12RES.ADC12CTL2 register is used and the default setting is 12-bit.
- In FR4xx family, the DMA is not supported. In FR59xx family, the DMA is supported in the ADC12_B
- In FR4xx family, an interrupt vector register ADCIV has six interrupt flag sources including three from the window comparator function. As the comparison, all of the ADC12_B interrupts are handled using the ADC12IV.
- On ADC clock source and sampling rate, MODOSC, ACLK, MCLK and SMCLK can be set as ADC clock. The conversion time can be calculated in (resolution-bit+2) × ADCDIV × $1/f_{ADCCLK}$. The sampling time can be set by ADCSHTx.ADCCTL0 to 4, 8, 16,…, or 1024 ADC clock cycles. At the same time, the sampling time should be equal or larger than the min sampling time specified in FR4xx device data sheet. This value is related to the equivalent internal and external resistance and capacitance, resolution, and voltage.
- In the MSP430FR413x and MSP430FR203x devices, the ADC pin selection is set in the SYSCFG2 register. For other FR4xx devices, ADC pin selection is set in the PxSEL0 and PxSEL1 registers.
- Because there is only one pair of power supply pins (DVCC and DVSS) in FR4xx devices, to achieve good ADC performance, board design should avoid system noise:
  - Place decoupling capacitors as close as possible to the DVCC pin.
  - Select reference voltage carefully.
  - Do not layout high-frequency toggled digital signals close to power line or ADC input signals.
  - Do not toggle I/O pins while ADC is working.
  - Find more design guidance for ADC on www.ti.com.

Some register names have been changed and some functions have been simplified. For more information when porting firmware, see the MSP430FR4xx and MSP430FR2xx family user's guide.

8.10 Enhanced Comparator (eCOMP)

Compared to COMP_E in FR59xx, the enhanced comparator (eCOMP) module in the FR4xx, some of the differences are:

- The eCOMP module integrates a 6-bit DAC for reference voltage input. The DAC has a dual-buffer on-chip reference voltage selection. The dual buffer can set different values to have two different DAC output voltages as the eCOMP reference input.
- The eCOMP can function in high-power (high speed) or low-power (low speed) mode according to the power mode selection. This module also has different step hysteresis configurations for better comparison performance.
- There are two interrupt flags in eCOMP, can support dual edge mode (either rising or falling edge can be triggered).
- eCOMP module is available on select FR4xx devices. See device-specific data sheet for details.

8.11 Operational Amplifiers

Two operational amplifiers are available in the MSP430FR231x devices of FR4xx. One op amp is in the Smart Analog Combo (SAC) module, and the other op amp is in the Transimpedance Amplifier (TIA).

The FR231x devices support SAC-L1, which includes only one operational amplifier. Unlike in FR59xx devices, no feedback resistor is included in the MSP430FR231x devices, so external resistors must be added for the amplifier circuit. The SAC supports rail-to-rail input and rail-to-rail output.

The TIA is an amplifier that converts current to voltage. Similar to the SAC-L1, the TIA does not integrate a feedback resistor. One external feedback resistor is needed for the current-to-voltage conversion. TIA supports 1/2- rail input and rail-to-rail output. For the FR231x devices in the PW16 package, there is one dedicated low-leakage input pin for the TIA. This pin supports picoamp-level low-leakage input that improves the accuracy of current conversion.

Unlike in FR59xx devices, FR231x devices have no dedicated analog power or ground pins. If a GPIO needs to drive high current, TI recommends that you do not use the SAC or TIA module at the same time. Using both at the same time affects the power supply of SAC and TIA, which leads to lower performance. For the SAC and TIA layout, keep the traces short and avoid vias. Any toggling pins should be far away from the SAC and TIA pins. The rich internal connections between different modules can also help optimize the layout and reduce pin use. For the internal module connections, see the device-specific data sheet.

8.12 Smart Analog Combo (SAC)

The SAC module has three different configurations from low level to high level: SAC-L1, SAC-L2, and SAC-L3, according to the feature set from minimum to maximum. The FR235x devices support SAC-L3, which support OA (operational amplifier), PGA (programmable gain amplifier), and DAC (digital-to-analog converter)

- OA (operational amplifier)
  - Rail-to rail input
  - Rail-to-rail output
  - Multiple input selection
- PGA (programmable gain amplifier)
  - Configurable modes included buffer mode and PGA mode
  - Programmable PGA gain up to 33x
  - Supports inverting and noninverting mode
- DAC (digital-to-analog converter)
  - 12-bit DAC core
  - Programmable setup time
  - Internal or external reference selection
  - Software selectable data loading

For the details on use of the SAC, see How to use smart analog combo in MSP430 devices.

9 ROM Libraries

FR235x and FR215x devices have the MSP430 driver library and the FFT library in ROM. FR267x and FR247x devices have the MSP430 driver library in ROM. These software libraries are tested to work with the Code Composer Studio™ IDE and IAR Embedded Workbench® IDE toolchains.

- For the ROM image to be compatible between CCS and IAR toolchains, there are certain project properties restrictions. More details are provided in the TI.com attribute guide.
- To use DriverLib in ROM, #include "rom_driverlib.h". Header file checks continue to provide helpful hints at build time until the user application adheres to __cc_rom.
- To use FFTLib in ROM, #include "DSPLib.h". FFTLib is a subset of MSP software library DSPLib.
- For more information, see the MSP430 Driver Library for MSP430FR2xx_4xx ROM README and MSP DSP Library ROM README in MSP430Ware.

The library ROM image is located above the 64KB memory address. Application code using ROM must be large code model (20-bit address pointers rather than 16-bit address pointers).

Benefits of ROM library use:

- Code execution at clock speeds that exceed 8 MHz is faster from ROM than from FRAM. Without FRAM wait states, code execution performance is limited only by the processor clock, which is generally faster than other subsystems. Executing code from RAM gives comparable performance, but the available RAM size is typically more limited.
- More nonvolatile storage (FRAM) available in the device is left for application code.

10 Conclusion

This application report describes many of the key feature changes in the FR4xx family compared to the FR59xx family. This document describes migration from the FR59xx family to the FR4xx family, so the peripherals and features that are supported in the FR59xx family but not supported in the FR4xx family are not included. For the details of a given device, the device-specific data sheet is always the best source of information. For module functionality and use, see the MSP430FR4xx and MSP430FR2xx family user's guide. For any bugs and workarounds in the FR4xx family devices, see the device-specific errata sheet.

11 References

1. MSP430FR4xx and MSP430FR2xx family user's guide
2. MSP430FR58xx, MSP430FR59xx, and MSP430FR6xx family user's guide
3. MSP430FR413x mixed-signal microcontrollers
4. MSP430FR203x mixed-signal microcontrollers
5. MSP430FR2433 mixed-signal microcontroller
6. MSP430FR231x mixed-signal microcontrollers
7. MSP430FR21xx, MSP430FR2000 mixed-signal microcontrollers
8. MSP430FR235x, MSP430FR215x mixed-signal microcontrollers
9. Migrating from the MSP430F2xx and MSP430G2xx families to the MSP430FR4xx and MSP430FR2xx family
10. Maximizing FRAM write speed on the MSP430FR573x
11. Code Composer Studio™ IDE for MSP430™ user's guide
12. MSP430 hardware tools user's guide
13. MSP430 32-kHz crystal oscillators
14. MSP430 FRAM quality and reliability
15. MSPMATHLIB: an optimized MSP430 library of floating-point scalar math functions

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 4, 2018 to March 26, 2019 **Page**

- Added column for "FR267x, FR247x" in Table 1, *F4xx Family Device Comparison* 4
- Added column for FR2676 and changed "Peripherals" and "ROM Library" rows in Table 2, *Comparison of Memory Maps* 5
- Added column for FR2476 in Table 3, *F4xx FRAM Protection Comparison* 7
- Added FR267x and FR247x to the third paragraph in Section 3.5, *Bootloader (BSL)* 7
- Deleted "physical" from "On the FR59xx devices, a physical fuse is used" 8
- Listed the applicable devices in the second paragraph in Section 7.1.3, *VREF* 11
- 11
- Added the paragraph that begins "In FR59xx, the internal shared VREF voltages..." in Section 7.1.3, *VREF* 11
- Updated Section 7.2.1, *DCO Frequencies* 11
- Corrected the list of devices that support MCLK at 24 MHz in Section 7.2.3, *FRAM Access at 16 MHz and 24 MHz and Clocks-on-Demand* 12
- Added FR267x and FR247x to the "Clock sources for ACLK" row in Table 6, *Comparison of FR4xx and F59xx Clock Systems* 13
- Deleted FR231x from the devices that support ICC in Section 7.5, *Interrupt Vectors* 14
- Added DMA row and changed op amp, DAC, and ADC rows in Table 8, *FR4xx and FR59xx Peripherals* 15
- Added FR267x and FR247x to the first list item in Section 8.2.1, *Digital Input/Output* 16
- Added FR267x and FR247x to the paragraph that begins "The eUSCI module in most FR4xx devices..." in Section 8.3, *Communication Modules* 17
- Added the "Pin of FR267x or FR247x" column to Table 10, *FR4xx eUSCI Pin Configurations* 18
- Added FR267x and FR247x in the first paragraph of Section 8.4, *Timer and IR Modulation Logic* 19
- Added FR267x and FR247x to the last paragraph in Section 8.6, *RTC Counter* 19
- Added FR267x and FR247x to the first paragraph in Section 9, *ROM Libraries* 23

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