

# TUSB217-Q1 Configuration Guidelines

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## ABSTRACT

The TUSB217-Q1 is a USB 2.0 high-speed redriver designed to help extend the distance at which a USB host can communicate with a USB device. The TUSB217-Q1 can compensate for both AC loss and DC loss found in signal conditioning environments and can help improve the signal integrity of USB 2.0 high speed traffic.

This application report provides guidelines on how to configure the TUSB217-Q1 to improve or eliminate any signal integrity issues for different signaling environments. These recommendations can be followed when designing with TUSB217-Q1 devices. This application report is intended for developers familiar with a high-speed PCB design and layout. Knowledge of the USB 2.0 protocol is recommended as well.

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## Trademarks

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## 1 Introduction

The TUSB217-Q1 is a USB 2.0 high-speed (HS) signal conditioner, designed to compensate for ISI signal loss in a transmission channel. The TUSB217-Q1 has a third-generation patented design which is agnostic to USB Low Speed (LS) and Full Speed (FS) signals. LS and FS signal characteristics are unaffected by the TUSB217-Q1 while HS signal losses are compensated. The TUSB217-Q1 has both AC boost settings and DC boost settings. Programmable AC boost and DC boost permits compensation for a wide variety of transmission media for USB 2.0 high-speed data. Implementing the TUSB217-Q1 can help pass USB high-speed electrical compliance tests or enable USB communication beyond five meter applications.

## 2 TUSB217-Q1 Features

The TUSB217-Q1 is designed to compensate both AC loss (due to capacitive load) and DC loss (due to resistive loss) in the transmission channel. The TUSB217-Q1 has a patented design that speeds up transition edges of USB 2.0 high-speed signal with an edge booster and increases static levels with a DC boost function.

In addition, the TUSB217-Q1 includes a pre-equalization function to improve the receiver sensitivity and compensate the ISI jitter in application with longer cable length. USB low-speed and full-speed signal characteristics are unaffected by the TUSB217-Q1. The TUSB217-Q1 improves signal quality without altering packet timing or adding propagation delay, making it ideal for applications that require low latency.

The TUSB217-Q1 helps a system to pass the USB 2.0 high-speed electrical near end eye compliance tests with a cable as long as five meters.

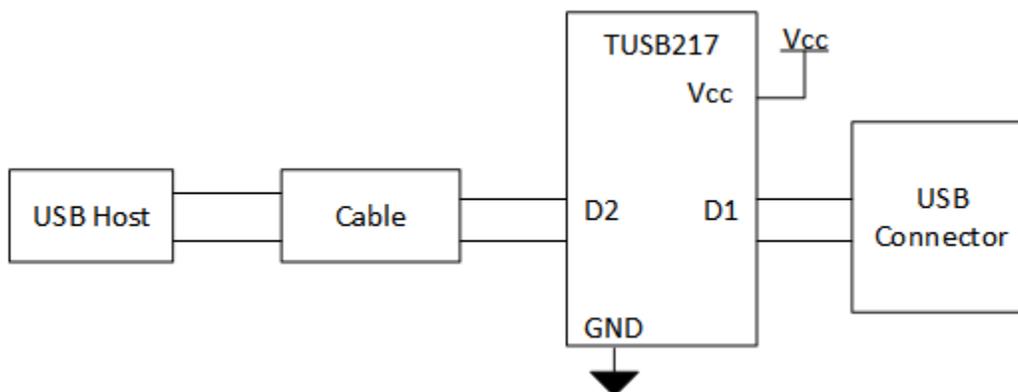


Figure 1. TUSB217-Q1 Typical Application

## 3 General Implementation Guidelines

### 3.1 Selecting TUSB217-Q1 Equalization and Boost Level

The primary purpose of the TUSB217-Q1 is to restore the signal integrity of a USB high-speed channel up to the USB connector. The platform goal is to pass the USB near-end or far-end eye mask with the TUSB217-Q1 in the best location.

Typically, place the TUSB217-Q1 as close to the USB connector on the host platform as possible in order to pass Near-end eye mask testing. To pass Far-end eye Mask testing, place the TUSB217-Q1 toward the middle to your transmission media. This includes systems where the USB connector may be placed at the far-end of an internal cable.

The TUSB217-Q1 can be daisy chained together to help further extend distance from USB Host to USB device. TI recommends only to daisy chain up to three TUSB217-Q1 in a single implementation. Adding an additional TUSB217-Q1 in this way does not guarantee a linear increase in performance and additional considerations need to be taken.

Table 1 and Table 2 show recommendations for the USB high-speed boost settings and receiver sensitivity settings are listed. The configuration for these settings vary, primarily, based on pre-channel length and insertion loss characteristics. Refer to table 5 in the [TUSB217-Q1 USB High Speed Signal Conditioner Data Sheet](#) for recommended resistor values for GPIO mode.

**Table 1. Recommended TUSB217-Q1 GPIO Settings**

BOOST SETTING	RX_SEN SETTING	MAX PRE-CHANNEL LOSS TO PASS (NEAR-END EYE MASK)	ESTIMATED HIGH SPEED INSERTION LOSS (dB) <sup>(1)</sup>
Level 0	Low	6 inches 4 mil FR4 Trace	0.654
Level 0	Low	12 inches 4 mil FR4 Trace	1.191
Level 0	Medium	1 meter 28 AWG	1.571
Level 1	Medium	1.7 meter 28 AWG	1.96
Level 2	Medium	2 meter 28 AWG	2.127
Level 2	High	3 meter 28 AWG	3.01
Level 3	High	5 meter 28 AWG	4.776

<sup>(1)</sup> This column gives insertion loss at 240 MHz or 480 Mbps for USB high-speed traffic.

**Table 2. Recommended TUSB217-Q1 I2C Settings**

EDGE_BOOST SETTING	DC_BOOST SETTING	RX_SEN SETTING	MAX PRE-CHANNEL LOSS TO PASS (NEAR-END EYE MASK)	ESTIMATED HIGH SPEED INSERTION LOSS (dB) <sup>(1)</sup>
0x0	0x0	0x0	6 inches 4 mil FR4 Trace	0.654
0x0	0x0	0x0	12 inches 4 mil FR4 Trace	1.191
0x3	0x2	0x44	1 meter 28 AWG	1.571
0x3	0x2	0x44	1.7 meter 28 AWG	1.96
0x6	0x2	0x44	2 meter 28 AWG	2.127
0x8	0x6	0x77	3 meter 28 AWG	3.01
0xF	0xF	0xFF	5 meter 28 AWG	4.776

<sup>(1)</sup> This column gives insertion loss at 240 MHz or 480 Mbps for USB high-speed traffic.

### 3.2 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp can result in digital circuits not being set correctly. The device must not be enabled until the power on ramp has settled to VCC or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by the microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant must be larger than five times of the power on ramp time (0 to VCC). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

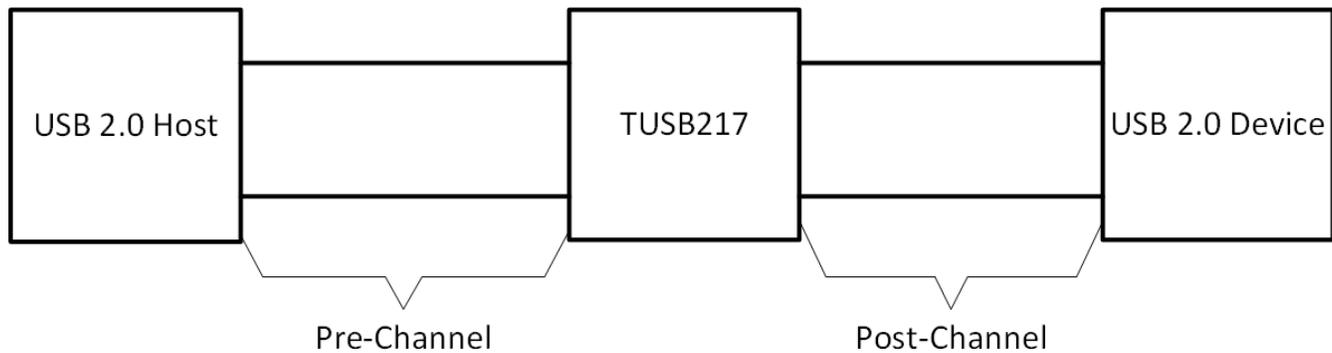
$$CR_{STN} = [Ramp\ Time \times 5] \div [500\ k\Omega] \quad (1)$$

In addition, TI recommends using a ferrite bead with an impedance of 100 Ω at 100 MHz. This ferrite bead must be located between the power supply and bulk capacitance on VCC pin of TUSB217-Q1.

## 4 Frequently Asked Questions

### What is the Pre-Channel and Post-Channel?

The pre-channel is the path the signal takes from the host to the TUSB217-Q1 device. The post-channel is the path the signal takes from the TUSB217-Q1 device to the USB device.



**Figure 2. Pre-Channel and Post-Channel**

### Can D1 and D2 be Swapped?

It does not matter whether D1 or D2 is connected to the host or the device. It does matter that the DP is connected to the data plus and that DM is connected to data minus.

### Does the Thermal Pad Need to be Connected to GND?

No, the thermal pad on the TUS213 and TUSB215 are not connected to anything and do not need to be connected to GND.

### What Are the Near-end and Far-end Eye Masks?

Near-end eye masks are used to test the electrical compliance to the USB protocol for USB receptacles while far end eye masks are used to test the electrical compliance of a USB plug. This means that Near-end eye masks should be used with a eye captured at the USB receptacle. Far-end eye masks should be used to test eye diagram measured after a specific distance of transmission media (i.e. 3 meter cable).

### Why is the TUSB217-Q1 Stuck in High-speed Upon Startup?

Due to the lack of HS negotiation and subsequent enumeration during HOST downstream eye diagram test, the TUSB217-Q1 detects the HOST downstream eye diagram test by detecting high-speed test fixture to get into high speed electrical compliance mode.

Some host or hub downstream ports have been observed to pull down DP/DM low during power up or when it is in the process of initialization. During this time period, while DP/DM is being pulled down by the host, if TUSB217-Q1 is powered on, the TUSB217-Q1 can detect this low bus condition on DP/DM as a test fixture and get into high speed electrical compliance mode.

While in this mode, ENA\_HS remains high even if the device is disconnected or suspend. If ENA\_HS is high, low speed or full speed device can fail to enumerate. RSTN must be low to reset the device and exit compliance mode.

The recommendation at power up is to hold TUSB217-Q1 in reset by holding RSTN low until the host initialization is completed.

## 5 References

- [TUSB217-Q1 USB High Speed Signal Conditioner Data Sheet](#)
- [High-speed Layout Guidelines Application Report](#)

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