Application Report
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# Embedded Scheduler in Cell Battery Monitor of the bq769x0

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**ABSTRACT**

The Scheduler is the most critical digital embedded block inside the cell battery monitor IC, providing the crucial timing frame to the monitor. This application note expands on the parameters detailed in measurement – synchronizing the timing of the ADC modulator schedule during the Coulomb Counting and cell balancing. Understanding the operations of the Scheduler allows the user to implement optimized cell balancing algorithms, polling of the ADC via the host microcontroller.

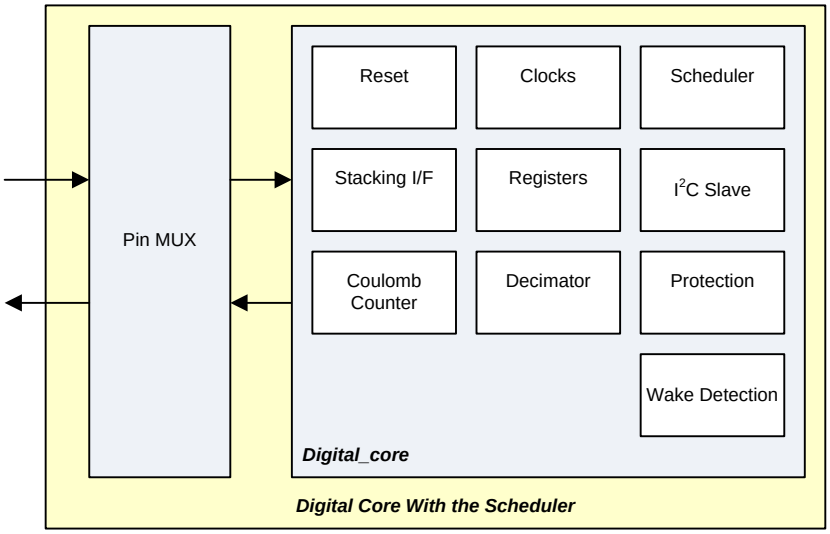


**Figure 1. Embedded Scheduler as Part of the Digital Core**

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## 1 Operations of the Scheduler

The ADC and Coulomb Counter are synchronized in the Scheduler to the 250 ms measurement period. The Scheduler is responsible for controlling the start and stop times of voltage measurements, coulomb counting, cell balancing, and stacked communications. The Scheduler is a state machine that operates on the 12.5 ms time slice from the internally-generated system clock block. The system clock is generated internally and runs at 256 kHz.

The Scheduler initiates a new frame every 250 ms. Every 2 seconds (8 frames), the Scheduler digitizes the temperature measurement information as illustrated in Figure 4. The Scheduler schedules each cell voltage to be measured 12.5 ms during passive balancing and 50 ms when passive balancing is turned off. The Scheduler provides the time slices for 5 voltages measured by the Decimator (VC1-VC5), and up to 10 additional voltages are stored in the register space (VC6-VC15). These voltages are measured in the middle and upper die of a stacked system and relayed to the bottom device via the stacked communications interface.

A fault condition will be detected approximately 0 to 250 ms after the event. For faults detected in the middle and top stacked devices, an additional communications delay is incurred. Cell voltages are transferred from the middle to bottom device and top to middle device once every 125 ms. Therefore, it can take from approximately 0 to 125 ms for a measurement to be transferred to the next lower device. In a 3-stacked system, this can be double for the top device. Finally, the comparison is done only once every 125 ms.

## 2 Scheduler and the ADC System

The *14-Bit ADC System* is represented in Figure 2. The digital block controls the clocks, enables, and select lines to the modulator and analog MUX'es. The modulator bit-stream is attenuated and decimated to produce a 14-bit result.

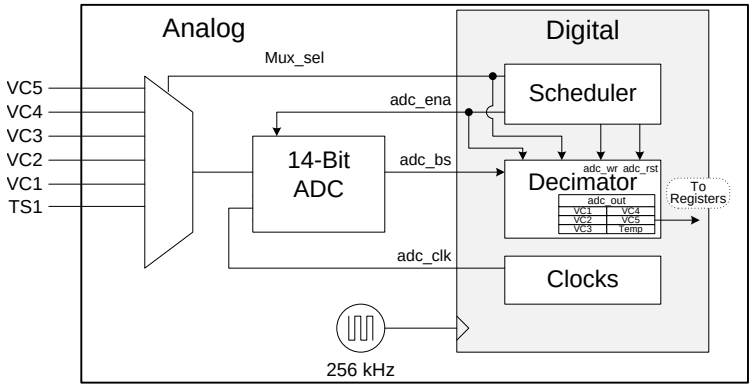


**Figure 2. 14-Bit ADC System**

## 2.1 Cell Balancing OFF

When cell balancing is OFF, each ADC channel is measured over a 50-ms window, as shown in Figure 2. At the beginning of the cycle, the ADC is enabled, the channel MUX is switched, or both occur. The first 500 µs of the cycle allow for settling before decimation begins. Eleven conversions are averaged over the window. At the end of the window, the average is stored as shown in Figure 3.

Measuring of 5 cell voltages is accomplished over one 250-ms period. Eight periods make up a 2-second super period. During the first 250 ms period of the 2-second super period, the cell voltage 5 measurement window is reduced to 37.5 ms and temperature is measured during the excess 12.5 ms. Table 1 shows the schedule during normal mode.

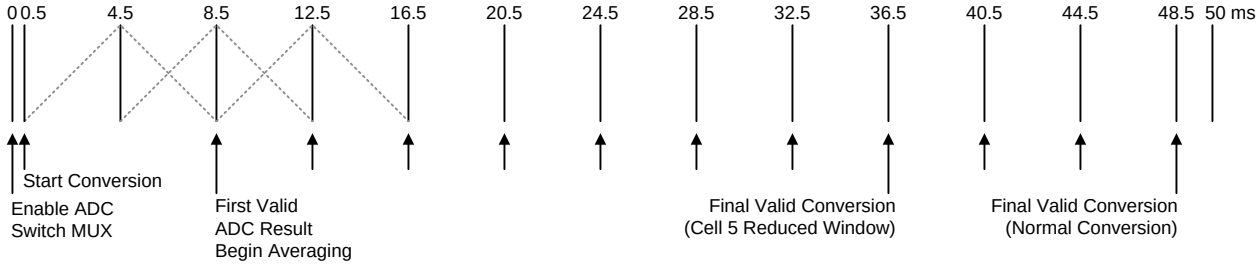


**Figure 3. Scheduler ADC Measurement Window Without Balancing**

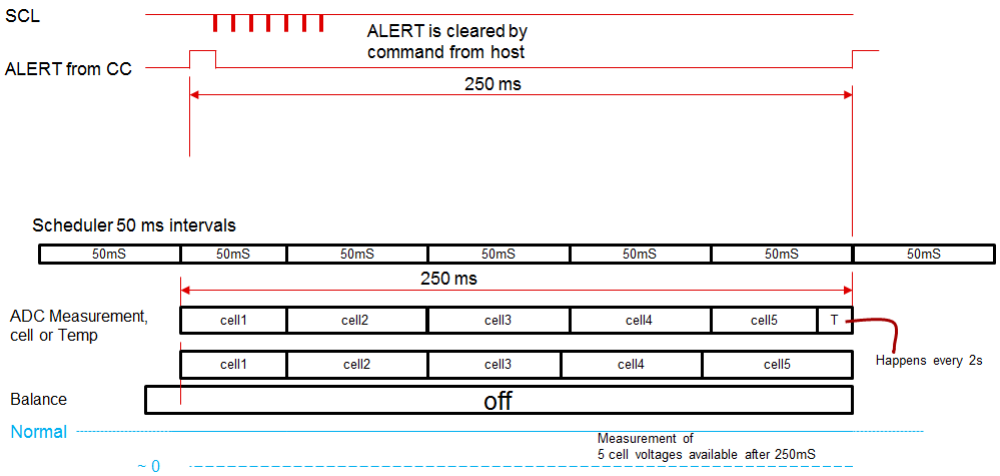


**Figure 4. Scheduler Time Frame Window During Without Balancing**

Table 1 shows the schedule during normal mode.

**Table 1. Scheduling During Normal Mode Without Balancing**

| tick_cnt | time (ms) | Measure | Stack | Volt Comp |
|---|---|---|---|---|
| 0 | 0.0 | VC1 | Start↑ | |
| 1 | 12.5 | ↓ | First stack communication at 0 ms | |
| 2 | 25.0 | ↓ | | |
| 3 | 37.5 | ↓ | | |
| 4 | 50.0 | VC2 | | Start↑ |
| 5 | 62.5 | ↓ | | First OV/UV comparison at 50 ms |
| 6 | 75.0 | ↓ | | |
| 7 | 87.5 | ↓ | | |
| 8 | 100.0 | VC3 | | |
| 9 | 112.5 | ↓ | | |
| 10 | 125.0 | ↓ | Start↑ | |
| 11 | 137.5 | ↓ | | |
| 12 | 150.0 | VC4 | | |
| 13 | 162.5 | ↓ | | |
| 14 | 175.0 | ↓ | | Start↑ |
| 15 | 187.5 | ↓ | | |
| 16 | 200.0 | VC5 | | |
| 17 | 212.5 | ↓ | | |
| 18 | 225.0 | ↓ | | |
| 19 | 237.5 | Temp | | |
| 20 | 250.0 | VC1 | Start↑ | |
| 21 | 262.5 | ↓ | | |
| 22 | 275.0 | ↓ | | |
| 23 | 287.5 | ↓ | | |
| 24 | 300.0 | VC2 | | Start↑ |
| 25 | 312.5 | ↓ | | |
| 26 | 325.0 | ↓ | | |
| 27 | 337.5 | ↓ | | |
| 28 | 350.0 | VC3 | | |
| 29 | 362.5 | ↓ | | |
| 30 | 375.0 | ↓ | Start↑ | |
| 31 | 387.5 | ↓ | | |
| 32 | 400.0 | VC4 | | |
| 33 | 412.5 | ↓ | | |
| 34 | 425.0 | ↓ | | Start↑ |
| 35 | 437.5 | ↓ | | |
| 36 | 450.0 | VC5 | | |
| 37 | 462.5 | ↓ | | |
| 38 | 475.0 | ↓ | | |
| 39 | 487.5 | ↓ | | |
| 40 | 500.0 | | | |

## 2.2 Passive Cell Balancing ON

When passive cell balancing is ON, each cell is measured by ADC for 12.5 ms as well as temperature in the first 250 ms period of the 2 second period. The remaining time is allocated to balancing. The values in the balancing registers are masked during the measurement time.

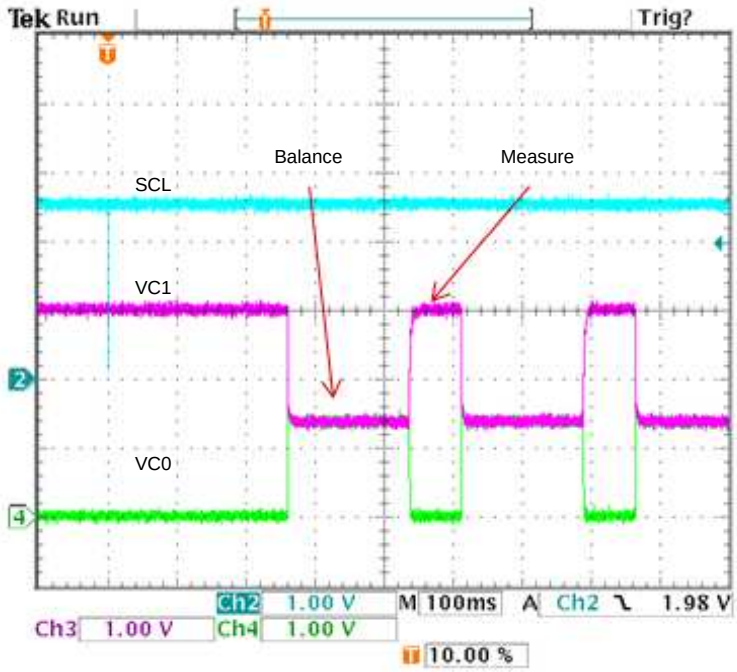


**Figure 5. Scheduler – Balance vs Measure**

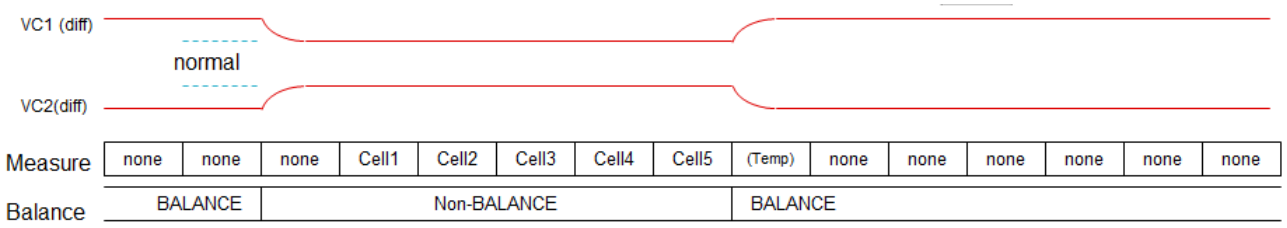


**Figure 6. Passive Cell Balancing of 2 Cells Timing**

When temperature measurements on the TS pin are selected, the thermistor bias is enabled 37.5 ms before the measurement begins and is then disabled after the measurement window is done as shown in Figure 8 and Table 2.

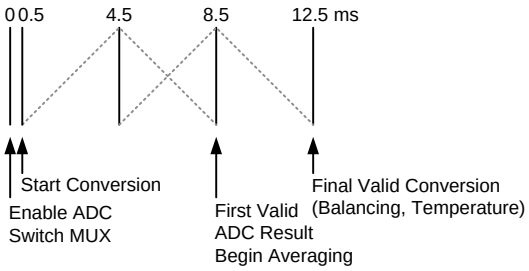


**Figure 7. Scheduler ADC Measurement Window During Balancing**

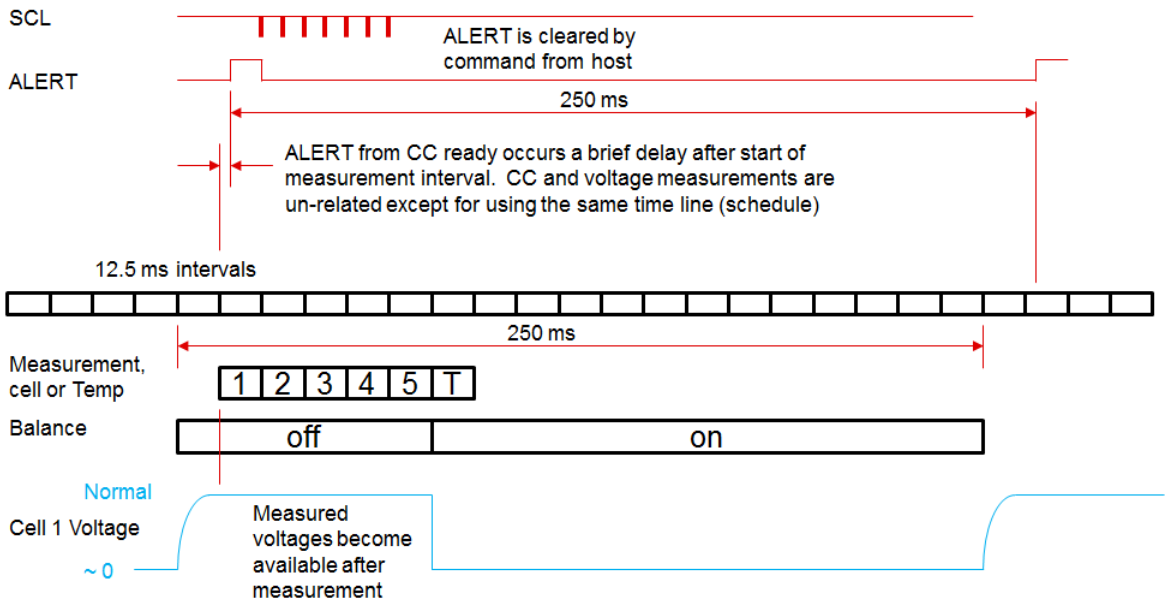


**Figure 8. Scheduler Time Frame Window During Balancing**

Table 2 shows the *Scheduler* for normal mode with passive cell balancing.

**Table 2. Scheduling for Normal Mode With Passive Cell Balancing**

| tick_cnt | time (ms) | Measure | Stack | Volt Comp |
|---|---|---|---|---|
| 0 | 0.0 | VC1 | Start↑ | |
| 1 | 12.5 | VC2 | First stack comms at 0 ms | |
| 2 | 25.0 | VC3 | | |
| 3 | 37.5 | VC4 | | |
| 4 | 50.0 | VC5 | | Start↑ |
| 5 | 62.5 | Temp | | First OV/UV comparison at 50 ms |
| 6 | 75.0 | BAL | | |
| 7 | 87.5 | BAL | | |
| 8 | 100.0 | BAL | | |
| 9 | 112.5 | BAL | | |
| 10 | 125.0 | BAL | Start↑ | |
| 11 | 137.5 | BAL | | |
| 12 | 150.0 | BAL | | |
| 13 | 162.5 | BAL | | |
| 14 | 175.0 | BAL | | Start↑ |
| 15 | 187.5 | BAL | | |
| 16 | 200.0 | BAL | | |
| 17 | 212.5 | BAL | | |
| 18 | 225.0 | BAL | | |
| 19 | 237.5 | BAL | | |
| 20 | 250.0 | VC1 | Start↑ | |
| 21 | 262.5 | VC2 | | |
| 22 | 275.0 | VC3 | | |
| 23 | 287.5 | VC4 | | |
| 24 | 300.0 | VC5 | | Start↑ |
| 25 | 312.5 | BAL | | |
| 26 | 325.0 | BAL | | |
| 27 | 337.5 | BAL | | |
| 28 | 350.0 | BAL | | |
| 29 | 362.5 | BAL | | |
| 30 | 375.0 | BAL | Start↑ | |
| 31 | 387.5 | BAL | | |
| 32 | 400.0 | BAL | | |
| 33 | 412.5 | BAL | | |
| 34 | 425.0 | BAL | | Start↑ |
| 35 | 437.5 | BAL | | |
| 36 | 450.0 | BAL | | |
| 37 | 462.5 | BAL | | |
| 38 | 475.0 | BAL | | |
| 39 | 487.5 | BAL | | |
| 40 | 500.0 | BAL | | |



A 12.5-ms measurement window is also used for all measurements when cell balancing is ON. This is shown in Table 2. When balancing is ON, the excess time in the 250 ms period is used for balancing.

## 3 Scheduler and the Coulomb Counter

Integrating 16-bit Delta-Sigma ADC, also called Coulomb Counter (CC), effectively measures accumulated charges “coulombs” across the sense resistor, using a 250-ms integration window generated by the *Scheduler*. The integration time (250 ms) is equivalent to the time needed for a single read through the decimation filter. The decimator comprises two FIR filters with a window function to generate the coefficients.

The CC integrates the values over a timeframe of 250 ms. After the initial BOOT (and CC_ENABLE being set), the first CC_READY occurs at around 400 ms. The first conversion will contain the integrated values obtained in the “250 ms frame” preceding CC_READY. Prior to the CC_READY flag going up, the CC registers are all cleared to ZEROs. Consecutive conversion of the CC happens at 250-ms intervals.

The Coulomb counting system is shown in Figure 9. The CC is controlled by the *Scheduler* via internal signals: the ‘cc_ena’ and ‘cc_wr’ signals. The ‘cc_ena’ is the general enable signal and gates the clock to the block. When ‘cc_ena’ is high, bit-stream counting commences. When ‘cc_wr’ is pulsed, the current count is stored to the read-only results register and the count is reset. In addition, the ‘cc_ready’ signal is raised. This signal generates an alert status via the Register block and is cleared by the ‘cc_ready_clr’ signal originating from the Register block. The clear signal is initiated by the host processor external to the bqMaximo device.

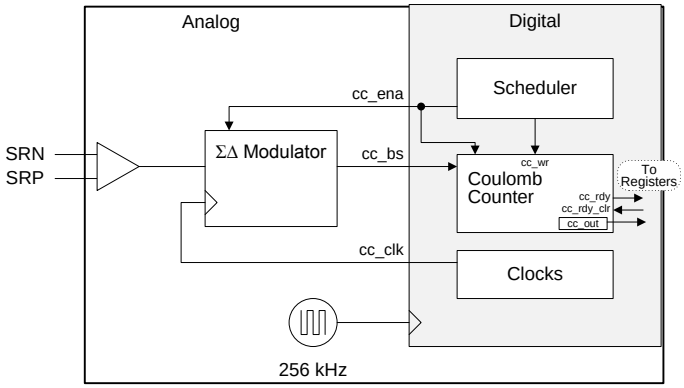


**Figure 9. 16-Bit Delta Sigma Coulomb Counter**

Two counting modes are available. In continuous counting, the scheduler holds ‘cc_ena’ high while ‘cc_wr’ is pulsed every 64000 cycles. In one-shot mode, the *Scheduler* raises ‘cc_ena’ for only a single accumulation period.

The registered count is stored locally in the Coulomb Counter block and is read from either the I2C or stacking interfaces via the Register block. Each time ‘cc_wr’ is pulsed the new result overwrites the previous result. There is no flag to detect this condition: It is the responsibility of the host processor to respond to the ready alert in a timely manner.

The digital block controls the clock and enable to the modulator. The modulator bit-stream is accumulated using a CC filter. The CC maintains a 16-bit signed count which initializes to –32000 (full-scale negative). When the counter is enabled, a bit-stream value of ‘1’ bit causes the counter to increment. A single accumulation period is 64000 cycles (250 ms).

## 4 Scheduler in Stacking Interface

The master functionality in the bottom and middle die is initiated by the *Scheduler* of that device. The *Schedulers* in different devices run independently from each other and are not synchronized to one another.

Internally, up to 3 die can be daisy-chained together as in a multi-chip module (MCM) as depicted in Figure 10. In such a system – stacked MCMs as in bq769030 and bq76940 – the stacking interface is used to communicate control information up the stack (from bottom to the top die) and measurement data and status information flow down the stack (from top to bottom). Two bits in the EEPROM identify whether a device is standalone (non-stacked-bq76920), bottom, middle, or top.

The bottom device acts as a master when communicating with the middle or top device. The middle device acts as a slave when communicating with the bottom device, and as a master when communicating with the top device. The top device always acts as a slave.

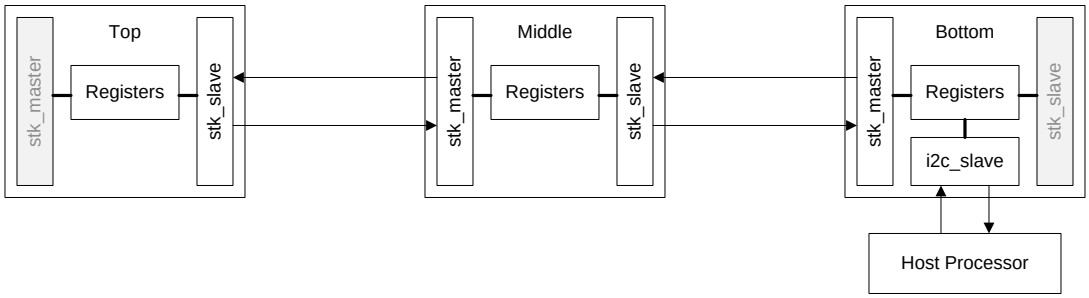


**Figure 10. Stacking Interface**

The bottom device is responsible for testing all 15 voltages for overvoltage and undervoltage (OV / UV) faults. The state machine cycles through all 15 cell voltage registers, comparing each to the OV and UV limits. The ‘ov_detect’ and ‘uv_detect’ signals are cleared at the beginning of the comparison. At the end of the comparison, if any cell voltage reading is above the OV trip threshold, the OV timer is incremented. Likewise, if any cell voltage is below the UV trip threshold and above the UV ignore threshold (approximately 500 mV) ‘uv_detect’ will be set and the UV timer will be incremented. If the detection signal is low, the timer is reset.

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