Application Report
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Improved Thermal Dissipation and Energy Efficiency for Peripheral Driving with TPL7407L

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ABSTRACT

The ULN2003A has long been a popular device used for driving high-current peripheral circuits from microcontroller and control logic output signals. The ULN2003A consists of seven Darlington bipolar transistors which sink current from the output to ground when a high logic signal is placed on the input. Because the ULN2003A is based on bipolar Darlington transistor topology, it dissipates a considerable amount of power even when it sinks small output currents.

The TPL7407L is a new peripheral driver that uses an N-channel MOSFET transistor on the output instead of the bipolar Darlington pair. Because of the NMOS output, the TPL7407L can sink more current to ground while dissipating less power and generating less heat which makes it an overall improved device compared to the ULN2003A. This application note explains how the CMOS technology in the TPL7407L improves power dissipation and thermal performance compared to the ULN2003A, including a 50% reduction in power consumption in typical use cases.

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1 Benefits

The improvements of the TPL7407L over the ULN2003A:

- Improved power efficiency and lower leakage current
- Sink 600 mA / channel on the output
- Maximum input drive across all GPIO ranges (1.8 V–5.0 V)
- Dissipates less than half the power for currents less than 250 mA per channel due to lower V_{OL}
- Wider temperature range, –40°C to 125°C

2 Comparison

Table 1 shows a side-by-side comparison of the ULN2003A and TPL7407L drivers. V_{OL} is the voltage drop from the output pin of the driver to ground. I_L is the current the driver sinks on the output. In the case of the ULN2003A, V_{OL} is the collector-to-emitter voltage, referenced in the datasheet as voltage parameter $V_{CE(sat)}$, and I_L is the collector current per channel, I_C (see Figure 1).

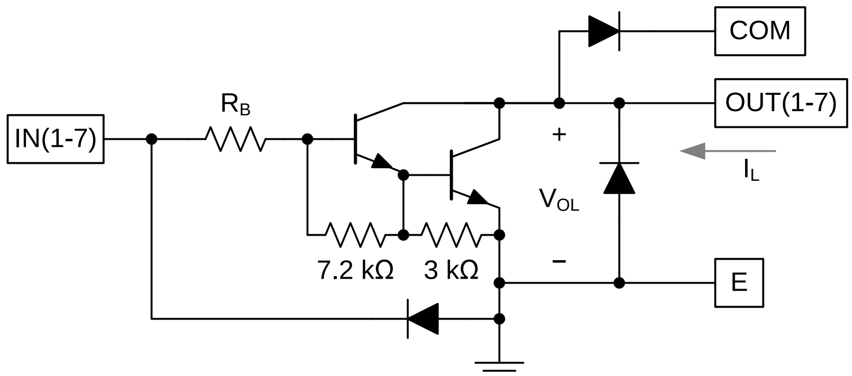

Figure 1. Schematic of Darlington Pair in Each Channel of the ULN2003A

For the TPL7407L, V_{OL} is the drain-to-source voltage referenced in the datasheet as voltage parameter V_{DS}, and I_L is the drain current per channel, I_{DS} (see Figure 2).

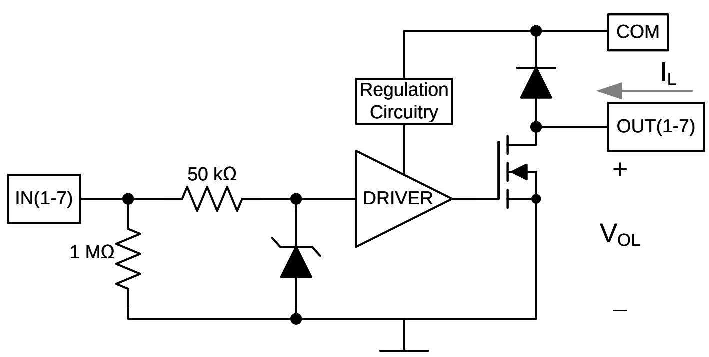

Figure 2. Schematic of NMOS in Each Channel of the TPL7407L

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Table 1. Comparison Between ULN2003A and TPL7407L

	ULN2003A	TPL7407L
Max Output voltage	50 V	40V
V_{OL}	V_{OL} at 100 mA ≥ 0.9 V (typ) V_{OL} at 200 mA ≥ 1 V (typ)	V_{OL} at 100 mA = 0.2 V (typ) V_{OL} at 200 mA = 0.42 V (typ)
Output Off Current (I_{OFF})	100 uA / ch (max)	0.5 µA / ch (max)
Ambient Temperature	–20°C to 70°C (Standard) –40°C to 105°C (I version)	–40°C to 125°C
Max Collector/Drain Current, I_L	500 mA	600 mA

The parameters in Table 1 were taken from the data sheets of both the ULN2003A and the TPL7407L. The table shows improved parameters of the TPL7407L over the ULN2003A such as: operating temperature range, max output current, output voltage, and leakage current.

3 Power Budgeting and Thermal Properties

The key improvement of the TPL7407L over the ULN2003A is the reduced voltage drop from the output pin to ground, V_{OL}. This lower voltage drop means that the TPL7407L will dissipate less power than the ULN2003A for the same amount of load current. Figure 3 shows the output voltage as a function of output load current for both devices for ambient temperatures of 25°C and 70°C. The data used for the following graphs was acquired using the SOIC package of both devices. The graph shows that the TPL7407L has a significantly lower output voltage over temperature than the ULN2003A.

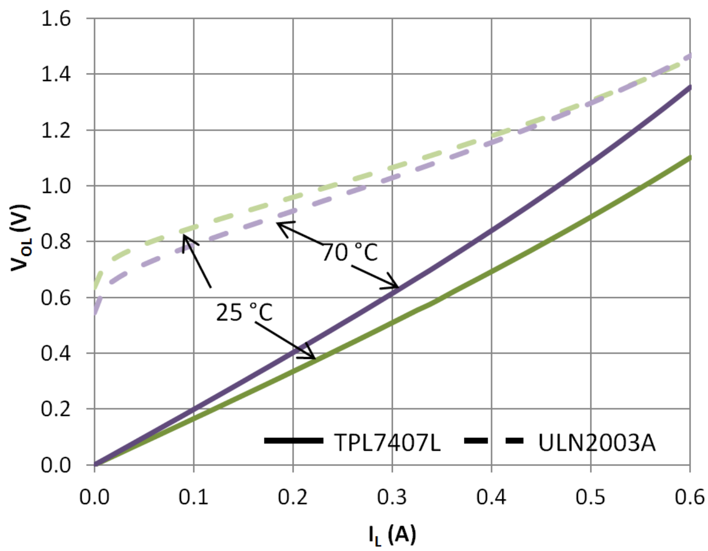

Figure 3. Output Voltage Versus Output Current for TPL7407L and ULN2003A

Figure 3 also shows that the output of the TPL7407L has the characteristics of a resistor. The output voltage is linearly dependent on the load current, according to Ohm’s law. The ULN2003A does not intercept the origin because one of the transistors in the Darlington pair will not saturate.

This zero-intercept operation of the TPL7407L translates to less power dissipated by the chip when compared to the ULN2003A. The power dissipated per channel, $P_{D(CH)}$, is calculated by Equation 1.

$$P_{D(CH)} = V_{OL} I_L \tag{1}$$

Because the output voltage of the TPL7407L is lower over the operating load current range, it will dissipate less power than the ULN2003A. Figure 4 compares the power dissipated by the two devices for a single channel.

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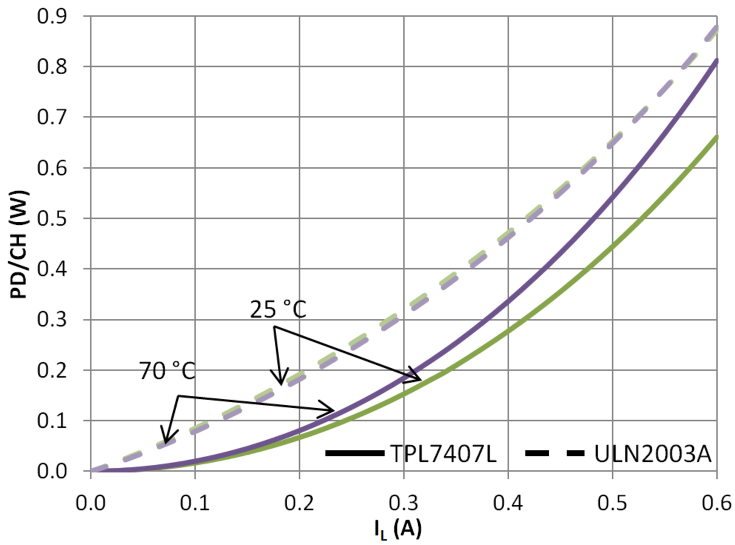

Figure 4. Dissipated Power per Channel Versus Output Current for TPL7407L and ULN2003A

When driving larger current loads, multiple inputs and outputs may be tied together, or paralleled. Figure 5 shows the power dissipation of the two devices for an application where all seven outputs are paralleled to sink current.

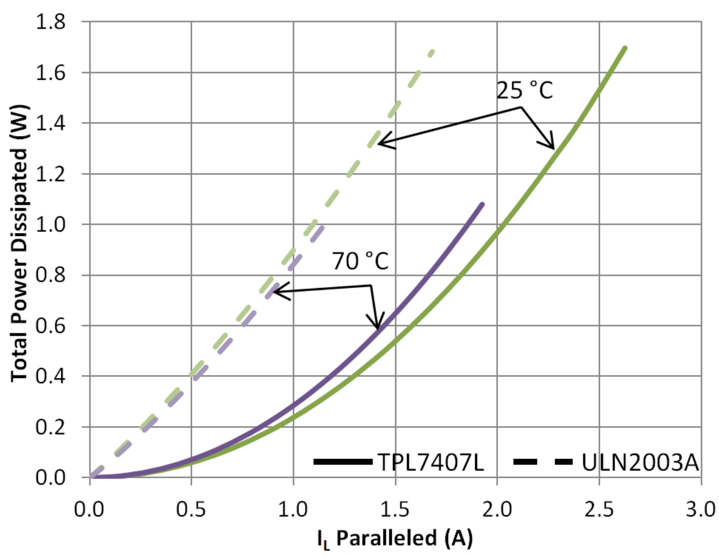

Figure 5. Dissipated Power Versus Seven Paralleled Channel Output Current for TPL7407L and ULN2003A

The plot lines in Figure 5 are limited by the maximum current of each device based on the temperature of operation. As the chip dissipates power, the temperature of the silicon junction, T_J, increases. The absolute maximum junction temperature, $T_{J,MAX}$, that these chips can tolerate is 150°C. Equation 2 shows the relationship between the junction temperature, the ambient temperature, T_A, and the package thermal impedance, θ_{JA}.

$$T_J = \theta_{JA} P_{D(CH)} + T_A \tag{2}$$

When designing with thermal considerations, the temperature rise, ΔT, is calculated (Equation 3) to find the maximum operating ambient temperature of a chip. The temperature rise is the change in temperature that occurs between the silicon junction and the ambient temperature.

$$\Delta T = \theta_{JA} P_{D(CH)} = T_{J,MAX} - T_A \tag{3}$$

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A lower temperature rise means that the chip will generate less heat for the same amount of load current. Figure 6 shows a comparison of the temperature rise for the TPL7407L and ULN2003A. The data used in Figure 6 was obtained by using the data from Figure 5 with Equation 3. Figure 6 is a calculated approximation of the actual operating characteristics. In practice, the chip increases the ambient temperature around it, which changes the operating conditions.

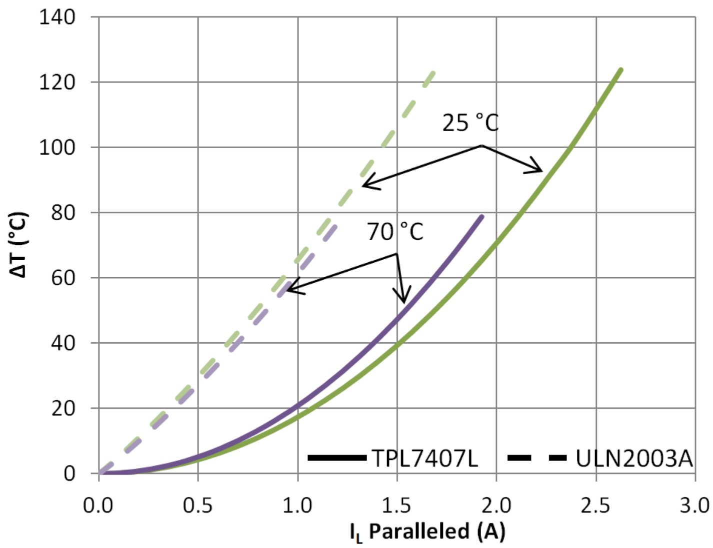

Figure 6. Temperature Rise Versus 7 Paralleled Channel Output Current for TPL7407L and ULN2003A

Although the thermal impedance of the ULN2003A (73°C/W) is lower than the TPL7407L (91.9°C/W), the TPL7407L dissipates such low power by comparison that its temperature rise is lower for the operating range of the ULN2003A. This lower temperature rise means that less heat will be generated by the chip.

4 How to Use More Channels to Improve Power Dissipation

As shown briefly in the previous section, the channels of the TPL7407L may be paralleled to drive loads beyond the single channel maximum current. For example, a 1-A load can be driven by 2 to 7 paralleled channels. The current through each channel is found by Equation 4 where I_T is the total current being sunk through the paralleled channels, $I_{OL/CH}$ is the current which each channel sinks, and N is the number channels used to sink that current.

$$I_{L/CH} = I_T/N \quad (4)$$

When choosing the number of channels to sink a large current, the designer must be conscientious of ambient temperature and power dissipation. One channel on the TPL7407L can sink its maximum specification of 600 mA at 25°C so long as no other channels are sinking current. As more channels sink current, the junction temperature increases, which decreases the individual current capacity of each channel. The datasheet specifies that the TPL7407L can sink 2 A using all the pins. That is a maximum of 286 mA per channel.

However, there are power dissipation benefits for increasing the number of channels used to sink the load current. This is because the output voltage is dependent on the load current of the TPL7407L. Figure 4 shows that as the current through each channel is reduced, the output voltage decreases proportionally.

The total power dissipated by chip, P_T, is dependent on the output voltage, $V_{OL\left(at\ I_{L/CH}\right)}$, at a specific output current, $I_{L/CH}$, as shown in Equation 5.

$$P_T = V_{OL\left(at\ I_{L/CH}\right)} I_T = V_{OL\left(at\ I_{L/CH}\right)} I_{L/CH} N \quad (5)$$

When more channels are used, a less current is sunk by each channel. When less current is sunk through each channel, the total power dissipated by the chip decreases for the same total load current. Table 2 shows a comparison of the total power dissipated by the chip when different numbers of channels are used. The total current sunk by the chip is 1 A at 25°C. The values in the table were calculated from the results shown in Figure 4.

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Table 2. Total Power Dissipation and Number of Channels Used to Sink I_T = 1 A

N	$I_{L/CH(MAX)}$ (mA)	P_T (W) for ULN2003A	P_T (W) for TPL7407L
2	500	1.30	0.899
3	333	1.10	0.568
4	250	1.01	0.422
5	200	0.959	0.335
6	167	0.924	0.278
7	143	0.899	0.238

As Table 2 shows, when the TPL7407L uses only two channels to sink 1 A of current, it dissipates the same power as seven channels of the ULN2003A. Paralleling more channels of the TPL7407L decreases its dissipated power even further below the lowest power dissipated by the ULN2003A. With lower power dissipated by the TPL7407L, more channels may be used to control more peripherals which can reduce the number of chips used per board from two ULN2003A chips to one TPL7407L chip. Another example of this BOM cost reduction can be found in Section 5.

5 Application

The ULN2003A and the TPL7407L are designed to sink large current loads that most logic or control devices cannot normally handle. Inductive devices such as solenoids, relays, and stepper motors require a large current to energize their coils quickly. One such system that uses multiple kinds of inductive devices controlled by a microcontroller is an air-conditioning system. Figure 7 shows a simplified block diagram of an air conditioning system using ULN2003A chips to drive various peripherals. The peripherals considered in this particular system are relays that power a blower motor, and a unipolar stepper motor that controls a valve or external louver.

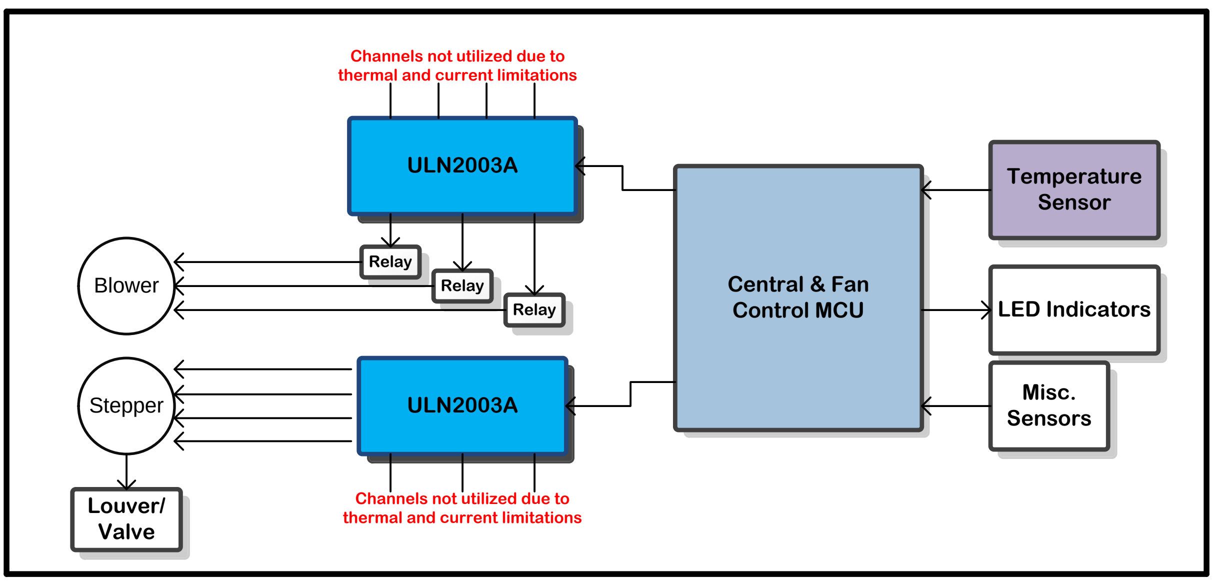

Figure 7. Air Conditioning System Using Two ULN2003A Chips to Drive Peripherals

Typical air-conditioning systems require multiple ULN2003A chips to drive these and other peripherals in their systems. As mentioned in the previous section, when multiple channels are used, the current capacity of each channel decreases because of the heat generated by power dissipation in the chip. As shown in Figure 4, the TPL7407L dissipates much less power than the ULN2003A. Since less power is dissipated, less heat is generated, which allows the current capacity of the TPL7407L to be much larger. With a larger current capacity, two ULN2003A chips may be substituted for one TPL7407L (Figure 8).

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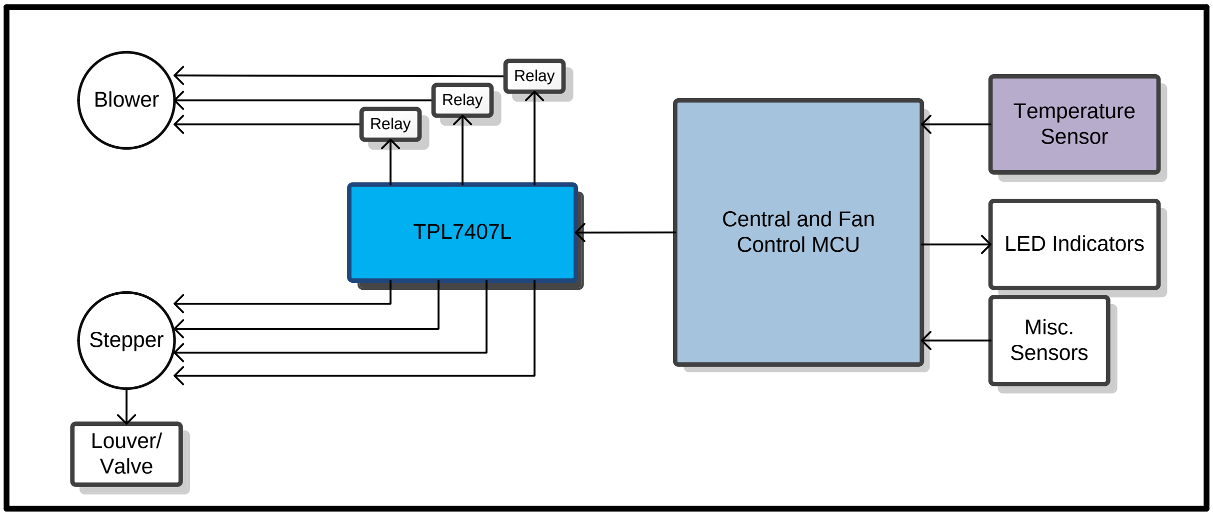

Figure 8. Air-Conditioning System Using One TPL7407L Chip to Drive Peripherals

When one TPL7407L is used in place of two ULN2003A chips, less heat is generated by the overall circuit. This is important, especially for designs that experience a wide range of temperatures. Other advantages of using one TPL7407L chip include: reduced BOM cost, less leakage/standby-current, and less circuit board space required.

6 Power Supply Recommendations

The COM pin is the power supply pin of this device to power the gate drive circuitry. This ensures full drive potential with any GPIO above 1.5 V. The gate-drive circuitry is based on low voltage CMOS transistors that can only handle a max gate voltage of 7 V. An integrated LDO reduces the COM voltage of 8.5 V to 40 V to a regulated voltage of 7 V. Though 8.5 V minimum is recommended for V_{com}, the part will still function with a reduced COM voltage with a reduced gate drive voltage and a resulting higher R_{dson}.

To prevent overvoltage on the internal LDO output due to a line transient on the COM pin, the COM pin must be limited to below 3.5 V/µs. Faster slew-rate (or hot-plug) may cause damage to the internal gate-driving circuitry due to the LDO's inability to clamp a fast input transient fast enough. Since most modern power supplies are loaded by capacitors > 10 µF, this should not be of any concern. It is recommended to use a bypass capacitor that will limit the slew rate to below 0.5 V/µs.

Figure 9 is a great example where repetitive slew rates may occur on the V_{com} pin. Whenever a Zener diode is used between V_{com} and the motor supply, the V_{com} pin will slew from the coil supply to a voltage that is the sum of the Zener voltage and the coil supply when there is a flyback event. Depending on the coil inductance and resistance, this can be very rapid.

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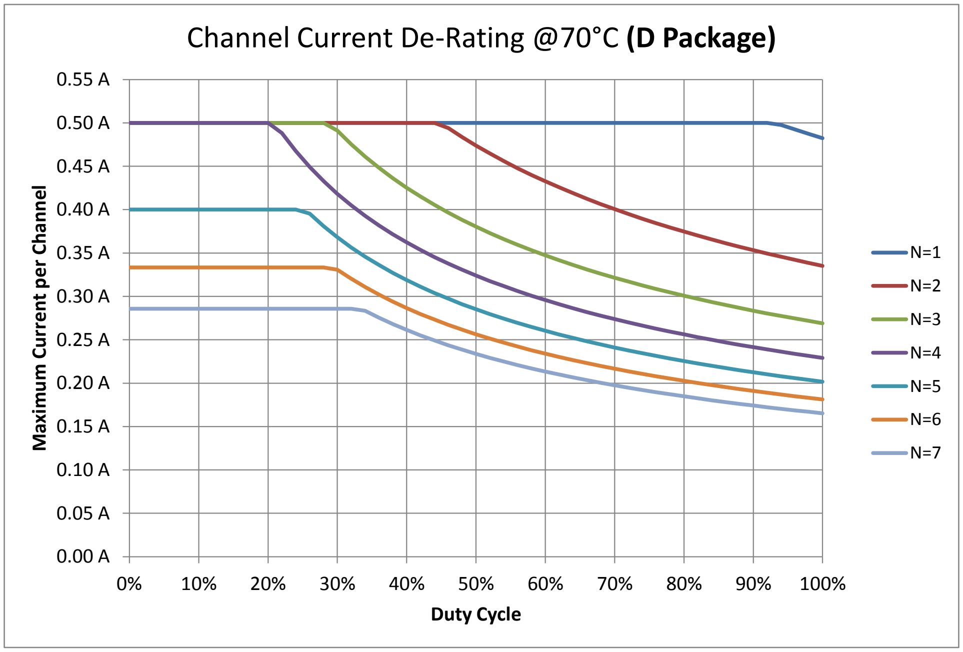

Figure 9. D Package Maximum Collector Current Versus Duty Cycle at 70°C

In summary, whenever the COM pin may experience a slew rate greater than 0.5 V/µs a capacitor must be added to limit the slew to < 0.5 V/µs.

7 Conclusion

The TPL7407L offers many improvements in designs over the ULN2003A. The TPL7407L has lower output voltage, lower power dissipation, less heat generation, and increased output current capability. It is pin-for-pin compatible with the popular ULN2003A and can reduce bill-of-materials costs and board space in high-current peripheral-driving applications.

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