Application Report
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Accuracy-Enhanced Ramp-Generation Design for D-CAP3 Modulation

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ABSTRACT

D-CAP and D-CAP2 control schemes have been widely used in TI Switched-Mode DC-DC converters due to their fast transient response and no off-chip compensation. Offset generated by current sense ramp adds an error to VFB and Vout and hence reduces DC accuracy. This paper introduces a new D-CAP3 control scheme which greatly improves DC accuracy of the converter while maintaining the same fast transient response as D-CAP/D-CAP2. Meanwhile, compact silicon implementation makes the new D-CAP3 control extremely low cost. D-CAP3 control has been implemented in many TI products such as TPS53912, TPS53913, TPS53915, TPS53513, TPS53515, TPS548A20, and TPS548D22. These products are ideal for powering low-voltage processors in rack server, single board computer, and hardware accelerator applications that benefit from a fast transient response time and reduced external component count.

Trademarks

1 Introduction

Switched-Mode DC-DC converter is an important category in Power Supply design. Ideally Switched-Mode DC-DC converter can achieve close to 100% power conversion efficiency, and it has been widely used in all kinds of electronic devices such as computers, cell phones, TVs, and so forth. In a Switched-Mode DC-DC converter, the control loop design is very critical since it determines major performance parameters of the converter such as speed of load transient response, DC accuracy and design cost, which includes die size and number of off-chip components. Different control schemes have been developed during the past few decades to improve these parameters.

Within these control schemes, voltage mode control [1] and current mode control [2] can achieve very good DC accuracy thanks to their high loop gain, but the load transient response can still be improved. Meanwhile, voltage mode and current mode control normally require several off-chip components for loop compensation which increases both design complexity and cost. However, D-CAP [3] and D-CAP2 [4] [5] control schemes can achieve fast load transient response. These two control schemes also remove all off-chip compensation components, thus making the part easier to be used and reducing design cost. With D-CAP and D-CAP2 control schemes, offset generated from current sense ramp creates variations on both VFB and Vout under different application conditions. Meanwhile, the fast but low-gain loop is not intended to correct these variations. It has been really challenging to achieve both fast transient response and high DC accuracy simultaneously while still keeping design cost low.

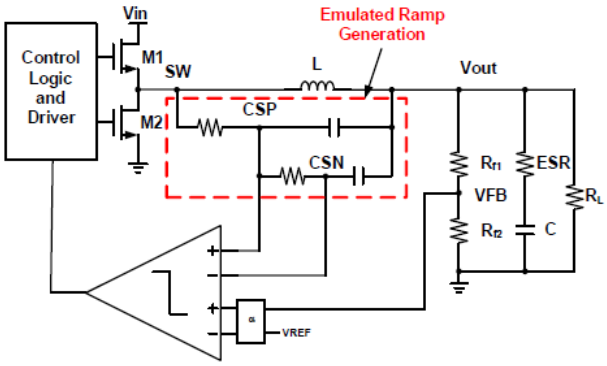

Figure 1. Structure of D-CAP2 control

This paper presents a new D-CAP3 [6] control scheme which greatly improves DC accuracy while maintaining the same fast transient response as D-CAP and D-CAP2. This simple but elegant implementation also makes the design extremely low cost. This paper is organized as follows. Section 2 introduces the structure and operation of D-CAP and D-CAP2 control. Section 3 presents the proposed D-CAP3 control structure, operational principle, and its circuit implementation. Experiment results and discussions are provided in Section 4 and Section 5 respectively.

2 D-CAP and D-CAP2 Control Schemes

2.1 Structure of D-CAP and D-CAP2 Control Schemes

Figure 1 shows the structure of the D-CAP2 control scheme. Vin is the input voltage and Vout is the regulated output voltage. M1 and M2 are the high-side and low-side power transistors, respectively. The Control Logic and Driver block generates pseudo-constant-ON-time pulses based on Vin, Vout, and switching frequency. The loop comparator compares α*VFB+CSP with α*VREF+CSN to initiate these ON pulses whenever needed. The emulated Ramp Generation block is composed of a 2nd order low pass filter. This filter can emulate inductor current and brings inductor current information back to the control loop. D-CAP control is similar to D-CAP2 control except current information is generated through the loading capacitor equivalent series resistor (ESR). Current flowing through the ESR generates voltage ripple across the ESR and thus adds current ripple information to Vout. This ripple will be brought back to the comparator input through the FB pin and make the loop stable. However, D-CAP control is only good for applications with high ESR loading capacitors. For low ESR loading capacitors, such as ceramic capacitors, voltage ripples on Vout and VFB are small and may not be sufficient to make the loop stable. D-CAP2 control is thus needed by adding internal ripple through low pass filter.

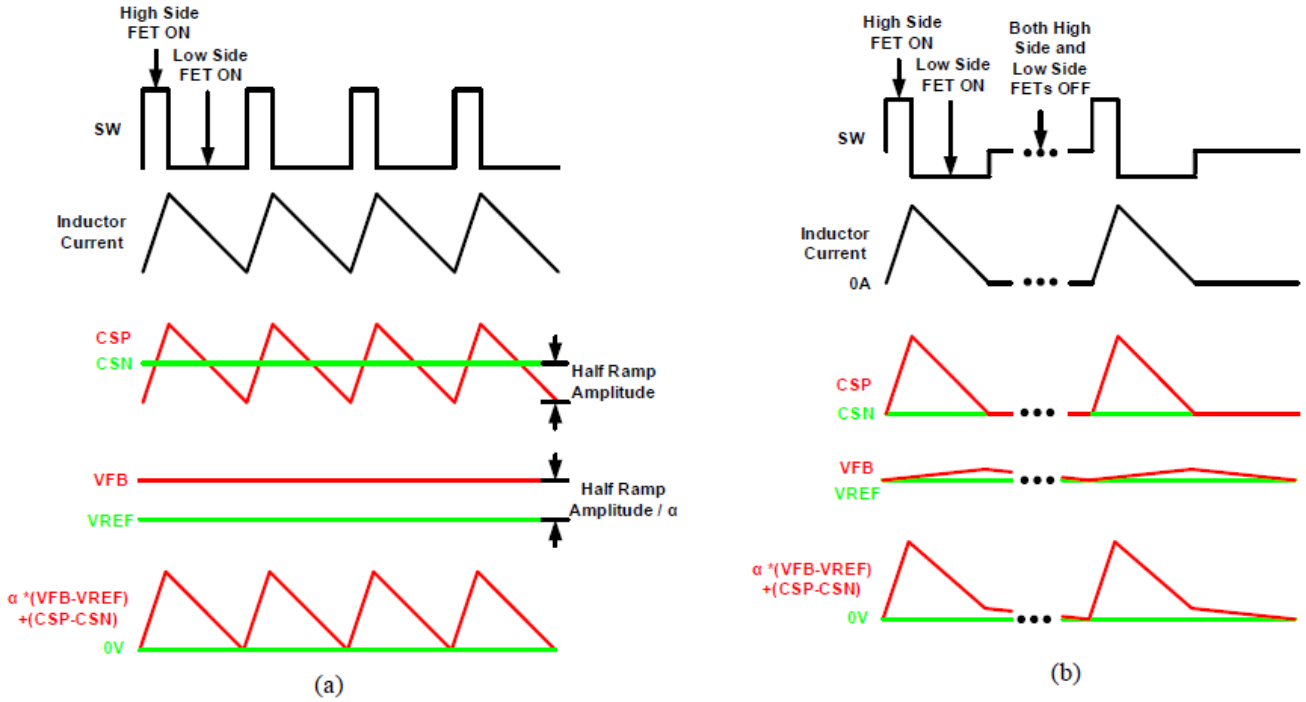

Figure 2. (a) CCM Operation and (b) DCM Operation of D-CAP2 Control

2.2 Operational Principle of D-CAP and D-CAP2 Control Schemes

Figure 2 shows the operational principle of D-CAP2 control. The loop comparator monitors its inputs α*(VFB-VREF)+(CSP-CSN) to generate ON pulses. Whenever the sum of the input voltages becomes lower than 0 V, the comparator output goes low to initiate an ON pulse. The ON pulse width is calculated by the Control Logic and Driver block based on Vin, Vout, and switching frequency settings. During the ON pulse, high-side power transistor M1 is turned on and the SW node is pulled to close to Vin. The inductor current increases to charge Vout. Figure 2 (a) shows the operation of a D-CAP2 converter under Continuous Conduction Mode (CCM) where the inductor current is always higher than 0 A. Since CSN is a filtered version of CSP, it is located at the middle of CSP ripple in CCM. As a result,

$$CSN = CSP\_valley + CSP\_ripple/2 \quad (1)$$

Meanwhile, the turn on condition of the converter is

$$\alpha \times (VFB - VREF) + (CSP - CSN) = 0 \quad (2)$$

This forces

$$\alpha \times (VFB - VREF) = (CSN - CSP\_valley) \quad (3)$$

or

$$VFB - VREF = CSP\_ripple/2\alpha \quad (4)$$

From Equation 4, under CCM operation, feedback voltage VFB is not equal to reference voltage VREF. The offset between reference and feedback voltage is CSP_ripple/2α. This offset will greatly reduce output voltage accuracy since Vout is proportional to VFB and

$$VOUT = VFB \times \frac{Rf1 + Rf2}{Rf2} \quad (5)$$

More importantly, the ramp amplitude of CSP ripple may not be constant for different switching frequencies and Vin, Vout combinations, hence the offset CSP_ripple/2α is not fixed. This makes Vout accuracy even worse since it may vary when different Vin or switching frequency settings are applied.

Discontinuous Conduction Mode (DCM) of D-CAP2 converter is described in Figure 2 (b). Similar to CCM, an ON pulse is triggered when α*(VFB-VREF)+(CSP-CSN) = 0 V. After the ON pulse, the low side power transistor is turned on to pull the SW node to ground. Inductor current decreases during this period since negative voltage is applied to the inductor. Both high-side and low-side power transistors will be turned off when the inductor current is around 0 A to save power. SW node will equal Vout after both power transistors are turned off and the inductor current remains 0 A.

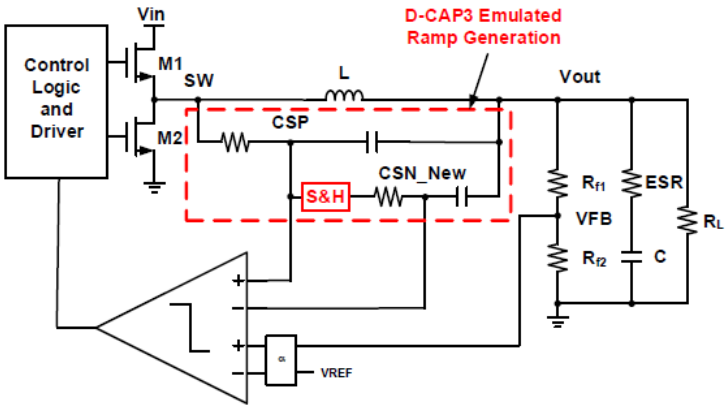

Figure 3. Structure of D-CAP3 Control

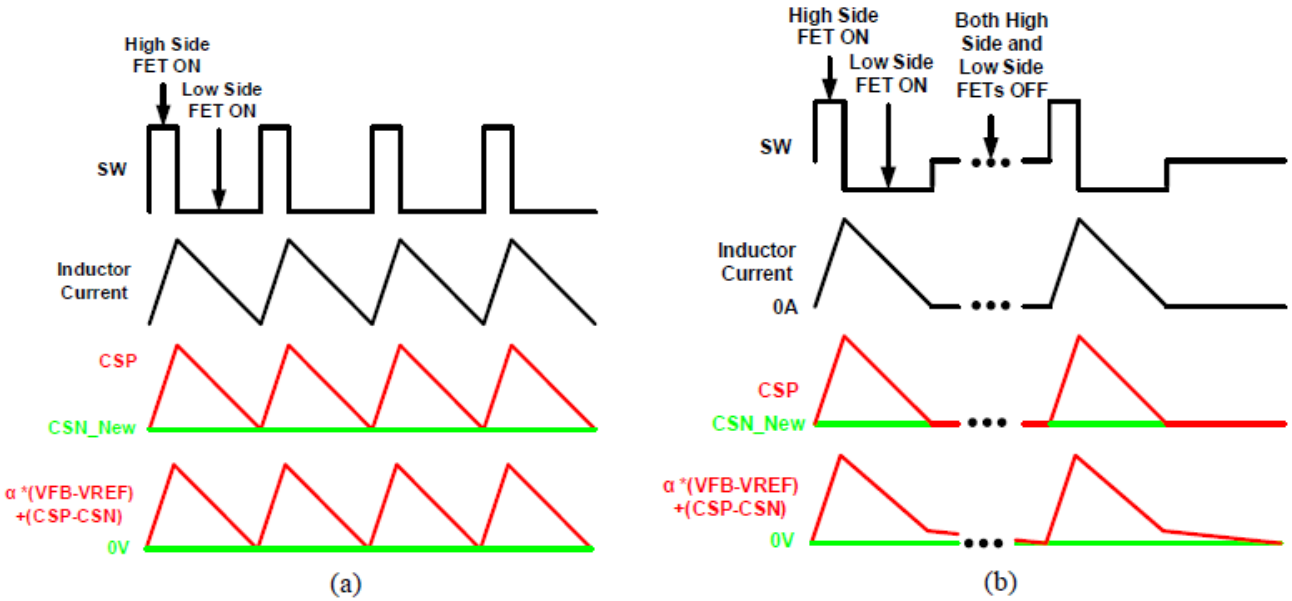

Figure 4. (a) CCM Operation and (b) DCM Operation of D-CAP3 Control

In Deep DCM, the time interval between two pulses is long so both CSN and CSP capacitors in the current sense filter network will be discharged. Meanwhile, with VSW = Vout

$$CSN = CSP\_valley = Vout \quad (6)$$

and the same turn on condition in Equation 2, VFB is forced to equal VREF in DCM operation:

$$VFB - VREF = 0 \quad (7)$$

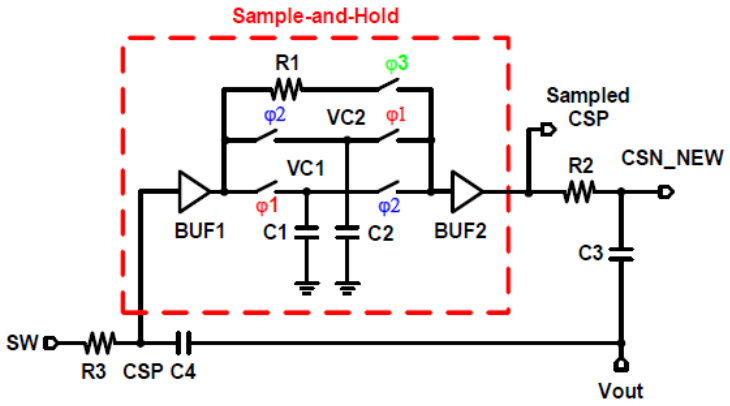

Figure 5. Circuit Implementation of D-CAP3 Ramp Generation Block

From Equation 4 and Equation 7, VFB and Vout are not constant in CCM and DCM. The difference in CCM and DCM greatly reduces Vout DC accuracy and therefore should be improved.

3 D-CAP3 Control Scheme

3.1 Structure and Operational Principle of D-CAP3 Control Scheme

Figure 3 shows the structure of the D-CAP3 control scheme. A Sample-and-Hold block is added between CSP and CSN filter. At valley of each CSP ripple, the Sample-and-Hold block samples CSP and holds it during the next switching cycle. CSN_New will be the filtered version of CSP_valley instead of CSP. CSN_New is used to replace CSN as the loop comparator input in D-CAP3. Figure 4 shows the operation of D-CAP3 in (a) CCM and (b) DCM. Since CSN_New is the filtered CSP_valley, it always equals to CSP_valley during normal operation in both CCM and DCM.

$$CSN\_New = CSP\_valley \tag{8}$$

By replacing CSN with CSN_New, the turn on condition of the high-side FET is:

$$\alpha \times (VFB - VREF) + (CSP - CSN\_New) = 0 \tag{9}$$

CSP increases after high-side FET is turned on. Therefore at turn on point, CSP=CSP_valley. This forces:

$$\alpha \times (VFB - VREF) = (CSN\_New - CSP\_valley) \tag{10}$$

By substituting Equation 8 into Equation 10, under all conditions we can get,

$$VFB = VREF \tag{11}$$

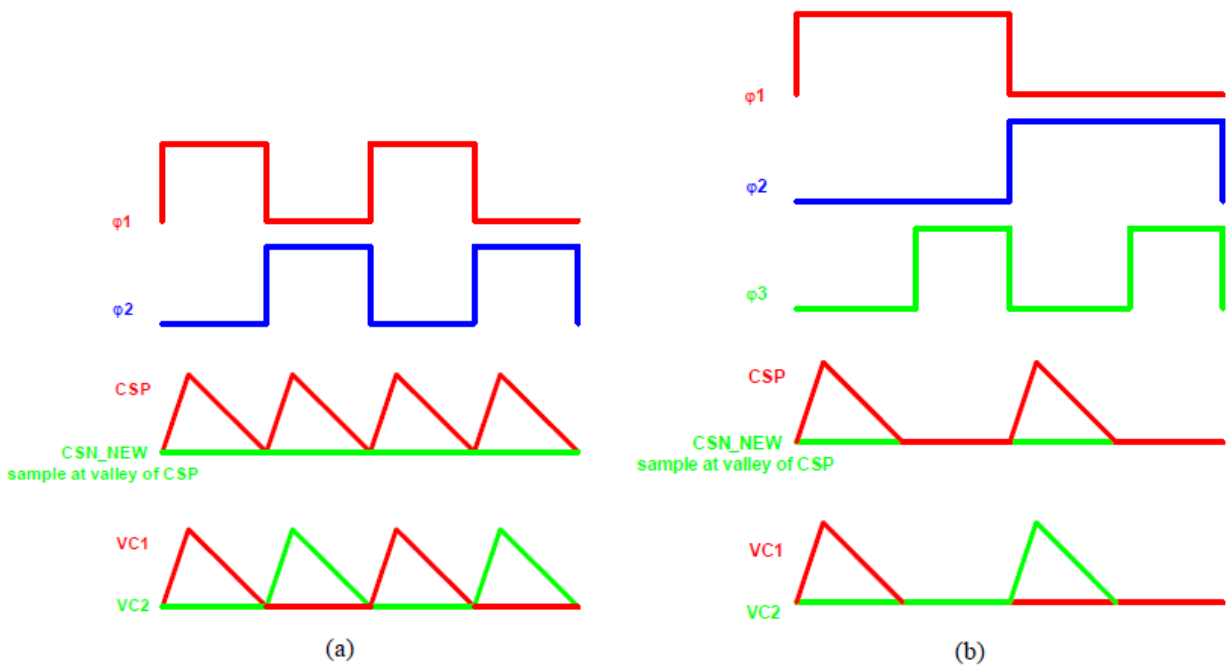

Figure 6. Operation of D-CAP3 Ramp Generation in (a) CCM and (b) DCM

VREF is a constant voltage reference, and by forcing VFB to always equal VREF, a constant Vout is achieved over different Vin, switch frequency, and load current settings. DC accuracy of the converter is thus improved. Meanwhile, compared to D-CAP2, only DC level of CSN is moved to valley of CSP to remove offset. High frequency effect of Sample-and-Hold will be filtered out by CSN filter. Small signal behavior of D-CAP3 is similar to that of D-CAP2 and fast transient response is thus maintained.

3.2 Circuit Implementation of D-CAP3

Figure 5 shows the structure of D-CAP3 ramp generation block. The Sample-and-Hold block is realized with two buffers BUF1 and BUF2, two sampling capacitors C1 and C2, one resistor R1, and five switches. R2, R3, C3, C4 form two filters for CSP and CSN_New signals.

With the use of BUF1 and BUF2, sample and hold voltages across capacitor C1, C2, and C3 can track quick voltage changes at inputs of the buffers without disturbing them. VC1 and VC2 are voltages across capacitor C1 and C2, respectively. Three phases φ1 to φ3 are applied to control ON/OFF states of the switches. During φ1, capacitor C1 is connected to output of BUF1 so VC1 is tracking CSP. At the same time C2 is connected to input of BUF2 and VC2 is holding CSP_valley from previous cycle. During φ2, VC2 is tracking while VC1 is holding. Since the holding capacitor is always connected to the input of BUF2, Sampled CSP will be equal to CSP_valley all the time. From Figure 6, φ1 and φ2 change ON/OFF state right before high-side power transistor is turned on and φ3 is high only when both high-side and low-side power transistors are off. φ1 to φ3 signals can thus be generated from gate control signals of high-side and low-side power transistors with logic circuitry.

Figure 6 shows the timing diagram of D-CAP3 ramp generation. In CCM, φ1 and φ2 are set to high alternately to sample CSP valley in each cycle and always hold CSP_valley at Sampled CSP. φ3 is always low in CCM. In DCM, φ3 is pulled to high after both high-side and low-side transistors are turned off. When φ3 is high, output of BUF1 is connected to input of BUF2 through resistor R1. This will prevent the holding capacitor from being discharged during the long waiting period between two DCM pulses. Compared to D-CAP2 implementation, only a Sample-and-Hold block is added in the ramp generation block to improve DC accuracy. The design change improves performance greatly at very low design cost.

4 D-CAP3 Results

Figure 7 shows simulation results with (a) D-CAP2 control and (b) D-CAP3 control. In D-CAP2 control, VFB is obviously higher in CCM than in DCM. The difference CSP_ripple/2α will be further multiplied by (Rf2+Rf1)/Rf2 times on Vout based on Equation 5. In D-CAP3 control, VFB is almost equal to VREF in both CCM and DCM. DC accuracy is thus greatly improved in the D-CAP3 design.

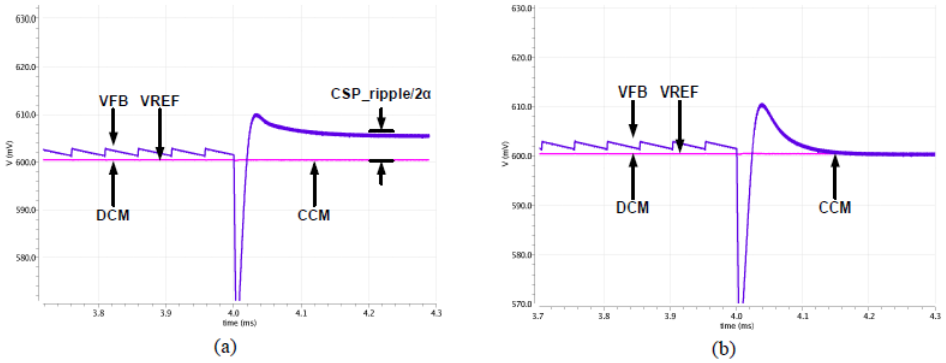

Figure 7. Simulation Results From (a) D-CAP2 Control and (b) D-CAP3 Control

Figure 8 is the measured load transient response of TPS53912. In this measurement VIN=5 V and Vout=1.2 V. Switching frequency is 500 kHz. Since internal reference voltage is 0.6 V, a resistor divider with Rf1=Rf2 is connected between Vout and ground to generate VFB. During the test, load current increases from 0 A to 3 A in 0.3 μs and the part goes into CCM from DCM. From Figure 8, Vout difference under CCM and DCM is eligible even when the oscilloscope is zoomed in to 10 mV/div. Since VFB is half of Vout, the difference in VFB under CCM and DCM is half of that on Vout. The constant voltage on both VFB and Vout indicates that good DC accuracy is achieved in the D-CAP3 design.

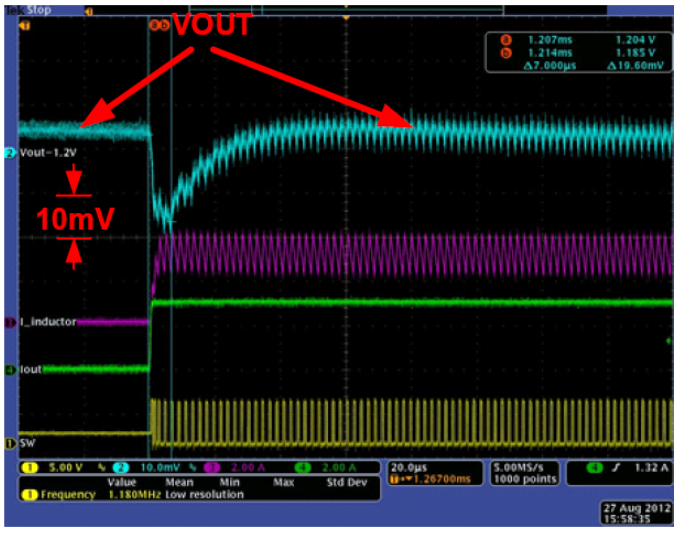

Figure 8. Measured Load Transient Response of TPS53912

5 Discussion

A new control scheme for switched-mode DC-DC converters has been presented in this paper. With the new D-CAP3 control scheme, DC accuracy of the converter is greatly improved. Meanwhile, fast transient response and low design cost are maintained. The new control scheme has been implemented in several products and has greatly improved performance of these products.

6 References

1. Daniel Meeks, “Loop Stability Analysis of Voltage Mode Buck Regulator with Different Output Capacitor Types – Continuous and Discontinuous Modes,” *TI Application Report*, April 2008
2. Robert Sheehan, “Understanding and Applying Current-Mode Control Theory”, *Power Electronics Technology Exhibition and Conference*, Nov. 2007
3. Chuan Ni and Tateishi Tetsuo “Adaptive Constant On-Time (D-CAPTM) Control Study in Notebook Applications”, *TI Application Report*, December 2007
4. Nancy Zhang, Wenkai Wu, Weidong Zhu, “D-CAP Mode with all-Ceramic Output Capacitor Application”, *TI Application Report*, Feb. 2011
5. Toshiyuki Zaitsu, Katsuya Goto, Takahiro Miyazaki, Junichi Yamamoto, “D-CAP2 Frequency Response Model,” *TI Application Report*, January 2013
6. Song Guo, “Improved Emulated Current RAMP for DC-DC Converter”, *TI Patent*, Feb. 2013

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2016) to A Revision	Page
• Changed the *Abstract* statement	1
• Changed the second paragraph in the *Introduction*	1
• Deleted figure "Photo of TPS53912 Layout"	6
• Deleted paragraph "D-CAP3 was first implemented in our product" in the *D-CAP3 Results* section	7
• Changed list item 3 in the *References* section	8

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