Application Report

Op Amp ESD Protection Structures

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ABSTRACT

All operational amplifier (op amp) input stages feature some sort of protection against electrostatic discharge (ESD). Most amplifiers accomplish this with diodes from both inputs and the output to both supply rails. While these diodes offer protection against ESD strikes, they can also lead to undesirable input leakage current when one, or both, of the inputs exceeds the V+ rail. However, there are a select few op amps with input stages designed to prevent this leakage. This application report covers the typical ESD protection structure along with an alternative protection structure. Additionally, testing methods for observing the behavior of the ESD protection under device shutdown is covered and sample data from devices with input protection structures that do not have diodes from the inputs to the V+ supply pin is included.

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1 Introduction

To help deal with short-term, high-voltage events, amplifiers have electrostatic discharge (ESD) protection structures. These structures typically feature diodes that protect amplifier inputs and outputs from unintended damage by clamping these pins to the supply rails under ESD conditions.

However, these diodes are not designed to be relied upon for electrical overstress (EOS) events where the input voltage significantly exceeds the supply rail for a longer period of time. Under such a scenario, leakage current can flow from the inputs to the supply rails. This can have undesirable effects including, but not limited to, *back-powering the amplifier*, device damage, and complete device failure. Understanding these scenarios and what can be done to avoid them is important in op amp circuit design.

This application note considers the typical amplifier ESD protection structure as well as an alternative structure that does not have diodes from the inputs to the V+ supply rail. Then, some Texas Instruments (TI) devices are highlighted with this alternative input protection structure and how the behavior of the protection structure of an op amp can be measured for certain scenarios.

2 Standard Op Amp ESD Protection

2.1 Standard Op Amp ESD Protection: Structure

The majority of op amps have input structures that include a protection diode between each input and each supply rail, as shown in Figure 2-1. The purpose of these diodes is to protect the amplifier from sudden ESD strikes by clamping the rising voltage and redirecting, or steering, the current surge away from the input stage transistors. If either input reaches a voltage greater than V+ plus the forward voltage of the ESD protection diode, the protection diodes will become forward biased and the current will flow from the input to ground. In a similar manner, if either input reaches a voltage lower than V- minus the forward voltage of the ESD protection diode, the protection diodes will become forward biased and the current will flow from ground to the input. Note that the forward voltage drop of the ESD diode is about 500 mV in many data sheets.

During an ESD event, several current paths are available, including through the absorption device, and the path taken depends on the voltages at the pins. An example is shown in Figure 2-1 where the IN+ pin takes a large, positive voltage and the V- pin is at ground. It is important to note that ESD protection is for out of circuit events, such as might occur during handling or assembly, and is not intended for in-circuit events.

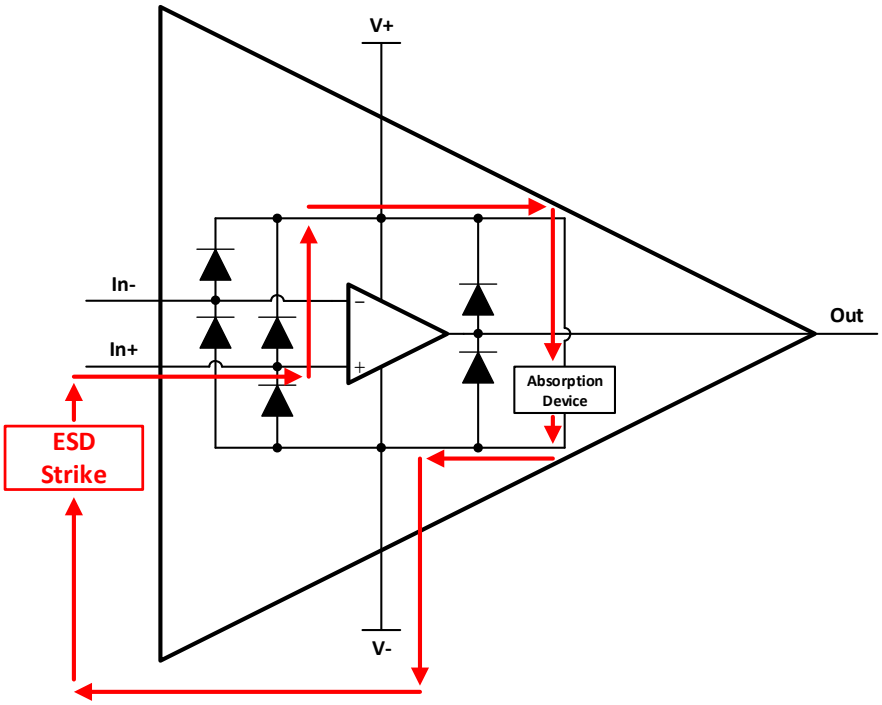


Figure 2-1. Path of Current During ESD Strike From In+ to V- for Op Amp With Standard ESD Protection

The behavior of the output protection diodes, also seen in Figure 2-1, mirrors that of the input protection diodes. If the output reaches a voltage higher than V+ plus the forward voltage of the ESD diode, a current path will form and current will flow from the output to ground. If the output reaches a voltage lower than V- minus the forward voltage of the ESD diode, a current path will form and current will flow from ground to the output.

Because this protection structure is designed for high-energy, short-duration ESD events, the diodes must be protected from destruction during the longer instances of Electrical Overstress (EOS). During EOS events, the applied voltage may be a lot lower. For example, it may be in the region of 500mV over the supply voltage rather than 1kV. However, these scenarios also last for much longer periods of time. The level of current that the protection diodes can sustain under EOS is often given in the "Absolute Maximum" section of the data sheet as ±10mA. Nonetheless, it is advisable to keep this number under ±1mA when possible.

If the circuit designer anticipates the possibility of either input going outside the min/max common-mode voltage range in the data sheet's Absolute Maximum Ratings table, it is common practice to include series resistors at the IN+ and IN- pins that are sized to limit the input current. Surpassing the common mode range may also necesitate the addition of external TVS diodes from the supply pins to ground for extra current protection. Though uncommon, there are cases when the output node may need resistive protection as well. This is true when there is a risk that the output node of the op amp will be driven while the op amp is turned off. These topics are covered in much more depth in the Texas Instruments Precision Labs presentations on ESD and EOS.

Table 2-1 shows an example Absolute Maximum Ratings table from the TLV9051/2/4 data sheet. Note that the common-mode voltage should be limited to be no less than (V-) – 0.5V and no more than (V+) + 0.5V. If this is not heeded, the diode paths will leak current. If enough current passes through, damage will occur to the amplifier's inputs and potentially render the device useless.

Table 2-1. Absolute Maximum Ratings for the TLV905x

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				7	V
Signal input pins	Voltage(1)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		V_S + 0.2	V
	Current(1)		–10	10	mA
Output short-circuit(2)			Continuous		
Operating ambient temperature, T_A			–40	150	°C
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.

(2) Short-circuit to ground, one amplifier per package.

2.2 Standard Op Amp ESD Protection: Considerations

The TLV9051 device has the traditional ESD diode protection shown in Figure 2-2. For certain applications, such as a battery-powered system, the circuit designer can choose to save power by temporarily turning off the amplifier. This can be done by floating, or leaving open, the V+ pin. It can also be done by grounding the V+ pin, which is the preferred alternative as is explained below. When the amplifier is turned off, the input may continue to see a voltage, such as a signal being generated by a sensor. A similar scenario can occur in a sensor circuit when the sensor turns on and sends a signal that reaches the amplifier's inputs before the amplifier's supply pins have fully ramped.

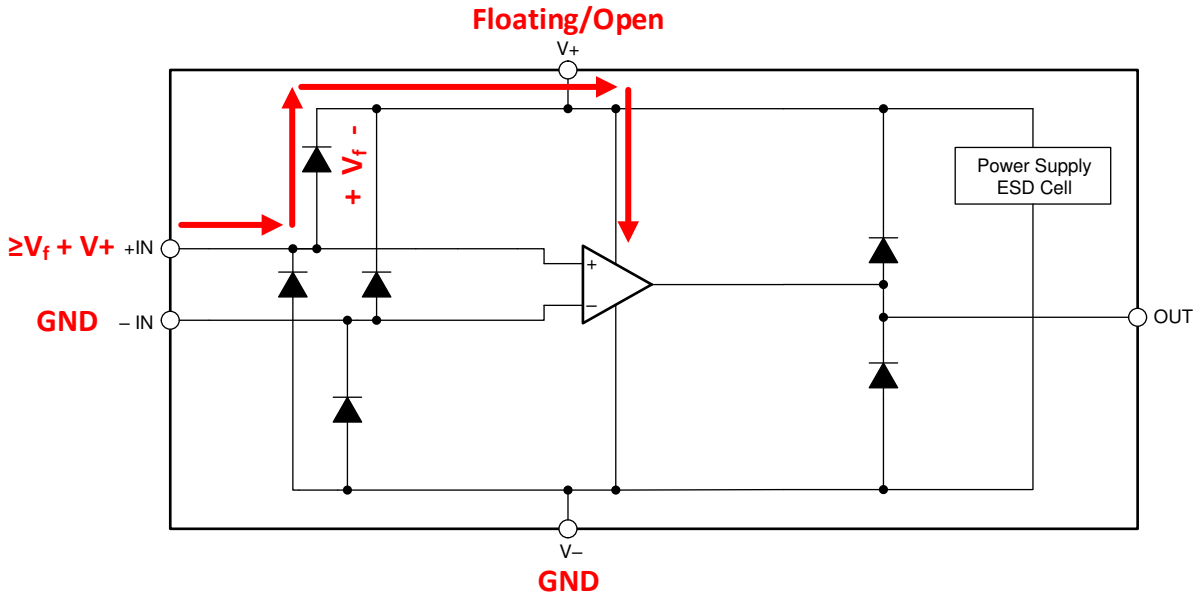


Figure 2-2. Input Current Path of a Back-Powered Op Amp

In such cases, there exists the possibility of back-powering the amplifier. If the input sees a voltage greater than the ESD diode's forward voltage plus the voltage at the V+ rail, then the diode can begin to leak. The voltage at the input creates a current through the ESD diode to the op amp supply pin. If the V+ pin is not being driven, the voltage can float up, especially if there is an impedance to ground at this node from another section of the circuit. The device is then turned on using the input signal as a crude voltage source. The output of the amplifier begins to provide undesired output signals, which can then feed to downstream components.

One way to help protect against accidentally back-powering the device is not to leave the V+ pin floating. When the pin is left floating or open, its voltage is unpredictable and it may not be possible to tell when the protection diode to V+, or even to V-, is likely to turn on. By grounding this pin, the circuit designer can help prevent the voltage of the V+ pin from floating upward and turning on the amplifier.

Even if grounding the V+ pin prevents the amplifier from being back-powered in such a scenario, there still exists the possibility of unwanted leakage current into the op amp. The input protection diode to V+ can still be turned on if the input voltage is higher than GND by the forward voltage drop of the protection diode. The best way to prevent back-powering of the amplifier and leakage current when the amplifier is off but an input is present is to avoid turning on the ESD diodes entirely. For cases when an input voltage is unavoidable while the amplifier is turned off, an alternate ESD protection scheme is needed.

3 Op Amp ESD Protection Without Input Diodes to V+

There are several op amps with an alternative input ESD protection structure that does not have a protection diode from the inputs to V+. This protection behaves differently than the typical protection. Parts in this category include: OPA348, TLV341/TLV341A, TLV342/TLV342A

3.1 Op Amp ESD Protection Without Input Diodes to V+: Structure

Figure 3-1 shows an example of an alternate input protection structure for the IN+ and OUT pins. The same structure is present on the IN- pin as on the IN+ pin, though it is not shown here for the sake of simplicity. In contrast, the output pin has diode paths to both rails. Note that not all of the input protection is shown here. Instead, this figure shows only the portion most relevant to this application report.

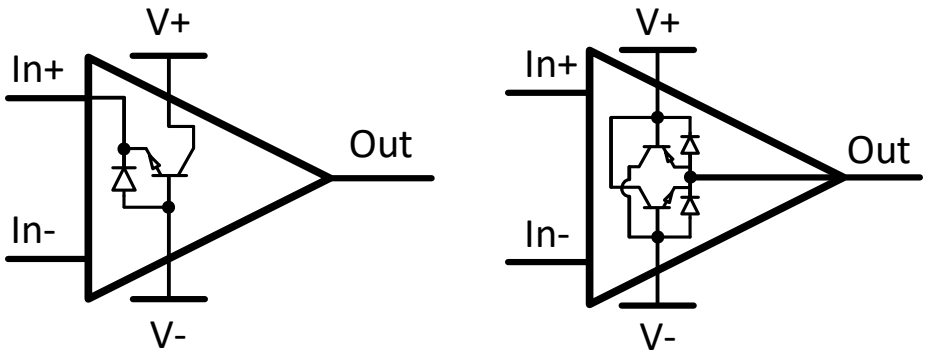


Figure 3-1. Leakage Paths for IN+ (also present for IN-) and OUT

With this type of structure, IN+ and IN- can exceed V+ without turning on a diode protection path and conducting current. For example, if V+ and V- are grounded, then leakage current is prevented in the case of a positive input signal. Similarly, if V+ is left open and V- is grounded while a positive input signal is seen, then leakage current and the possibility of back-powering the amplifier are avoided as long as V+ is not permitted to float high.

There is a limit to how far the input voltage can be taken beyond V+. Eventually, the input will be driven too far and significant current will begin to flow. This limit will depend on the operating circumstances of the circuit and is not specified in product data sheets. Thus, the circuit designer should test the limits of the device under the expected operating conditions to validate the proper operation of the circuit and ensure that excessive current flow is avoided. Example test setups and sample data are provided later in this document.

Finally, it is important to remember that the devices in question will still start to turn on their diode protection paths if one of the input pins falls below the input voltage range, just as the parts with the standard op amp ESD protection. So it is important to consider what type of input signals will be present while the amplifier is turned off.

3.2 Op Amp ESD Protection Without Input Diodes to V+: Considerations

As mentioned in the previous section, there is a limit to how far amplifiers with alternate input ESD protection can exceed the V+ rail. When this limit is exceeded, the leakage current will begin to rise rapidly. Should the input voltage continue to rise, a deep snap back effect occurs at the input. The deep snap back effect causes the voltage of the protection circuitry to suddenly fall and clamp the input voltage at a much lower level. The danger with deep snap back is that the input current can go very high and risk damage to the input structure of the part. Furthermore, the device can become stuck in this state, a phenomenon known as "latch-up." For more information on ESD protection snap-back, see Matthew Xiong's blog post, "The dangers of deep snap-back ESD circuit-protection diodes."

ESD protection structures without input diodes to the V+ rail can work well in applications where the amplifier must be turned off while an input signal is present. But the possibility of a deep snap back effect needs to be considered. It is a best practice to avoid entering the high current conduction regions altogether. For more protection, input resistors can be added to limit the input leakage to ±10mA, or even ±1mA when possible.

An example of this effect is shown in Figure 3-3. In this example, the OPA348 amplifier has its V- pin at ground and its V+ pin connected to a supply at 0V. The output and inverting input are left open, while the non-inverting input is driven with a positive voltage. The corresponding input leakage current is then measured. The test configuration is shown in Figure 3-2.

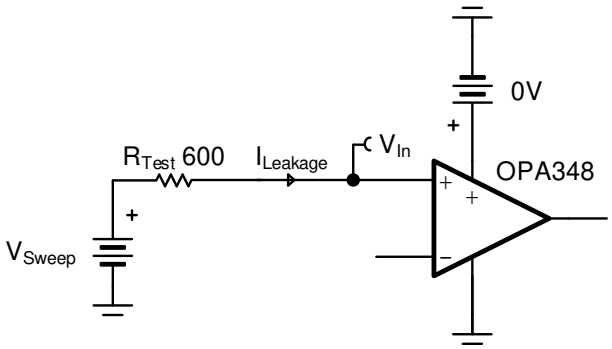


Figure 3-2. OPA348 - Test Setup of Leakage Current for Extended Applied Input Voltage

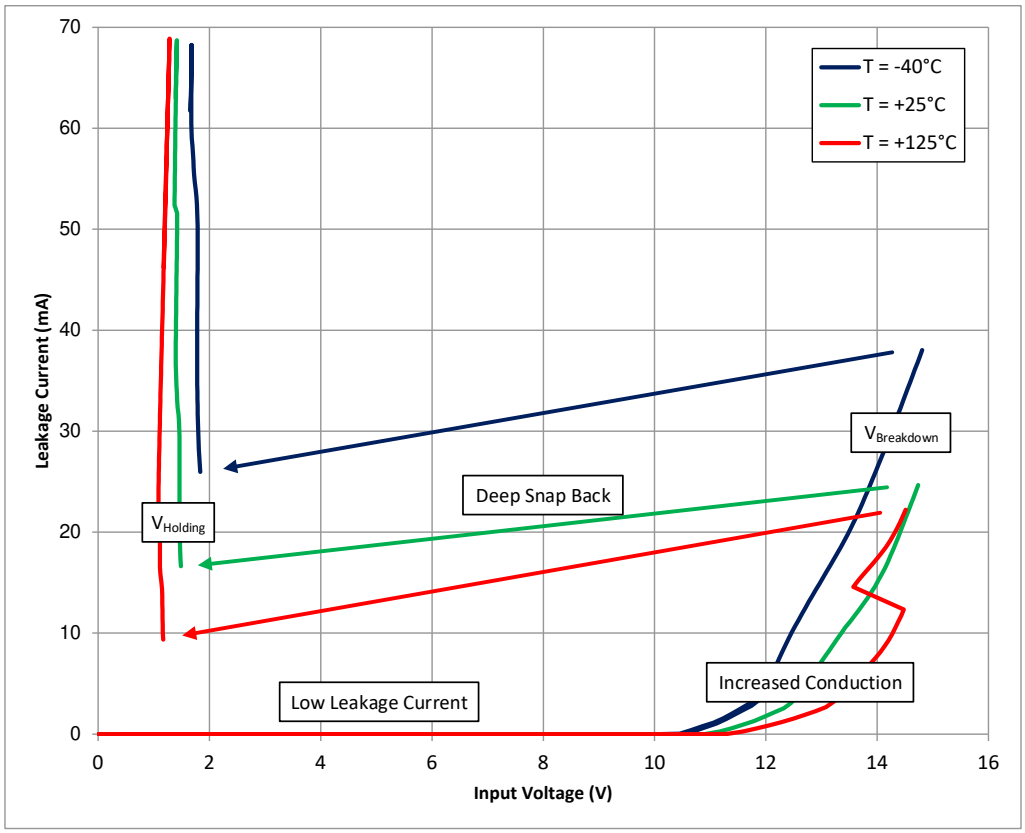
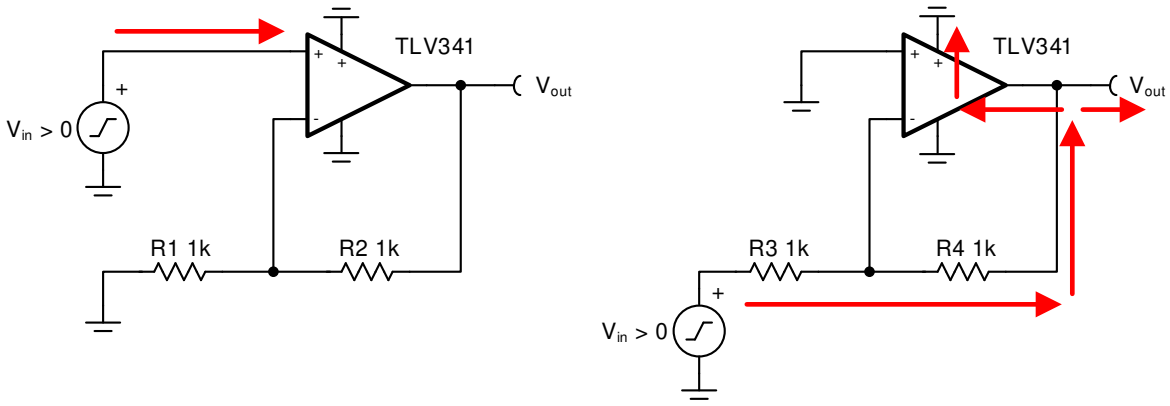


Figure 3-3. OPA348 - Leakage Current for Extended Applied Input Voltage

From an input voltage of 0V to about 10V, there is low leakage current. In this region, the alternate ESD protection structure prevents an input signal from back-powering the amplifier or creating significant leakage current. After about 10.5V, the input current begins to rise rapidly. When the input is driven even further, deep snap back occurs. The voltage suddenly drops and is clamped at a lower level. Simultaneously, the input current rises to very high levels. This is hazardous for the part and the operating regions of higher current should be avoided to prevent damage. For the purpose of demonstration, the input current in this experiment was allowed to exceed the data sheet limit of 10mA. Do not exceed the absolute maximum ratings in your design.

It should also be pointed out that an alternate input structure does not prevent all possibilities of unwanted current, even if the amplifier is off. For example, if a TLV341 amplifier is placed in a non-inverting configuration while the supplies are grounded and the device turned off, the input will be able to handle some positive voltage without leaking current to the V+ rail or output (Figure 3-4 left). However, if the same amplifier under the same scenario is put into an inverting configuration, current will not pass through the input pin but will be passed to the output through the feedback loop (Figure 3-4 right). Furthermore, it may turn on the diodes at the output pin and pass into the V+ pin. So, care must be given not just to the op amp, but also to the circuit setup.



Non-Inverting Amplifier Configuration Inverting Amplifier Configuration

Figure 3-4. Circuit Configuration Can Influence Leakage Current

4 How to Measure the Leakage Current of an Op Amp's ESD Protection Structure

The leakage current of an op amp can be measured to better understand the behavior of its ESD protection circuitry. One method of measurement involves picking an amplifier, grounding the supply pins, and sweeping the voltage at the input and output pins one pin at a time. The pins not under test can be left open. Measuring the corresponding current passing through the V+ and V- pins shows the amount of leakage current. This setup is shown in Figure 4-1 and gives an idea of amplifier behavior when the amplifier is turned off with grounded supply pins and an input or output signal is still present. To avoid damaging the device during testing, it is a good idea to limit the current available from the voltage source to ±10 mA. In production, it is better to limit the current to ±1mA when possible. This test method was used to confirm the input structure behavior of some devices and the sample data can be found in Appendix A.

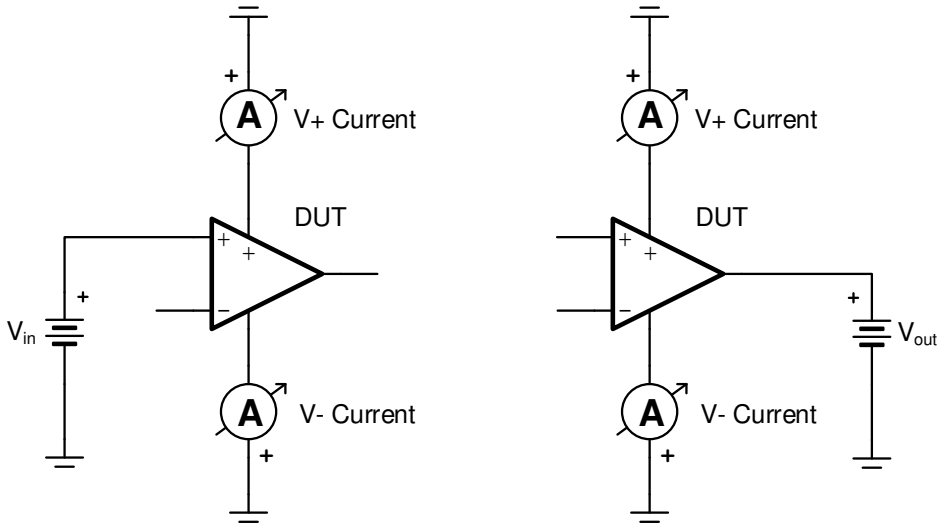


Figure 4-1. Setup 1 - Example Schematic for Testing IN+ and OUT Pins With Grounded Supplies

Depending on how the amplifier is turned off, a different test setup may be more appropriate for accurately observing the leakage current while an input or output voltage is present. For example, a shutdown pin may allow the circuit designer to put the amplifier into shutdown mode while the V+ supply pin still has a voltage present. Alternatively, some circuit designers look to turn off their amplifiers by switching open the V+ pin. Alternate leakage current test setups for some of the more popular scenarios are shown in Figure 4-2 through Figure 4-4. Sample data for these test setups is also available in Appendix A.

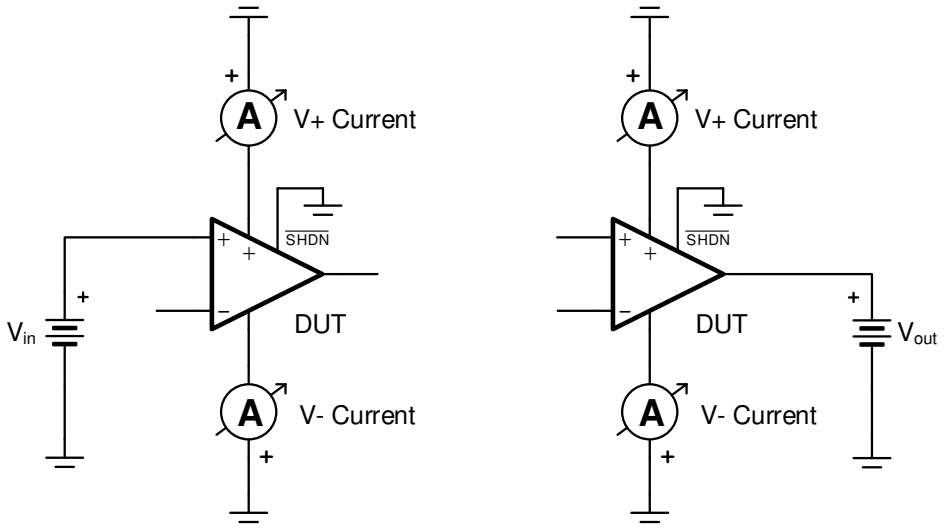


Figure 4-2. Setup 2 - Example Schematic for Testing IN+ and OUT Pins With Grounded Supplies and Shutdown Pin

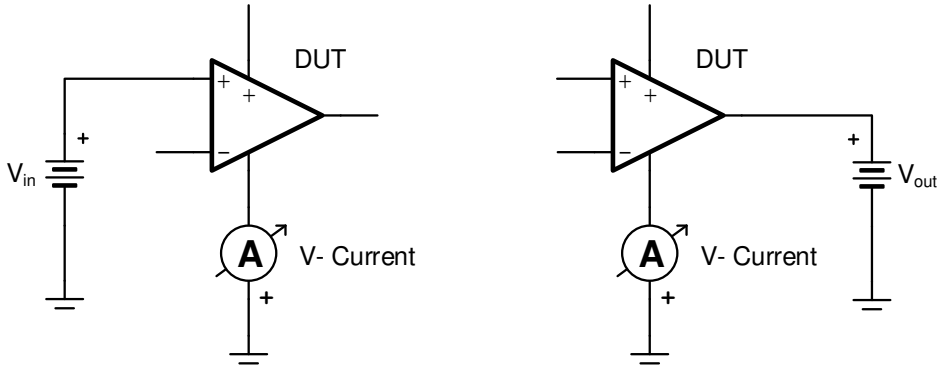


Figure 4-3. Setup 3 - Example Schematic for Testing IN+ and OUT Pins With Open V+ Pin and Grounded V- Pin

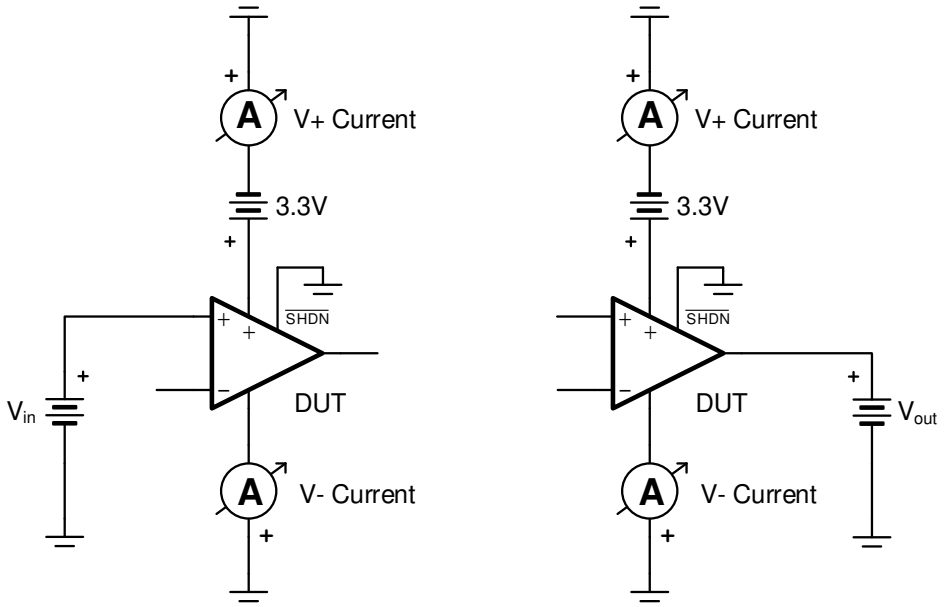


Figure 4-4. Setup 4 - Example Schematic for Testing IN+ and OUT Pins With Power on V+ Pin, Grounded V- Pin and Shutdown Pin Low

5 Summary

Most amplifiers come with standard ESD diode structures to protect them from sudden, high-voltage discharges. Although these are robust circuits, alternative protection structures are preferable in some applications. It is important for analog circuit engineers to understand the strengths and limits of different ESD protection circuits and to be able to verify the type of protection structure of an op amp.

6 References

1. To learn more about back-powering amplifiers, see Tim Claycomb's Precision Hub blog post titled, "The self-powering device?"
2. To learn more about ESD and its effects on op amps, visit the TI Precision Labs Presentation on Electrostatic Discharge (ESD).
3. To learn more about EOS and its effects on op amps, visit the TI Precision Labs Series on Electrical Overstress (EOS).
4. For more information on ESD protection snap-back, see Matthew Xiong's blog post, "The dangers of deep snap-back ESD circuit-protection diodes."

A Measured Data for Op Amps With Alternate ESD Protection

The results in the appendix were gathered using the test setups described in Section 4. Data was taken at room temperature. To learn about changes over temperature, see Figure 3-3.

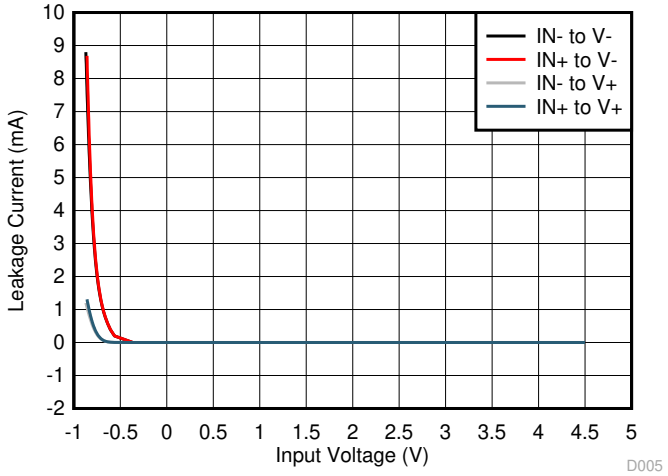


Figure A-1. OPA348 - Setup 1 - Leakage Current for Applied Input Voltage

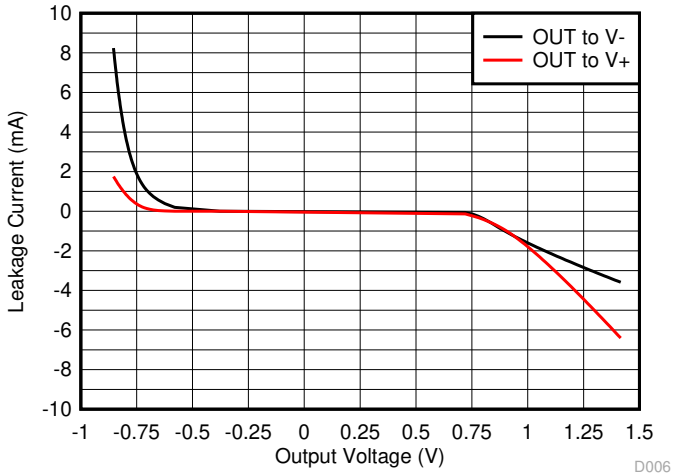


Figure A-2. OPA348 - Setup 1- Leakage Current for Applied Output Voltage

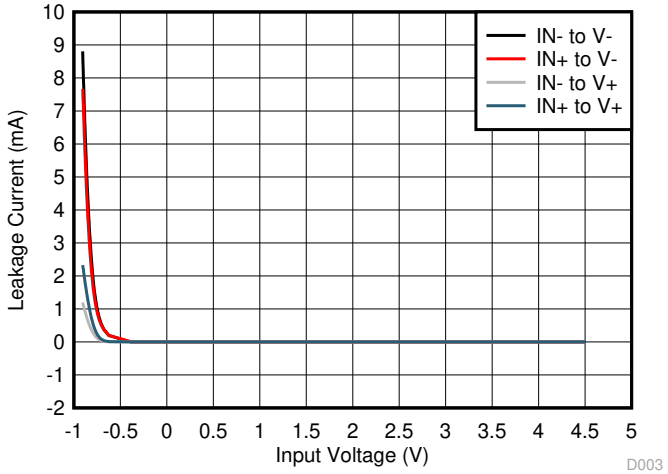


Figure A-3. TLV342/TLV342A - Setup 1- Leakage Current for Applied Input Voltage

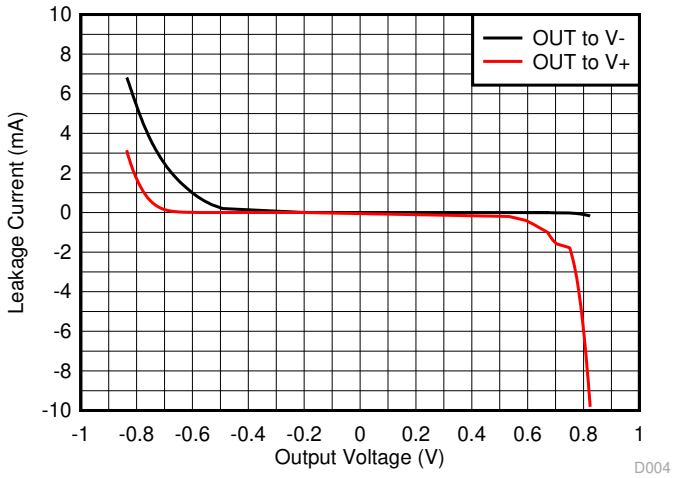


Figure A-4. TLV342/TLV342A - Setup 1 - Leakage Current for Applied Output Voltage

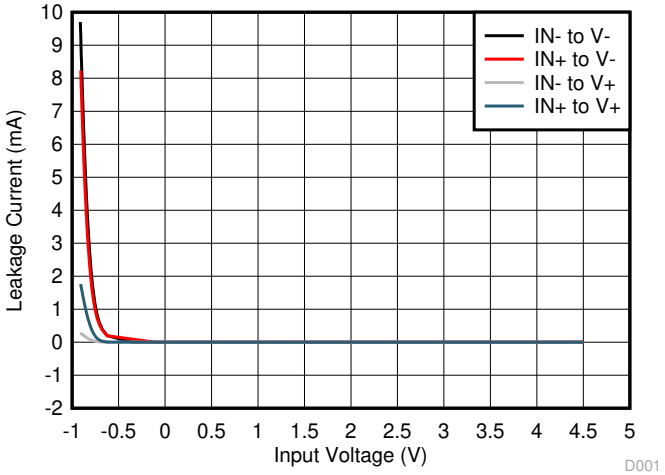


Figure A-5. TLV341/TLV341A - Setup 2 - Leakage Current for Applied Input Voltage

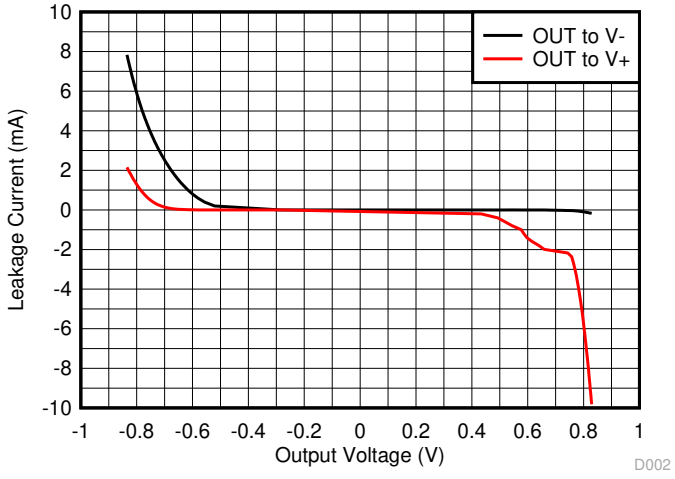


Figure A-6. TLV341/TLV341A - Setup 2 - Leakage Current for Applied Output Voltage

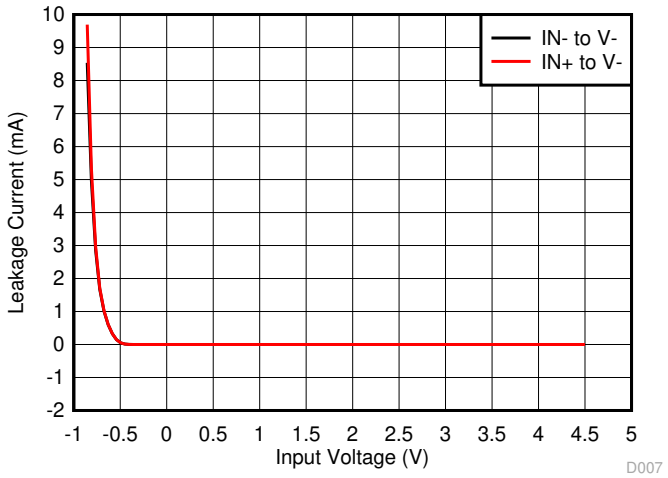


Figure A-7. OPA348 - Setup 3 - Leakage Current for Applied Input Voltage

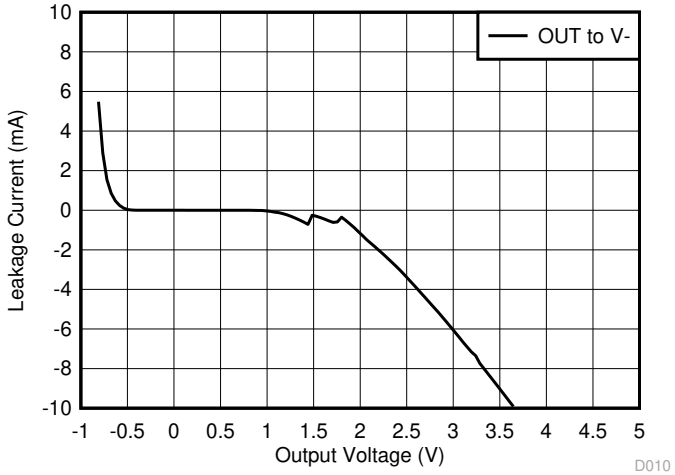


Figure A-8. OPA348 - Setup 3 - Leakage Current for Applied Output Voltage

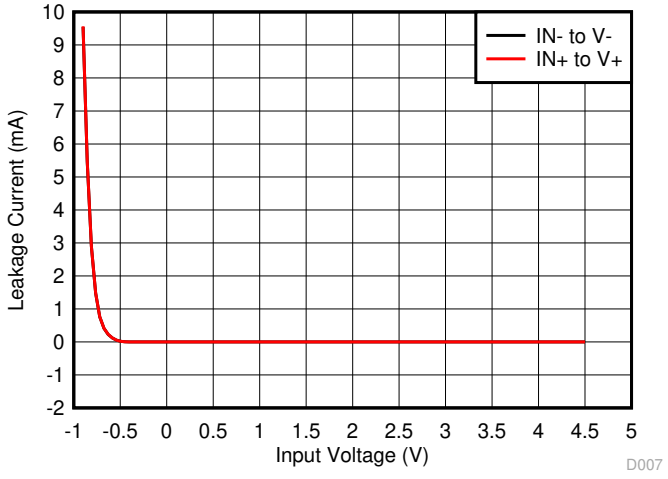


Figure A-9. TLV342/TL342A - Setup 3 - Leakage Current for Applied Input Voltage

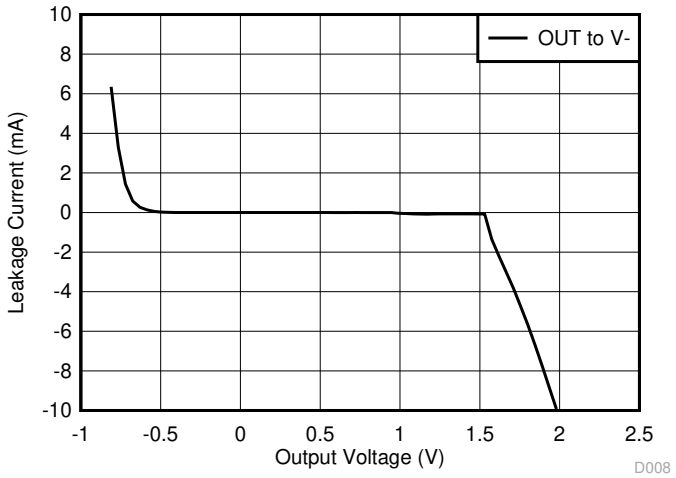


Figure A-10. TLV342/TLV342A - Setup 3 - Leakage Current for Applied Output Voltage

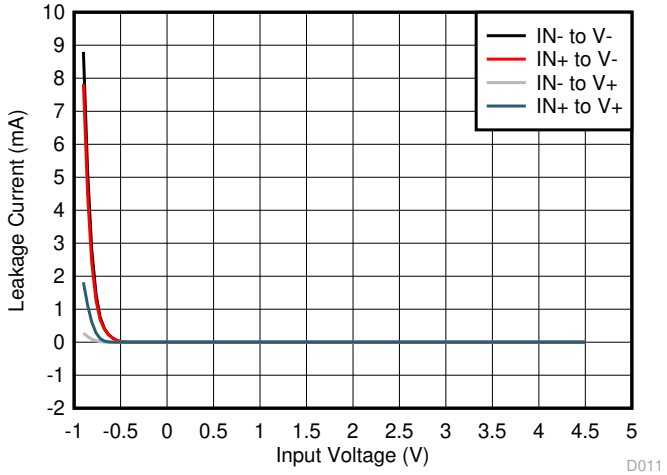


Figure A-11. TLV341/TLV341A - Setup 4 - Leakage Current for Applied Input Voltage

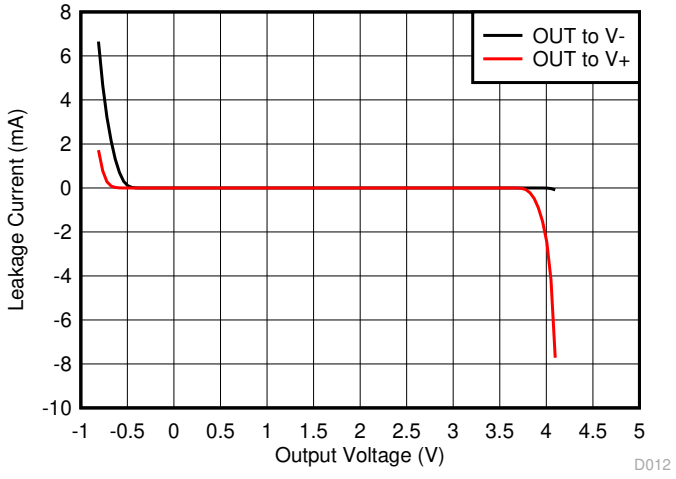


Figure A-12. TLV341/TLV341A - Setup 4 - Leakage Current for Applied Output Voltage

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