

# LDO noise examined in detail

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## Introduction

Requirements and expectations for telecommunication systems continue to evolve as complexity and reliability of the communication channels continue to increase. These communication systems rely heavily on high-performance, high-speed clocking and data-converter devices. The performance of these devices is highly dependent on the quality of system power rails. A clock or converter IC simply cannot achieve top performance when powered by a dirty power supply. Just a small amount of noise on the power supply can cause dramatic negative effects on the performance. This article examines a basic LDO topology to find its dominant noise sources and suggests ways to minimize its output noise.

A key parameter indicating the quality of a power supply is its noise output, which is commonly referred to by the RMS noise measurement or by the spectral noise density. For the lowest RMS noise or the best spectral noise characteristics, a linear voltage regulator like a low-dropout voltage regulator (LDO) always has an advantage over a switching regulator. This makes it the power supply of choice for noise-critical applications.

## Basic LDO topology

A simple linear voltage regulator consists of a basic control loop where a negative feedback is compared to an internal reference in order to provide a constant voltage—regardless of changes or perturbations in the input voltage, temperature, or load current.

Figure 1 shows a basic block diagram of an LDO regulator. The red arrow indicates the negative-feedback signal path. The output voltage,  $V_{OUT}$ , is divided by feedback resistors  $R1$  and  $R2$  to provide the feedback voltage,  $V_{FB}$ .  $V_{FB}$  is compared to the reference voltage,  $V_{REF}$ , at the negative input of the error amplifier to supply the gate-drive voltage,  $V_{GATE}$ . Finally, the error signal drives the output transistor, NFET, to regulate  $V_{OUT}$ .

A simplified analysis of noise begins with Figure 2. The blue arrow traces a subset of the loop represented by a common amplifier variation known as a voltage follower or power buffer. This voltage-follower circuit forces  $V_{OUT}$  to follow  $V_{REF}$ .  $V_{FB}$  is the error signal referring to  $V_{REF}$ . In steady state,  $V_{OUT}$  is bigger than  $V_{REF}$ , as described in Equation 1:

Figure 1. Negative-feedback loop of LDO

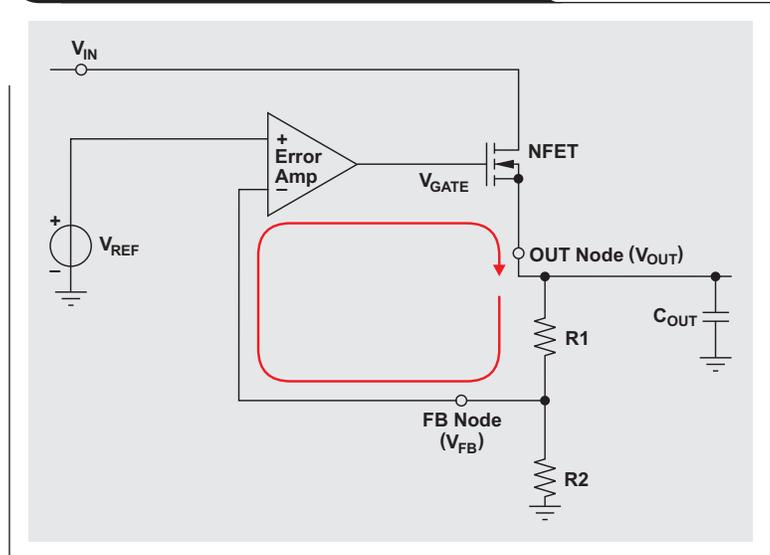
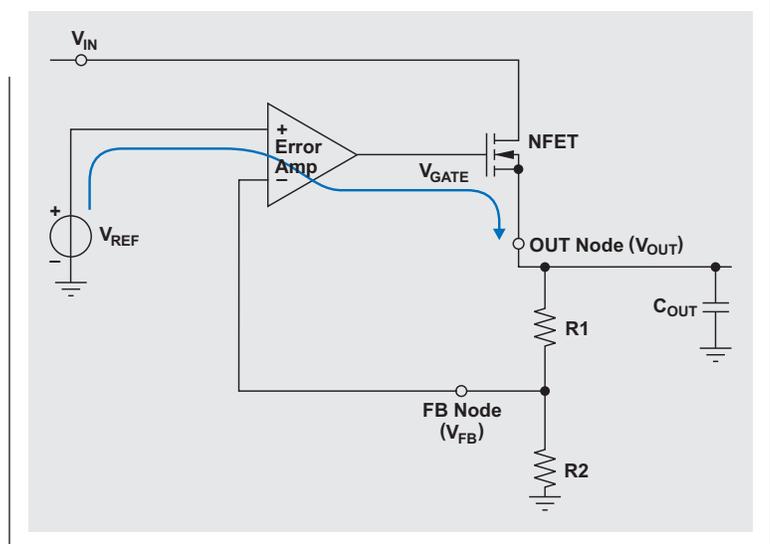


Figure 2. Reference-voltage buffering of LDO



$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \times V_{REF}, \quad (1)$$

where  $1 + R1/R2$  is the gain that the error amplifier must have to obtain the steady-state output voltage ( $V_{OUT}$ ).

Suppose the voltage reference is not ideal and has an effective noise factor,  $V_{N(REF)}$ , on its DC output voltage ( $V_{REF}$ ). Assuming all circuit blocks in Figure 2 are ideal,  $V_{OUT}$  becomes a function of the noise source. Equation 1 can be easily modified to account for the noise source, as described in Equation 2:

$$V_{OUT} + V_{N(OUT)} = \left(1 + \frac{R1}{R2}\right) \times (V_{REF} + V_{N(REF)}), \quad (2)$$

where  $V_{N(OUT)}$  is the independent noise contribution to the output, expressed by Equation 3:

$$V_{N(OUT)} = \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)} \quad (3)$$

From Equations 2 and 3, it's clear that a higher output voltage generates higher output noise. The feedback resistors, R1 and R2, set (or adjust) the output voltage, thereby setting the output noise voltage. For this reason, many LDO devices characterize the noise performance as a function of output voltage. For example,  $V_N = 16 \mu V_{RMS} \times V_{OUT}$  illustrates a standard form describing the output noise.

### Dominant sources of LDO output-voltage noise

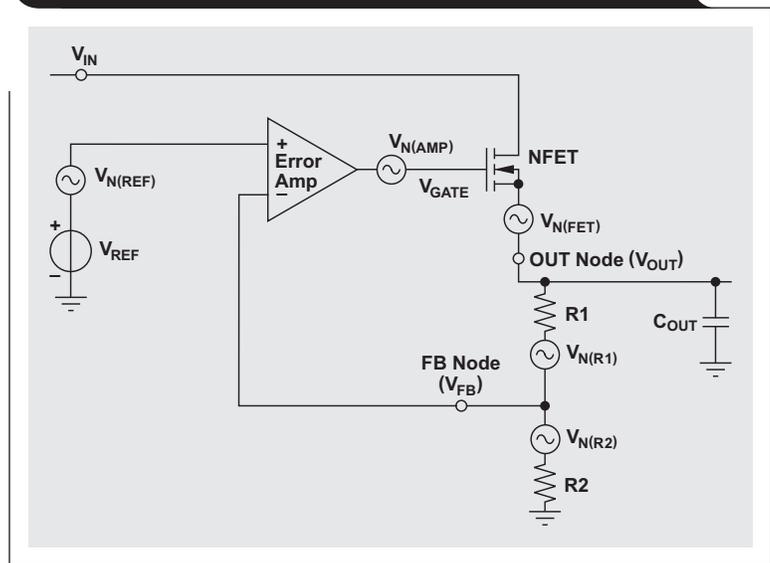
For most typical LDO devices, a dominant source of output noise is the amplified reference noise in Equation 3. This is generally true even though the total output noise is device-dependent. Figure 3 is a complete block diagram showing each equivalent-noise source corresponding to its respective circuit element. Since any device with current flowing through it is a potential noise source, every single component in Figure 1 and Figure 2 is a noise source.

Figure 4 is redrawn from Figure 3 to include all equivalent-noise sources referenced at the OUT node. The complete noise equation is

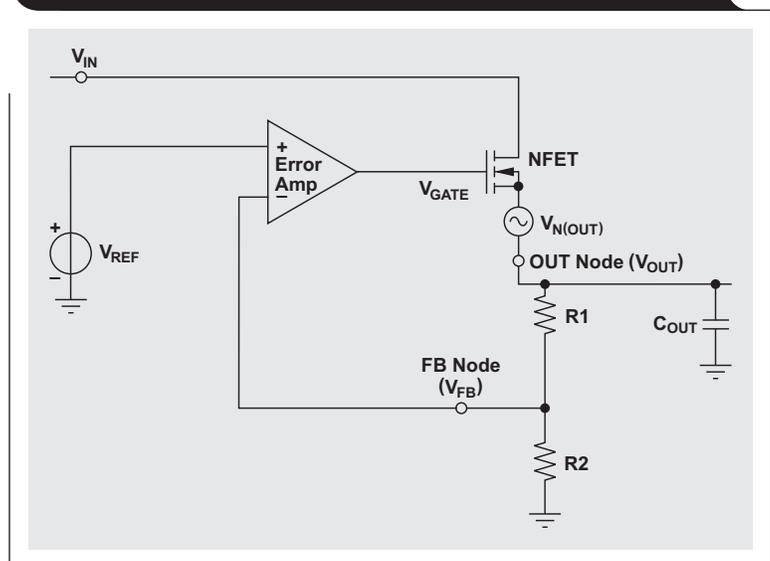
$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1 + \frac{R1}{R2}\right) \times (V_{N(REF)} + V_{N(R1)} + V_{N(R2)}). \quad (4)$$

In most cases, because the reference-voltage block, or bandgap circuit, consists of many resistors, transistors, and capacitors,  $V_{N(REF)}$  tends to dominate the last three

**Figure 3. LDO topology with equivalent-noise sources**



**Figure 4. LDO topology with a consolidated noise source**



noise sources in this equation where  $V_{N(REF)} \gg V_{N(R1)}$  or  $V_{N(REF)} \gg V_{N(R2)}$ . Thus, Equation 4 can be simplified to

$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)}. \quad (5)$$

For higher-performance LDO devices, it is common to add a noise-reduction (NR) pin to shunt reference noise to ground. Figure 5 illustrates how the NR pin works to reduce noise. Since it is known that  $V_{N(REF)}$  is the dominant output-noise source, an RC filter capacitor,  $C_{NR}$ , is inserted between the reference-voltage block ( $V_{REF}$ ) and the error amplifier to reduce this noise. This RC filter reduces the noise by an attenuation function of

$$G_{RC}(f) = \frac{1}{\sqrt{1+(f/f_p)^2}} < 1, \quad (6)$$

where

$$f_p = \frac{1}{2\pi \times R_{NR} \times C_{NR}}$$

The amplified reference noise is therefore reduced to  $(1 + R1/R2) \times V_{N(REF)} \times G_{RC}$ , and Equation 5 then becomes

$$V_{N(OUT)} = V_{N(AMP)} + V_{N(FET)} + \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)} \times G_{RC} \quad (7)$$

In the real world, all control signal levels are frequency-dependent, including the noise signal. If the error amplifier has limited bandwidth, the high-frequency reference noise ( $V_{N(REF)}$ ) is filtered by the error amplifier in a way similar to using an RC filter. But in reality an error amplifier tends to have a very wide bandwidth, so the LDO device has very good power-supply ripple rejection (PSRR), which is another key performance parameter of high-performance LDOs. To satisfy this conflicting requirement, IC vendors settle on having a wide-bandwidth error amplifier for the best PSRR over less noise. This decision leads to using an NR pin function if low noise is also mandatory.

### Controlling reference noise in a typical circuit

#### Amplified reference noise

The Texas Instruments (TI) TPS74401 LDO was used for testing and measurements. The common setup parameters are shown in Table 1. Please note that a soft-start capacitor,  $C_{SS}$ , in the TPS74401 datasheet<sup>1</sup> is referred to as a noise-reduction capacitor,  $C_{NR}$ , in this article for easier reading.

First, the effect of the amplifier gain was examined with a negligibly small  $C_{NR}$ . Figure 6 shows RMS noise versus output-voltage settings. As discussed earlier, the dominant noise source,  $V_{N(REF)}$ , is amplified by the ratio of the feedback resistors R1 and R2. Equation 7 can be modified into the form of Equation 8:

$$V_{N(OUT)} = V_{N(Other)} + \left(1 + \frac{R1}{R2}\right) \times V_{N(REF)} \times G_{RC}, \quad (8)$$

where  $V_{N(Other)}$  is the sum of all other noise sources.

Figure 5. LDO topology with reference-noise filter

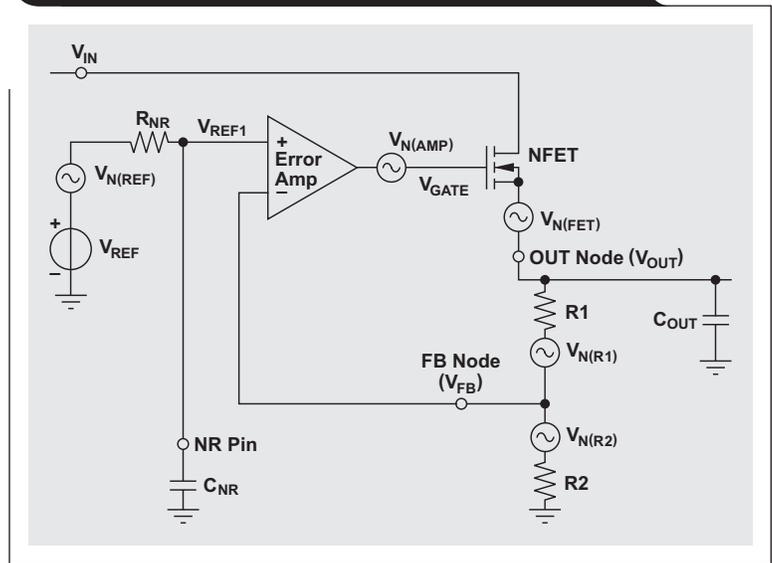


Figure 6. RMS noise versus output voltage

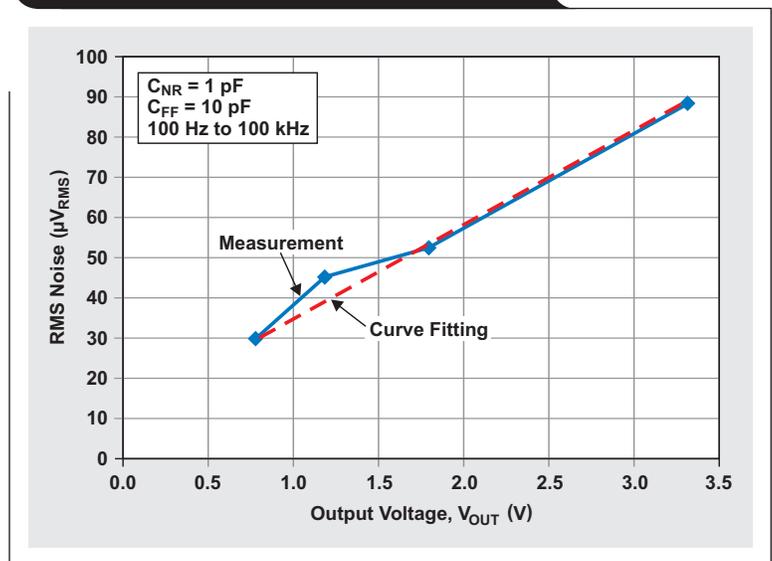


Table 1. Setup parameters

$V_{IN} = V_{OUT(Target)} + 0.3 V$	$I_{OUT} = 0.5 A$		$C_{OUT} = 10 \mu F$
$V_{OUT(Target)}$	R1	R2	$1 + R1/R2$
3.3 V	31.25 kΩ	10 kΩ	4.125
1.8 V	12.5 kΩ	10 kΩ	2.25
1.2 V	5 kΩ	10 kΩ	1.5
0.8 V	0 Ω (short OUT node to FB node)	Open circuit	1

If Equation 8 is fitted to a linear curve of the form  $y = ax + b$  as shown by the red dotted line in Figure 6,  $V_{N(REF)}$  (the slope term) can be estimated as  $19 \mu V_{RMS}$ , and  $V_{N(Other)}$  (the y-intercept term) as  $10.5 \mu V_{RMS}$ . As explained

later under “Effect of the noise-reduction (NR) pin,” the value of  $C_{NR}$  was chosen as 1 pF to minimize the RC-filter effect to a negligible level, and  $G_{RC}$  is treated as being equal to 1. In this situation, the basic assumption is that  $V_{N(REF)}$  is the dominant noise source.

Note that the minimum noise occurs when the OUT node is shorted to the FB node, making the amplifier gain  $(1 + R1/R2)$  equal to 1 ( $R1 = 0$ ) in Equation 8. Figure 6 shows this minimum-noise point to be approximately  $30 \mu V_{RMS}$ .

**Canceling amplified reference noise**

This section explains a very effective technique for achieving a configuration with minimum output noise. A feedforward capacitor,  $C_{FF}$ , forwards (bypasses) output noise around  $R1$  as illustrated in Figure 7. This bypass or shorting action prevents the reference noise from being increased by the gain of the error amplifier at frequencies higher than the resonant frequency,  $f_{Resonant}$ , of  $R1$  and  $C_{FF}$ , where

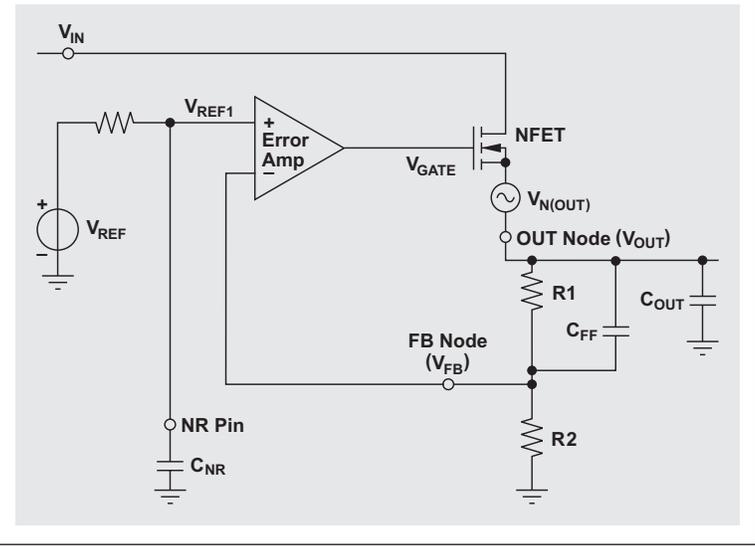
$$f_{Resonant} = \frac{1}{2\pi \times R1 \times C_{FF}}$$

The output noise becomes

$$V_{N(OUT)} = V_{N(Other)} + \left[ 1 + \frac{R1 \parallel \frac{1}{2\pi \times f \times C_{FF}}}{R2} \right] \times G_{RC} \times V_{N(REF)}$$
(9)

Figure 8 shows the changes in RMS noise relative to feedforward capacitance ( $C_{FF}$ ) and different output-voltage settings. Note that each point along each RMS plot represents the statistical mean of the integrated noise across

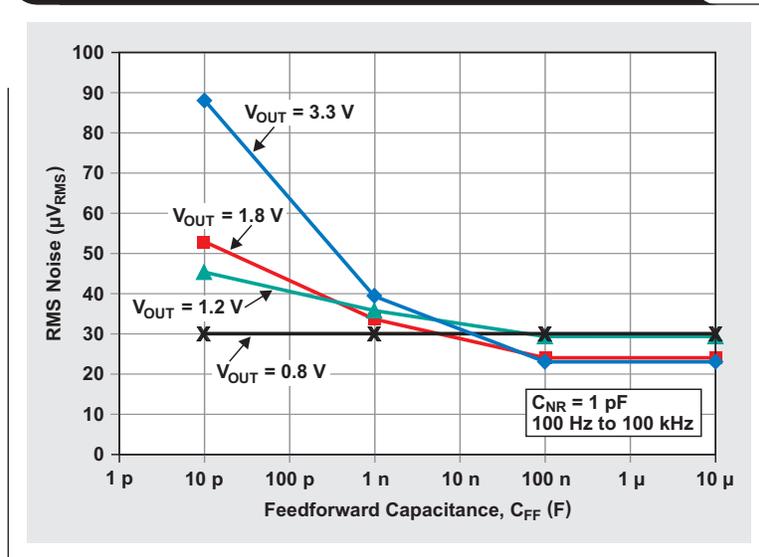
**Figure 7. LDO topology with feedforward capacitor ( $C_{FF}$ ) for minimizing noise**



the entire given bandwidth of interest for the circuit conditions described. As expected, all curves converge toward the minimum output noise of approximately  $30 \mu V_{RMS}$ ; in other words, the noise converges to  $V_{N(REF)} + V_{N(Other)}$  due to the effect of  $C_{FF}$ .

Figure 8 illustrates that, for a  $C_{FF}$  value greater than 100 nF, the amplifier gain of  $1 + R1/R2$  in Equation 8 is canceled. This is true only because the low-frequency noise does not contribute significantly to the overall statistical mean of the RMS calculation, even though that low-frequency noise is not completely canceled by  $C_{FF}$ . In order to see the actual effect of  $C_{FF}$ , it is necessary to look

**Figure 8. Effects of feedforward capacitance on noise**



at the actual spectral-density plot of the noise voltage (Figure 9). Figure 9 shows that there is minimum noise at the curve of  $C_{FF} = 10 \mu\text{F}$  but that all curves approach this minimum noise curve above certain frequencies. Those certain frequencies correspond to the resonant pole frequencies determined by the R1 and  $C_{FF}$  values. See Table 2 for the calculated  $C_{FF}$  values with an R1 value of 31.6 k $\Omega$ .

**Table 2. Calculated resonant frequencies**

	$C_{FF} = 10 \text{ pF}$	$C_{FF} = 1 \text{ nF}$	$C_{FF} = 100 \text{ nF}$	$C_{FF} = 10 \mu\text{F}$
$f_{\text{Resonant}}$	504 kHz	5.04 kHz	50.4 Hz	0.504 Hz

Figure 9 shows that the curve of  $C_{FF} = 100 \text{ nF}$  rolls off around 50 Hz. The curve for  $C_{FF} = 1 \text{ nF}$  rolls off around 5 kHz, but the resonant frequency for when  $C_{FF} = 10 \text{ pF}$  is obscured by the overall internal effects on the LDO noise. Given these observations of Figure 9, it is assumed for the rest of this discussion that  $C_{FF} = 10 \mu\text{F}$  to minimize noise.

**Effect of the noise-reduction (NR) pin**

$G_{RC}$  decreases when the RC filter capacitor ( $C_{NR}$ ) is used between the NR pin and ground. Figure 10 shows RMS noise as a function of  $C_{NR}$  (see Figure 5). The difference between the two curves is examined later in the third paragraph under “Other technical considerations.”

A wider integration range of 10 Hz to 100 kHz is used in Figure 10 to capture the performance difference in the low-frequency region. With  $C_{NR} = 1 \text{ pF}$ , both curves show very high RMS noise values. Although not shown in Figure 10, there is no RMS noise difference whether  $C_{NR} = 1 \text{ pF}$  or not. This is why  $G_{RC}$  is treated as being equal to 1 in the earlier section, “Amplified reference noise.”

As expected, RMS noise gets lower as  $C_{NR}$  increases, and converges toward the minimum output noise of approximately 12.5  $\mu\text{V}_{\text{RMS}}$  when  $C_{NR} = 1 \mu\text{F}$ .

For a  $C_{FF}$  of 10  $\mu\text{F}$ , the amplifier gain ( $1 + R1/R2$ ) can be ignored. Thus, Equation 8 can be simplified to

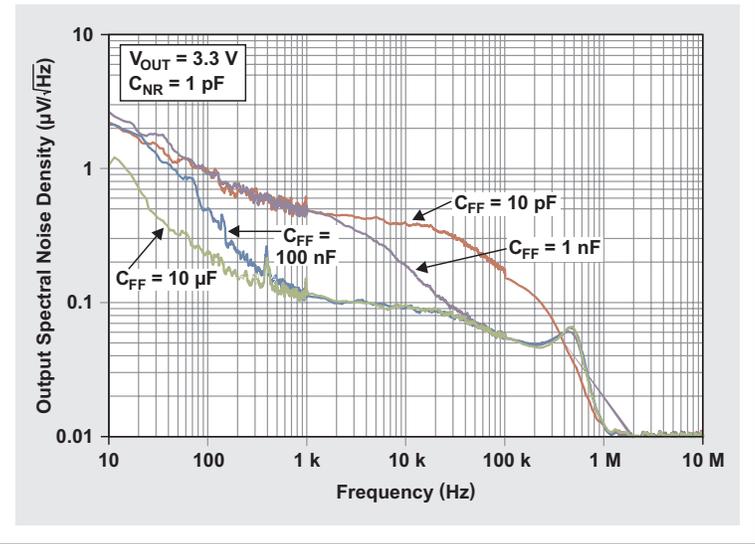
$$V_{N(\text{OUT})} = V_{N(\text{Other})} + V_{N(\text{REF})} \times G_{RC} \tag{10}$$

As seen,  $V_{N(\text{Other})}$  is not affected by  $C_{NR}$ . Therefore  $C_{NR}$  remains 10.5  $\mu\text{V}_{\text{RMS}}$  as was determined by the data-curve fit in Figure 6. Equation 10 can be expressed as

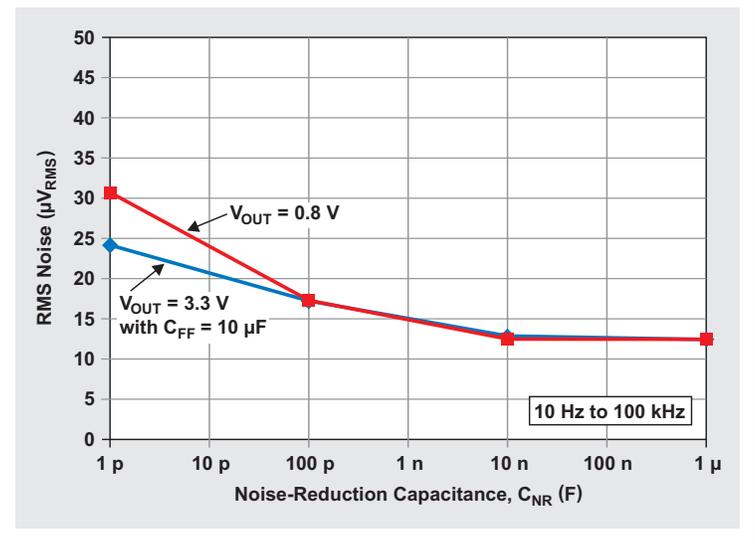
$$V_{N(\text{OUT})} = V_{N(\text{REF})} \times G_{RC} + 10.5 \mu\text{V}.$$

Next, it is important to determine the effect of noise-reduction capacitance on  $G_{RC}$ . The minimum measured

**Figure 9. Output spectral noise density for various  $C_{FF}$  values**



**Figure 10. RMS noise versus noise-reduction capacitance**



noise along the curve in Figure 10 allows Equation 10 to be rewritten as

$$V_{N(\text{OUT})} = 12.5 \mu\text{V} = V_{N(\text{REF})} \times G_{RC} + 10.5 \mu\text{V}, \tag{11}$$

where  $V_{N(\text{REF})} \times G_{RC}$  is solved to equal 2  $\mu\text{V}_{\text{RMS}}$ . Adding  $C_{NR}$  decreases the reference noise from 19.5  $\mu\text{V}_{\text{RMS}}$  to 2  $\mu\text{V}_{\text{RMS}}$ , which is to say that  $G_{RC}$  has decreased from unity to an average of 0.1 (2/19.5) over the frequency range of 10 Hz to 100 kHz.

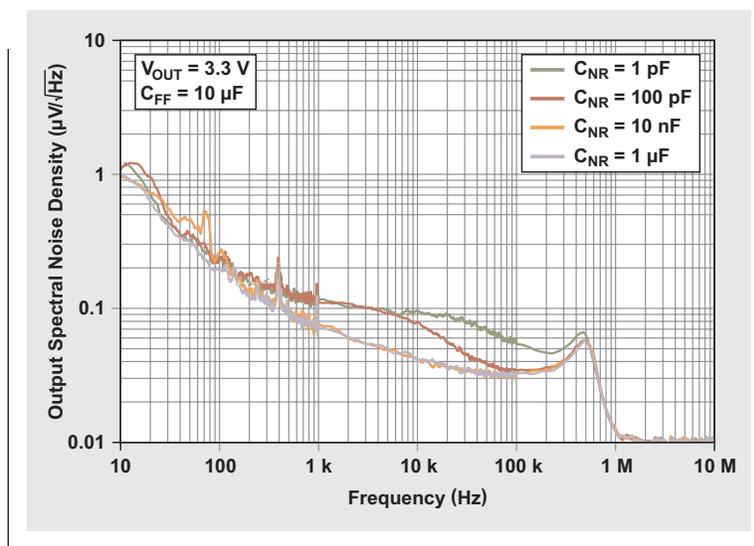
Figure 11 shows how  $C_{NR}$  reduces noise in the frequency domain. Just like the smaller  $C_{FF}$  values in Figure 9, a smaller  $C_{NR}$  starts working at a higher frequency. Note that the biggest  $C_{NR}$  value, 1  $\mu\text{F}$ , shows the lowest noise. Though the curve for  $C_{NR} = 10 \text{ nF}$  shows almost minimum noise close to the curve for  $C_{NR} = 1 \mu\text{F}$ , the 10-nF curve shows a small hump between 30 and 100 Hz.

The curves in Figure 8, where  $C_{NR} = 1 \text{ pF}$ , can be improved to those in Figure 12, where  $C_{NR} = 1 \mu\text{F}$ . Figure 8 shows little difference in RMS noise between  $C_{FF} = 100 \text{ nF}$  and  $C_{FF} = 10 \mu\text{F}$ , but Figure 12 clearly shows a difference.

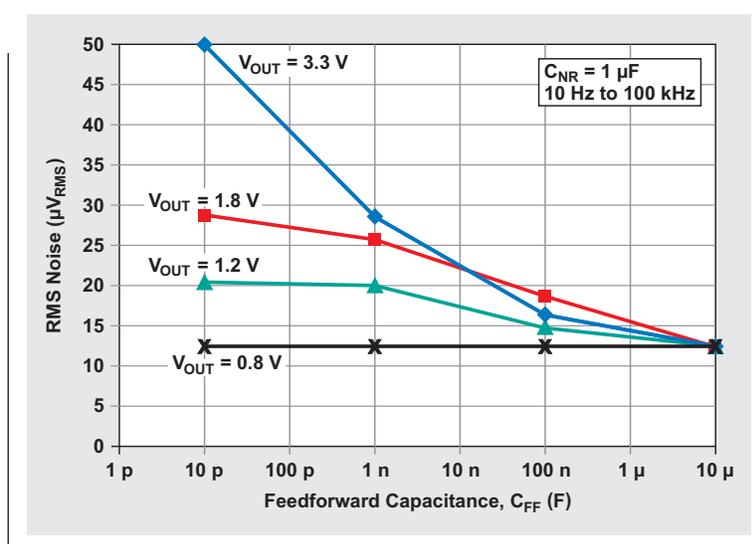
In Figure 12, regardless of the output voltage, values of  $C_{FF} = 10 \mu\text{F}$  and  $C_{NR} = 1 \mu\text{F}$  bring the lowest noise,  $12.5 \mu\text{V}_{\text{RMS}}$ , which is to say that the minimum  $G_{RC}$  value (in other words, the maximum effect of the RC filter) is 0.1. This value of  $12.5 \mu\text{V}_{\text{RMS}}$  is the noise floor of the TI device TPS74401.

When a new LDO device is used for noise-sensitive applications, it is good practice to figure out a noise floor unique to the device by using large  $C_{FF}$  and  $C_{NR}$  capacitors. Figure 12 indicates that an RMS-noise curve converges at the noise-floor value.

**Figure 11. Output spectral noise density versus frequency for various  $C_{NR}$  values**



**Figure 12. RMS noise versus feedforward capacitance after noise optimization**



## Other technical considerations

### Slow-start effect of noise-reduction capacitor

Besides its ability to reduce noise, an RC filter is also known to work as an RC delay circuit. Therefore, a big  $C_{NR}$  value causes a big delay of the regulator's reference voltage.

### Slow-start effect of feedforward capacitor

The same mechanism whereby  $C_{FF}$  bypasses the AC signal across the R1 feedback resistor also bypasses the output-voltage feedback information when  $V_{OUT}$  is ramping up after an enable event. Until  $C_{FF}$  is fully charged, an error amplifier takes a bigger negative feedback signal, resulting in a slow start.

### Why a higher $V_{OUT}$ value results in less RMS noise

In Figures 8 and 10, the curve for  $V_{OUT} = 3.3\text{ V}$  shows less noise than that for  $V_{OUT} = 0.8\text{ V}$ . Since it is known that a higher voltage setting can increase the reference noise, this looks odd. The explanation is that, because  $C_{FF}$  is connected to the OUT node,  $C_{FF}$  has the effect of increasing the output-capacitor value in addition to bypassing the noise signal across resistor R1. Figure 12 shows that, as the reference noise gets minimized, this phenomenon can't be observed.

### RMS-noise value

Because the noise floor of the TPS74401 is  $12.5\text{ }\mu\text{V}_{RMS}$ , this device is one of the lowest-noise LDOs on the market. This absolute value of  $12.5\text{ }\mu\text{V}_{RMS}$  can be a good reference to use in designing a regulator with very low noise.

## Conclusion

The basic noise of an LDO device and how to minimize it have been examined, including:

- How each circuit block contributes to output noise
- How the reference voltage is the dominant source of noise, amplified by an error amplifier

- How to cancel the amplified reference noise
- How an NR function works

Careful selection of a noise-reduction capacitor ( $C_{NR}$ ) and a feedforward capacitor ( $C_{FF}$ ) can minimize LDO output noise to a noise-floor level unique to the device. With this noise-minimized configuration, an LDO device keeps the noise-floor value regardless of the parameters that usually affect noise in non-optimized configurations.

Due to the expected side effect of a slow start when  $C_{NR}$  and  $C_{FF}$  are added to the circuit, values for these capacitors must be chosen that will provide a fast enough ramp-up.

The method described in this article is already being used to optimize the noise of TI's TPS7A8101 LDO. On page 10 of the TPS7A8101 datasheet,<sup>2</sup> the device shows a constant noise value no matter what parameter is changed.

## References

For more information related to this article, you can download an Acrobat® Reader® file at [www.ti.com/lit/litnumber](http://www.ti.com/lit/litnumber) and replace "litnumber" with the **TI Lit. #** for the materials listed below.

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1. "3.0A ultra-LDO with programmable soft-start," TPS74xx Datasheet . . . . .	SBVS066M
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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

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