Basics of debugging the controller area network (CAN) physical layer

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Introduction

The controller area network (CAN) standard continues to grow and is being adapted into many new applications outside of automotive and industrial networking. Microprocessors supporting it have become prevalent at low cost, and open-source protocol stacks make it very accessible and easy to add to new systems. There are CAN boards for BeagleBone (Capes), Stellaris[®] (BoosterPacks), Arduino (Shields), and many other microprocessor development platforms. When a designer's system is powered up and doesn't work, then what? This article presents a sound engineering approach to debugging the CAN physical layer. Basic debugging steps are provided, along with discussion of the expected behavior of a CAN physical layer and tips to help pinpoint the trouble.

Debugging basics

The ISO11898-2 and ISO11898-5 specifications provide details for the high-speed CAN physical layer or transceiver. With a fundamental knowledge of the CAN physical layer, common problems can be found quickly by using simple debugging tools. The basic lab tools needed are an oscilloscope, a digital multimeter (DMM), and a power supply. If the investigation leads to detailed problems, higher accuracy and more complex tools may be required. Problems at that level are outside the scope of this article, but the basics introduced here will help identify areas of concern and what additional tools will be required for further debugging. A CAN demonstration system assembled by Texas Instruments (TI) and TI's SN65HVD255D evaluation module (EVM)¹ are used for the demonstration hardware. A few other helpful items are also used, such as a CAN connector breakout cable and chip hooks to grab the transceiver pins and bring them to a cable for easy attachment to an oscilloscope probe (Figure 1).

Checking the connections

To begin the debugging session, a DMM is used to make sure the connections on the printed circuit board (PCB) are as expected—while the system is *unpowered*. This seems very basic, but it is amazing how many simple problems have been solved with this technique. Everyone assumes that the schematics, layout, and manufacturing are correct, but unfortunately sometimes they aren't. Improperly seated daughtercards, cold solder joints, and cables not terminated or connected properly are all common issues. The resistance setting of the DMM is used to



18

make sure all the traces and connections are properly made. A simplified schematic for a CAN application is shown for reference in Figure 2.

The PCB and network connections to check are summarized in Table 1. The expected resistance between the pins on the transceiver and the relevant other connections on the PCB is 0 Ω , unless the design uses some of the options outlined in the table comments. Examples include current-

Table 1. Summary of PCB and CAN transceiver connections

limiting series resistors, bus-termination resistors, or pullup or pull-down resistors on digital I/Os.

Checking bus termination

Most CAN standards specify a single twisted-pair cable (shielded or unshielded) with 120- Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Termination may be a

CONNECTION	COMMENTS
Ground	The transceiver GND should be connected to the PCB ground plane.
Power Supply (V _{CC} , V _{IO} , V _{RXD})	The V _{CC} on the transceiver should be connected to the voltage regulator's output. One should be careful in multirail designs: The V _{CC} of the transceiver may be 5 V or 3.3 V, depending on the CAN transceiver family. Some 5-V CAN transceivers have an I/O level-shifting pin (V _{IO} or V _{RXD}).
Transmit Data (TXD or D)	If a current-limiting series resistor is used, that is the expected resistance value. The TXD may need a pull-up to the V _{CC} if an open-drain output on a microprocessor is used.
Receive Data (RXD or R)	If a current-limiting series resistor is used, that is the expected resistance value.
Mode	 R_S, S, STB, EN, AB, or LBK may be available, depending on the specific CAN transceiver. R_S provides three modes of operation that need to be checked: 1. <i>High-speed mode</i>. There should be a connection to ground or low from the microprocessor's output pin. 2. <i>Slope-control mode</i>. There should be a pull-down resistor to ground between 10 and 100 kW. 3. <i>Low accurate and a</i>. There should be a logic bick via a pull up resister arvin the output from the microprocessor.
	 Low-power mode. There should be a logic high via a pull-up resistor or via the output from the microprocessor's output pin. The other pins are digital inputs with logic-low and -high thresholds that may be either driven by a microprocessor output or pulled high or low via a resistor. It should be verified that the device is in the proper mode.
V _{REF} or SPLIT pin	Some transceivers may have a V _{CC} /2 output reference. It may be floating, connected by a bypass capacitor to ground, or used to actively drive split termination. The application use should be verified.
CAN Bus (CANH, CANL)	The transceiver's CANH and CANL pins should be connected to the respective pins on the CAN bus. More informa- tion is provided under "Checking bus termination" in this article.

Figure 2. Simplified schematic for a CAN application



19

single 120- Ω resistor at the end of the bus on the cable, as shown on the left side of the CAN bus in Figure 3; or it may be in a terminating node, as shown on the right side of Figure 3. The termination resistance should not be removed from the bus. If the resistive load of the CAN termination is not present, signal integrity will be compromised and the bit timing will not be met. If filtering and stabilization of the bus's common-mode voltage is desired, split termination may be used as in Figure 2. In this figure, each resistor is 60 Ω , and the split capacitor may be anywhere from 1 nF to 100 nF,

depending on the frequency desired for the common-mode filter.² The measured resistance from CANH to CANL should be between 45 and 65 Ω to account for the tolerances within the CAN standard, the parallel impedance of the two termination resistors, and the input resistance of many nodes in parallel. The power rating of the termination resistors should be sized according to the worst-case fault conditions they may encounter, usually the power-supply voltage of the system to ground.

Checking the power supply

Before the system is powered up, the power supply (or supplies) to the CAN transceiver should first be checked. The V_{CC} should be powered with 3.3 V or 5 V, depending on the transceiver type used. Believe it or not, there have been several cases where a missing V_{CC} was the root cause of the problem. Therefore, it should be ensured that the V_{CC} is present at the transceiver's V_{CC} pin. A simple check with a DMM will confirm that power supplies are present. Care must be taken not to short the supply to ground, which unfortunately is a pin next to the V_{CC} pin.

There is approximately a 50-mA difference in current (I_{CC}) needed between the dominant state (~60 mA with a 60- Ω bus load) and the recessive state (10 mA). This 50-mA difference is needed to generate the differential voltage across the termination resistance during the dominant bus state and varies with bus loading. The DMM also may be used in current mode to verify the expected I_{CC} supply currents. Due to the switching nature of CAN, current measured with a DMM is a pseudo-average reading.

A local bypass capacitor of at least 4.7 μ F is recommended to ensure adequate supply buffering during the bus-state transitions. Otherwise, there may be significant voltage-supply ripple caused by the inrush current of the transceiver. An oscilloscope can be used to verify whether the supply voltage is stable or varying with the bus state. It would be undesirable to "starve" the transceiver during the transitions. The transceiver will be protected by its current limiting, but the supply current will be significantly





higher if one of the bus lines is shorted to a supply or ground when the transceiver is trying to drive the bus to a dominant state. If the voltage regulator cannot supply that amount of current, the voltage level may drop out of the transceiver's specification range, or may even be low enough to trip an undervoltage lockout condition on the transceiver.

CAN physical-layer basics

Once all the basics have been checked, the heart of the CAN physical layer—the CAN bus—can be examined. The transceiver's two key components are the receiver and the transmitter. The transmitter is normally called the driver in a CAN. The CAN physical layer is biased with a common-mode point of $V_{\rm CC}/2$, or approximately 2.5 V (Figure 4).





The transceiver translates the single-ended digital logic signals, TXD (or D) and RXD (or R), to the levels required by the differential CAN bus. When the bus is dominant, it has a differential voltage $(V_{diff(D)})$ defined by the CAN standard of >1.2 V at the receiving nodes and is in a logic-low state. When the bus is recessive, it has a differential voltage $(V_{diff(R)})$ defined by the CAN standard of -120 mV $\leq (V_{diff(R)}) \leq 12$ mV at the receiving nodes and is in a logic-high state. Both of these bus states are biased via the common-mode network in the transceiver. The typical bus levels are shown in Figure 5.

To debug the bus, one of the most useful tools is an oscilloscope. While a single-channel scope allows the signals to be seen, a dual- or quad-channel scope is the best. Ideally, TXD, RXD, CANH, and CANL can be seen at the same time to ensure that the transceiver and bus are behaving as expected with respect to each other. For the initial debugging, a low-bandwidth scope is all that is needed, since the CAN is limited to 1 Mbps in the standard. (In the near future this may change, with the introduction of a CAN with flexible data rates.) If the node is transmitting the bitstream of data, the input data can be seen on the TXD input. There is a propagation delay to the differential CAN bus pins (CANH/CANL), followed by another propagation delay to the RXD output. These delays are the loop time, or loop delay, in a CAN. If the node is receiving, then TXD will be idle; but the bus and RXD output will show the CAN frame.

To demonstrate basic CAN-bus operation, Figure 6 shows an oscilloscope with two analog channels and two digital channels, plus a function generator. The CAN bus is made up of two SN65HVD255D EVMs, each with 120- Ω termination set on the bus. The function generator from the scope is connected to the TXD input pin of the top EVM. In Figure 7, digital channel 1 shows the TXD input (light purple); analog channel 1 shows the CANH signal (blue); analog channel 2 shows the CANL signal (yellow); and digital channel 2 shows the RXD signal (green). While

Logic H I Logic L Logic H
Figure 6. Debugging on a CAN bus of two EVMs



Figure 7. TI CAN EVM signals





Figure 5. CAN bus states

the accuracy of this scope is very low, it appears from this simple test that in general the CAN physical layer is behaving as expected.

Figure 8 shows the oscilloscope and probe set up to debug on the TI CAN demonstration system. The nodes are set up in a daisy chain that uses CANopen[®] D-SUB 9-pin connectors. A bus breakout connector is in the upper left portion of Figure 8. It is used to easily connect the analog scope probes to the CANH and CANL pins of the CAN bus and to GND. Because the probes are too large to grab the TXD and RXD IC pins of the middle CAN node, these pins are connected to the digital channels of the scope with chip hooks and a short cable going to the probes. Another option is to solder a small wire to each transceiver pin so the scope probe may be more easily attached.

Figure 9 shows the CAN signals in more detail as captured by the scope. While these signals are not high in resolution or accuracy, they help determine what needs to be known about the operating CAN nodes. The scope was triggered on TXD of the middle node; the CANH and CANL signals are differential as expected; and the acknowledge (ACK) bit with the higher differential voltage is clearly visible at the end of the CAN frame. This higher voltage is the result of multiple CAN nodes generating this ACK bit at the same time in parallel. Another way to easily identify the ACK bit is that it is visible in the RXD signal but not in the TXD signal, which means it was generated by the other nodes as it should be.

CAN debugging examples

Figure 10 shows a CAN demonstration system where the CANH trace leading to the daisychain output has been broken on the righthand PCB. This occurred because a mounting bolt on the rear of this system had rubbed against the PCB while the system was being carried around the world over a number of years. When this system was connected to other CAN nodes via this daisy-chain bus connection, it didn't work.

Figure 8. Debugging on the TI CAN demonstration system



Figure 9. TI CAN demonstration system's signals



Figure 10. CAN demonstration system with broken CANH trace



22

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The CANH signal in Figure 11 shows the result of this broken PCB trace. A DMM continuity check also confirmed the open circuit.

Figure 11 also highlights in detail another important part of the CAN frame, the ACK bit. The scope was used in single mode and triggered on the TXD pin of the righthand node until a trigger on a single bit was found. This single bit is the ACK bit generated by this node to acknowledge that a valid CAN frame was received. All receiving nodes acknowledge the CAN frame from the sending node. The ACK bit seen on the bus has a slightly longer bit time than the transmitted ACK bit seen on TXD. This is an artifact of the multiple nodes transmitting ACK bits at the same time. Factors affecting this longer bit time are a 5-ns/m delay through the cabling; clock timing drift between the three CAN nodes; and the higher bus differential voltage resulting from two nodes transmitting an ACK bit concurrently. If these factors cause the ACK bit (slot) to become too long and to remain dominant in the ACK delimiter, it may cause a CAN error frame.

Another example of CAN bus debugging was a system where only very slow CAN data rates (bit timings) would work. Connecting an oscilloscope to the TXD pin showed very slow rise times on the TXD input (Figure 12). The 9.6-µs timing delay was equivalent to 10 bits at a CAN data rate of 1 Mbps. This discovery led to the root cause: A microprocessor with an open drain was being used to drive the transceiver's TXD pin. In this case there was no real drive to the logic-high level. Only the weak internal pullup of the CAN transceiver was bringing the TXD pin high, so it had a very long RC time constant. This problem was easily solved by adding a pull-up resistor on the TXD pin.







23

Conclusion

The basics of the CAN physical layer and the debugging examples presented in this article should ease any fear of jumping into the CAN world. With the additional references provided here and the appropriate datasheets, designers should have their CAN systems up and running in no time.

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