

How to simplify AFE filtering via high-speed ADCs with internal digital filters

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Introduction

Traditional designs for industrial data-acquisition often require elaborate filtering on the analog front end (AFE) in front of the analog-to-digital converter (ADC). An analog filter's primary objective is to attenuate unwanted out-of-band signals that can alias on top of the desired signal of interest—so the analog filter is also known as an anti-alias filter (AAF). Unwanted signals and noise in the alias band can originate from the driving amplifier, power-supply switching spurs or even intentional interferers (jammers).

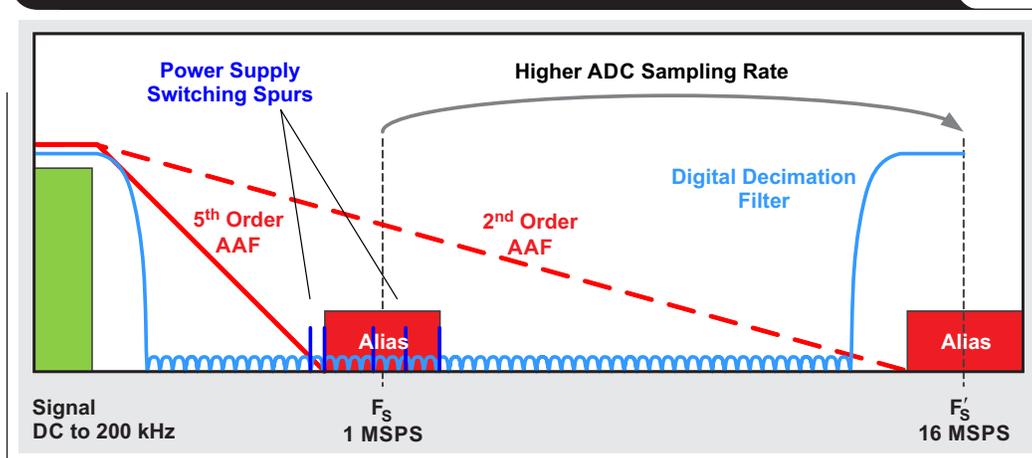
The alias frequency location directly depends on the ADC sampling rate—the faster the data converter can operate for a given instantaneous bandwidth, the further away the alias band gets from the desired signal, and the easier filtering becomes. In very high precision systems, designers often exploit this relationship by using delta-sigma ADCs—which by design use high oversampling rates along with decimation filters. In cellphone base stations, the push for direct radio-frequency sampling of the 3GPP bands from 1 to 6 GHz drove the adoption of gigasample-per-second (GSPS) data converters. The instantaneous bandwidth of the 3GPP bands are only a

fraction of the sampling rate, thus the new architecture of using oversampling GSPS converter also relaxed the requirements for the analog RF filter.

Industrial applications using successive approximation register (SAR) ADCs—such as power quality analysis, sonar or industrial radar with sampling rates between 1 MSPS to more than 10 MSPS—fall in between precision delta-sigma and GSPS ADC. The new ADC35xx and ADC36xx families of high-speed SAR ADCs are coupled with an integrated digital filter, enabling industrial applications to take advantage of this oversampling and decimation design technique in order to relax external analog filter requirements.

For the example shown in Figure 1, assume that the DC input signal is 200 kHz with an ADC sampling rate of 1 MSPS. A passband of around 300 kHz together with an alias rejection of around 40 dB requires approximately a fifth-order filter. By increasing the ADC sampling rate from 1 MSPS to 16 MSPS, the alias frequency band gets pushed out from 800 kHz to 15.8 MHz and therefore reduces the anti-alias filter to a second-order filter. Additionally, the alias band shifts away from the frequency region (600 kHz to 2 MHz), which often contains spurs from switching regulators in the power supply.

Figure 1. Anti-alias filter relaxation due to increased ADC sampling rates



Internal digital filter

The next objective is to examine the three purposes of the internal digital filter.

1. Attenuation of the alias frequency band

The most common digital decimation filter in the frequency domain is a digital low-pass filter. This filter consists of three different regions: the passband, the multiple transition bands and the alias bands, as shown in Figure 2. Any signals in the alias bands will alias on top of the passband but will be attenuated by around 85 dB or more in this figure. All three alias bands mirror around $F_S/8$, $F_S/4$ and $3 F_S/8$.

2. Output data-rate reduction

A high oversampling rate can be hard to handle for downstream processors. Furthermore, in an oversampling configuration, most of the frequency spectrum only contains unwanted content, which expends unnecessary energy to transmit. The digital filter discards samples and reduces the output data rate.

When the band of interest is not in the low-end frequency range, a digital mixer can downconvert the signal before low-pass filtering in order to maximize the reduction in output rate.

3. SNR improvement

The signal-to-noise ratio (SNR) of a data converter is calculated by integrating the noise floor across the ADC's Nyquist zone. In theory, the ADC SNR improves by 3 dB for every factor of 2 digital decimation. In reality, it is possible to get close to 3 dB until in-band noise starts to dominate.

In the earlier example, the ADC sampling rate increased from 1 MSPS to 16 MSPS. Adding a decimate by 16 digital filter would reduce the output rate back to 1 MSPS while increasing the ADC SNR by as much as 12 dB (4×3 dB).

Noise spectral density (NSD) is another measure of data-converter noise performance. It takes the SNR and bandwidth into consideration and is often used to compare different data converters. For example, a 16-MSPS ADC with an SNR of 82 dB would have an NSD of -151 dBFS/Hz [82 dB + $10 \times \text{LOG}$ (8 MHz)]. After decimation by a factor of 16, the SNR improves by 12 dB (from 82 to 94 dB), while the NSD stays constant at -151 dBFS/Hz [94 dB + $10 \times \text{LOG}$ (0.5 MHz)].

Understanding the decimation filter

Several trade-offs determine the architecture of the digital filter and the number of filter taps: programmable vs. fixed coefficients, the maximum passband ripple, the minimum stop-band attenuation, latency and power consumption. For example, a sharper filter roll-off and more stop-band attenuation require a higher number of filter taps, resulting in higher power consumption and longer latency. The filter coefficients determine whether the filter gives a low-pass, high-pass or band-pass frequency response.

When integrating a digital filter with a high-speed data converter, a finite impulse response (FIR) half-band low-pass filter is most commonly used by ADC designers because its design is inherently very power efficient. Half band means decimation by 2; every other coefficient is zero, and these coefficients don't use any computational power. Non-zero coefficients are symmetrical around the center of the impulse response.

Figure 2. Decimation filter regions in the frequency domain

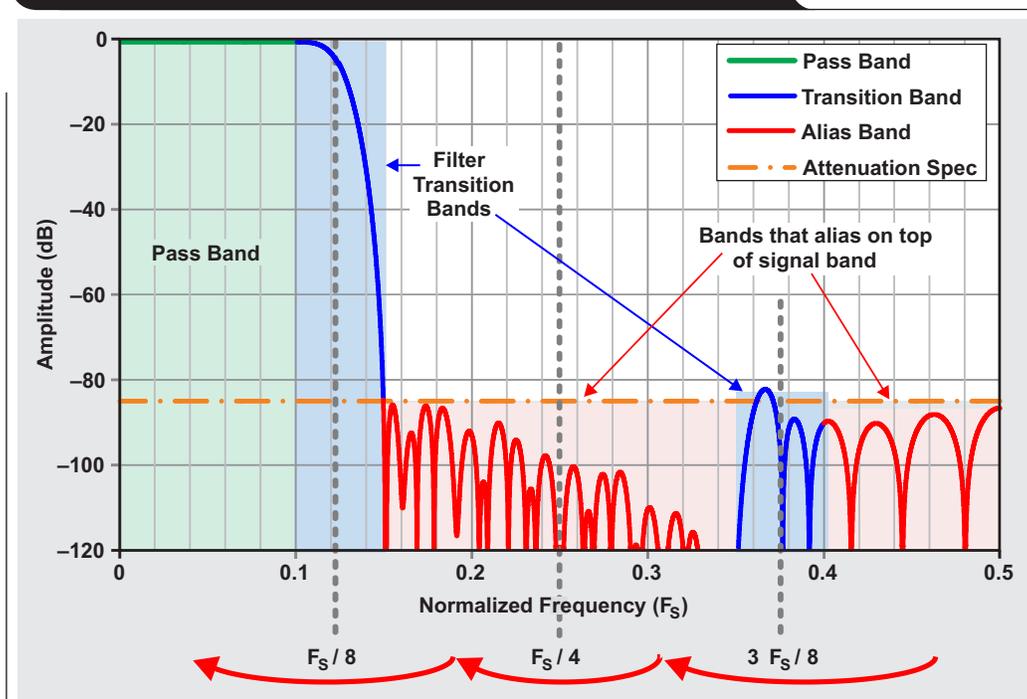


Figure 3 shows a generic FIR implementation. In a half-band implementation with seven taps/coefficients ($N = 7$), all even taps (h_2, h_6) except h_4 are zero, which reduces seven multiplications to five. For higher decimation rates, half-band filters are concatenated.

In theory, a low-, high- or band-pass filter could be integrated with the ADC; however, a low-pass filter is the most practical choice, especially when adding a complex mixer to build a digital tuner.

Note that the digital filter sits after the analog-to-digital conversion. Therefore, the digital filter can't prevent intended or unintended jamming of the receiver where the ADC gets driven into saturation. It is important to still use external filtering and adjustable gain to prevent overloading of the ADC.

Complex decimation—digital tuner

Adding a complex mixer [using $\cos(\omega t)$ and $\sin(\omega t)$ for I/Q output] turns the two digital low-pass filters into a tunable digital band-pass filter as can be seen in Figure 4. The mixer uses a numerically controlled oscillator (NCO) as the local oscillator (LO). Both the “I” path and the “Q” path are real low-pass filters in the frequency domain. The phase difference between sine and cosine cancels the positive/negative frequencies. The digital mixer shifts any frequency within the positive or negative Nyquist zone to zero Hertz, thus creating a very powerful tunable band-pass filter—while also replacing a traditional analog mixer.

Figure 5 illustrates the process of digital tuning. The Nyquist zone of the ADC shows the input signal (F_{IN})

Figure 3. Implementation example of a FIR design

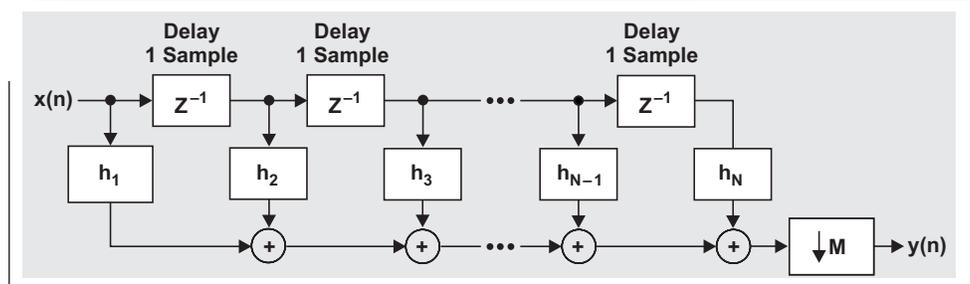
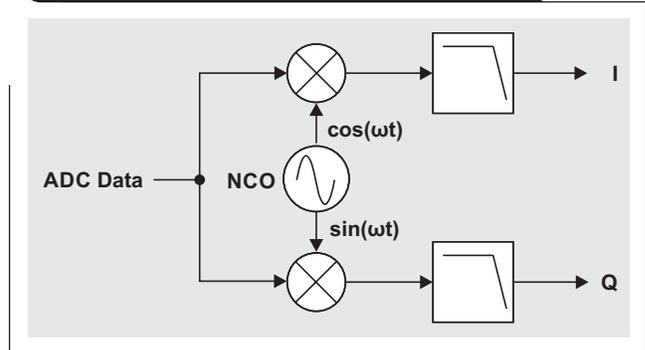
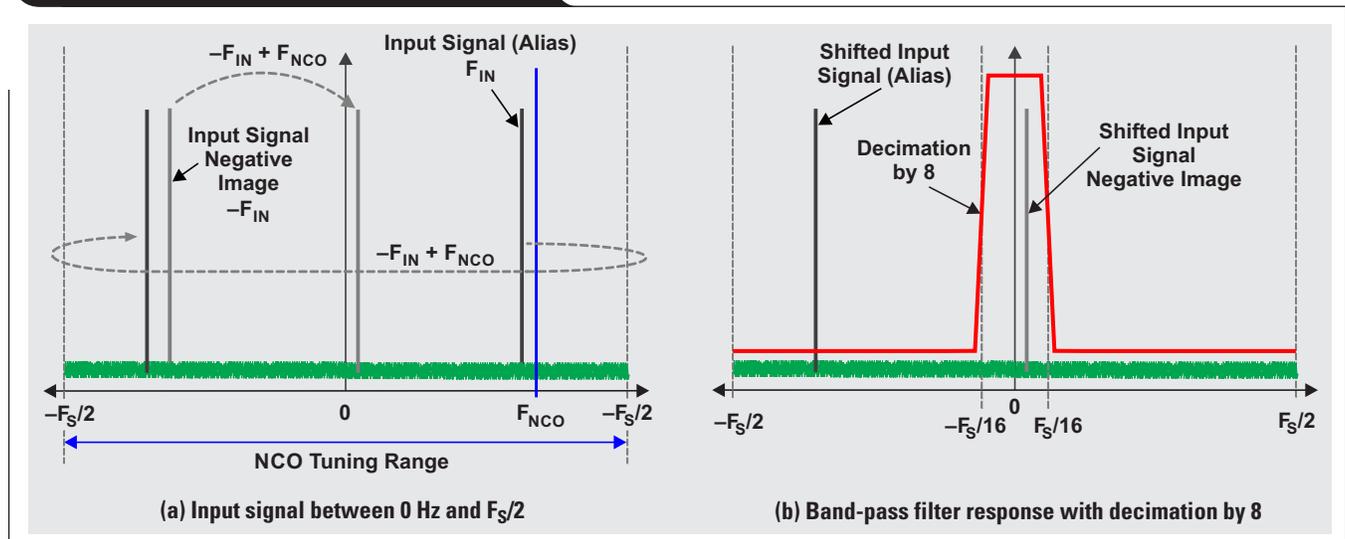


Figure 4. Block diagram of a complex decimation filter



between 0 Hz and $+F_S/2$. The negative image of that input signal ($-F_{IN}$) is located between 0 Hz and $-F_S/2$. Both the input signal and its negative image are mixed with the NCO frequency ($+F_{NCO}$ in this example). $+F_{IN}$ rotates to the negative Nyquist zone while $-F_{IN}$ rotates to the positive Nyquist zone. The example shows a band-pass filter response with decimation by 8 centered at 0 Hz, which passes the $-F_{IN}$ frequency mixed with the NCO frequency ($F_{OUT} = -F_{IN} + F_{NCO}$).

Figure 5. Illustration of complex filtering



Practical examples

In time-domain applications, a digital low-pass filter can remove higher-frequency noise on the input signal. When sampling a pulse-shaped waveform, the low-pass filter will remove higher-order harmonics, thus slowing down the edge rate of the pulse.

In frequency-domain applications such as radar, the integrated decimation filter becomes a very powerful feature for the reasons outlined earlier in this article. Further illustrated in Figure 6, the input signal F_{IN} is sampled with $F_S = 65$ MSPS, followed by complex decimation by 8 and an NCO frequency of 5.5 MHz.

Conclusion

In an effort to reduce the size of the printed circuit board and bill-of-materials cost, designers are looking to replace analog circuits with digital logic/intellectual property (IP). High-speed SAR data converters with integrated digital filtering like those in the ADC35xx and ADC36xx families are a good fit for a wide range of industrial applications. Similar to a delta-sigma converter, these ADCs ease analog filter constraints with a higher oversampling rate combined with integrated digital filtering. The complex mixer can also remove an analog mixing stage, further simplifying the analog front end signal chain.

Related Web sites

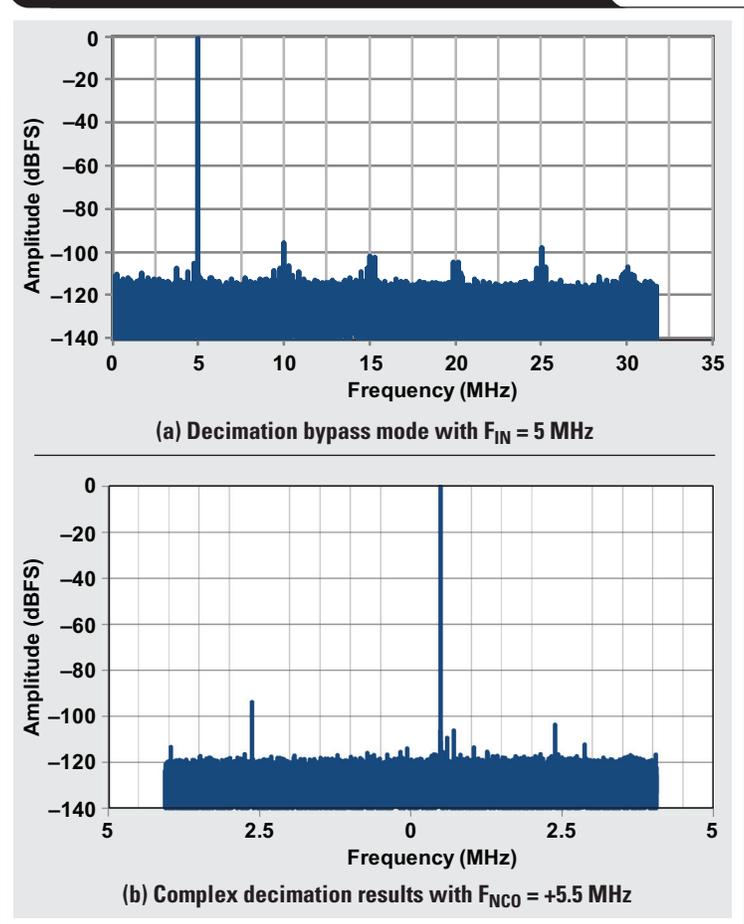
Product information:

[ADC3541](#)

[ADC3643](#)

[ADC3660](#)

Figure 6. Performance example of integrated decimation filter with $F_S = 65$ MSPS



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