

Clutter-free power supplies for RF converters in radar applications (Part 1)

By Rob Reeder, Applications Engineer, High-Speed Data Converters

Neeraj Gill, Applications Engineer, High-Speed Data Converters

Introduction

When looking for noise sources, power-supply pins are also considered inputs, and all active devices have them. In today's practical designs, power pins should be considered when designing in the radio-frequency (RF) domain. Noise and coupling on any power-supply input can cause substandard performance in radar applications because of the additional clutter.

Although the focus in this article is on data converters—particularly RF converters sampling in the gigahertz region—the principles discussed here are applicable to all integrated circuits, including fully differential amplifiers, mixers, low-noise amplifiers, gain blocks, RF switches and digital step attenuators in an application signal chain at low or high frequencies.

Essentially, the analog-to-digital converter (ADC) is a giant mixer; whatever is at the input will convolve to its output spectrum. This is true for any input. It may be assumed that “leaky noise,” also known as white noise or spurs, only comes from the clock or analog inputs, or both. For applications like advanced radar systems, though, the switch-mode power supply (SMPS) can also leak noise and wreak havoc on spectral performance.

Low-dropout regulators (LDOs) are commonly used to reduce the noisy bus-rail voltage that enters the system

board, which biases the various portions of the ADC.

However, this isn't always the most practical method when the component size and efficiency trade-offs are considered. Instead, some SMPS technologies can be adapted to these applications with a more in-depth understanding of the SMPS output noise.

This first installment of a two-part series describes what happens when noise couples onto the ADC's supply, how it might couple through the ADC's circuitry, and some common power-supply trade-offs.

Power-supply noise coupling

A noisy sampling clock provided to the ADC will ultimately prove disastrous for ADC performance. There are many papers written about this, so the following is just a high-level explanation. When a clock is considered sub-par, the ADC will deviate from its data-sheet specifications in signal-to-noise ratio (SNR) and noise spectral density. As illustrated in Figure 1, the fast-Fourier transform spectrum overlay shows the difference between a jittery clock and clean sampling clock applied to the ADC. Notice the degradation in the SNR of ~3 dB when using a sub-par sampling clock. This degradation drastically reduces the total dynamic range of the system.

Figure 1. Comparison of noisy vs. clean sampling clock

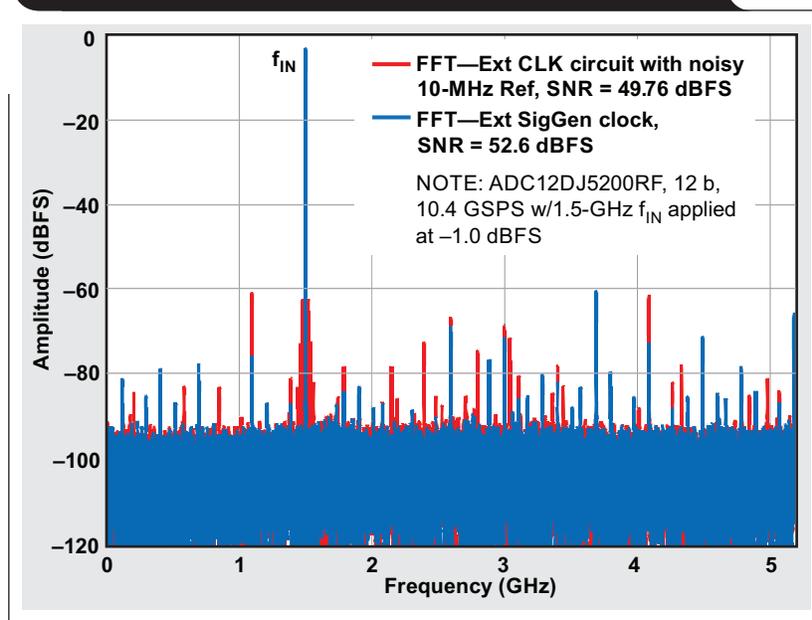
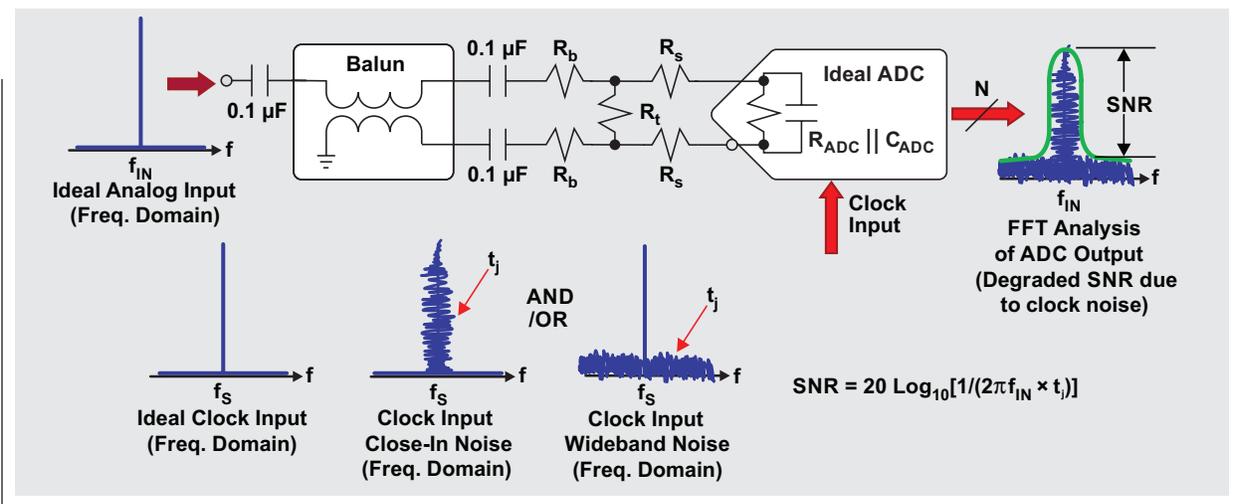


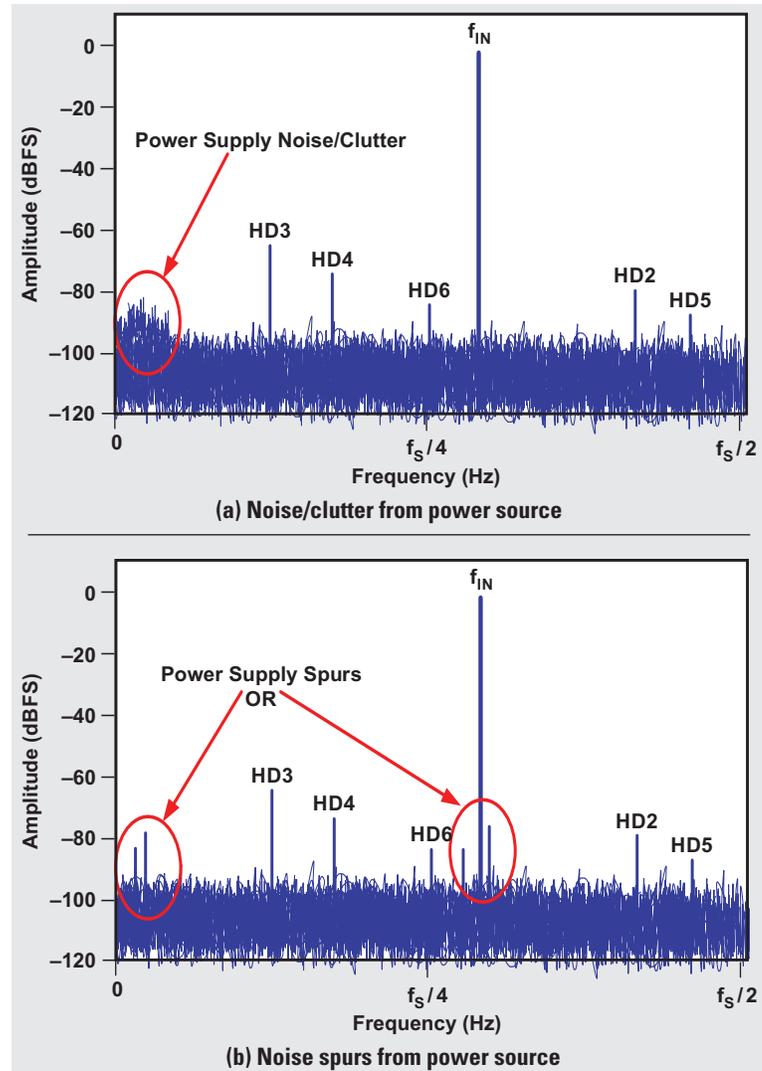
Figure 2. wideband or close-in noise coupled to the ADC's output spectrum from the clock inputs



To illustrate this a bit more, if the clock has any wideband or close-in noise, then either noise can be a component evident in the output spectrum. This is illustrated in Figure 2. Earlier, it was suggested that the ADC be thought of as a giant mixer; even if the ADC is ideal, any noise that couples only to the clock in either a wideband or close-in fashion will ultimately convolve to the output spectrum.

It is possible to apply the same concept to the power-supply input as well. By shifting the fundamental frequency (f_{IN}) down to DC, as shown in Figure 2, any wideband noise or close-in noise near DC will convolve to the output spectrum. See Figure 3.

Figure 3. Wideband or close-in noise coupled to the ADC's output spectrum from the power inputs



There is a slight difference in how noise couples through the clock versus how noise couples through the power-supply pins. In the clock example, the internal circuitry of the clocking nodes is well-tied into the sample-and-hold structures of the analog inputs. This makes it a perfect place for any noise or coupling through the clock pins to find their way into the internal signal path of the ADC as was shown in Figure 2. The coupling path is almost zero attenuation in this case.

Notice that the internal circuitry of the ADC shown in Figure 4 includes an attenuation symbol. This symbol represents the ADC's rejection of any noise or signal coupling through the power pins, which is measured as the power-supply rejection ratio (PSRR). Ultimately, this attenuation defines the amount of coupling rejection, or PSRR, from the internal circuit design inside the ADC. Some circuit design topologies allow less noise attenuation than others, and therefore, more noise leaks into the ADC's digitization path, degrading the performance of the ADC. Figure 5 illustrates two different circuit structure examples.

The type of structure shown in Figure 5a gives better attenuation to noise and coupling, (and thus better PSRR) because of the high-isolation metal-oxide semiconductor construction connected to the power supply rail. The

circuit in Figure 5b offers less attenuation to noise because of its simple resistive pull-up design.

Parasitics are another factor that distinguishes good and bad PSRR tolerance. Smaller process geometries and lower supply ranges are used today in many ADC designs, as well as many other devices. In turn, these geometries give rise to smaller voltage thresholds, which become more sensitive to noise.

Figure 4. Example of power-supply attenuated coupling path

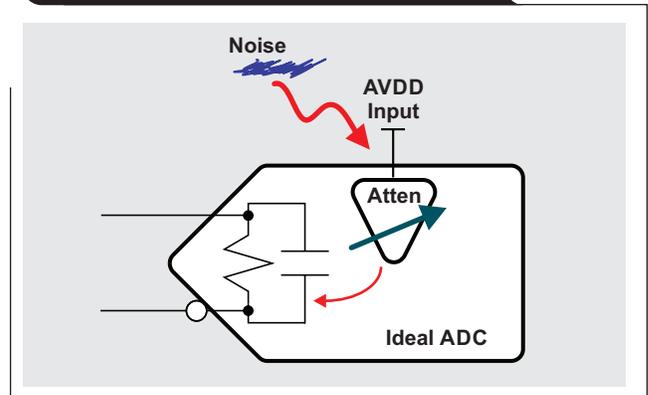
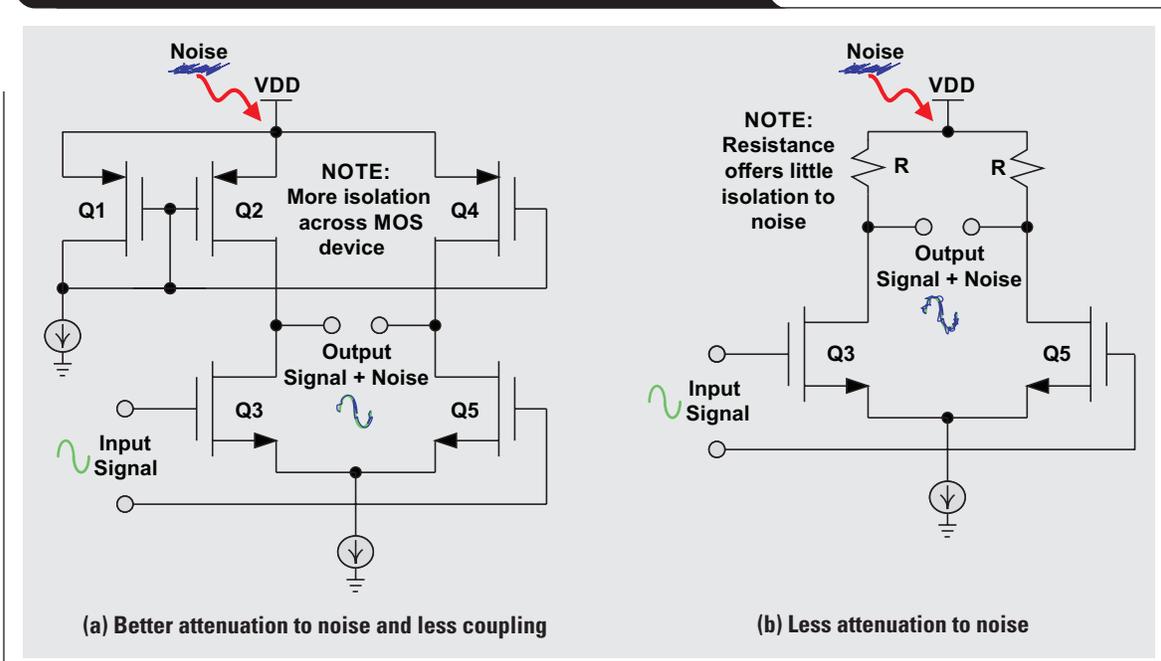


Figure 5. Generic examples of internal ADC circuit structures connected to a power-supply pin



Power-supply trade-offs: SMPSs vs. LDOs

Since high-speed ADCs are sensitive to power-supply noise, one popular method to minimize noise is to design with a switch-mode power supply (SMPS) to knock down the main bus-rail voltage available in the system (28 V or 15 V, for example). The SMPS provides a mid-rail voltage where the LDO can provide a clean voltage to the appropriate ADC power domain. See Figure 6.

An SMPS design, when compared to a linear supply, has

several advantages. The reduction in power loss translates to a better, more efficient solution. Less power dissipation from the power losses that build up in the numerous LDOs' voltage drops across the board, coupled with the size of the overall SMPS power-supply circuit, translate to more available PCB real estate. Using an SMPS alone does require careful consideration of the switching supply selected, filtering, and circuit design layout to achieve the chosen results, but it is possible. See Figure 7.

Figure 6. An SMPS and LDO design for the ADC12DJ5200RF evaluation module (EVM)

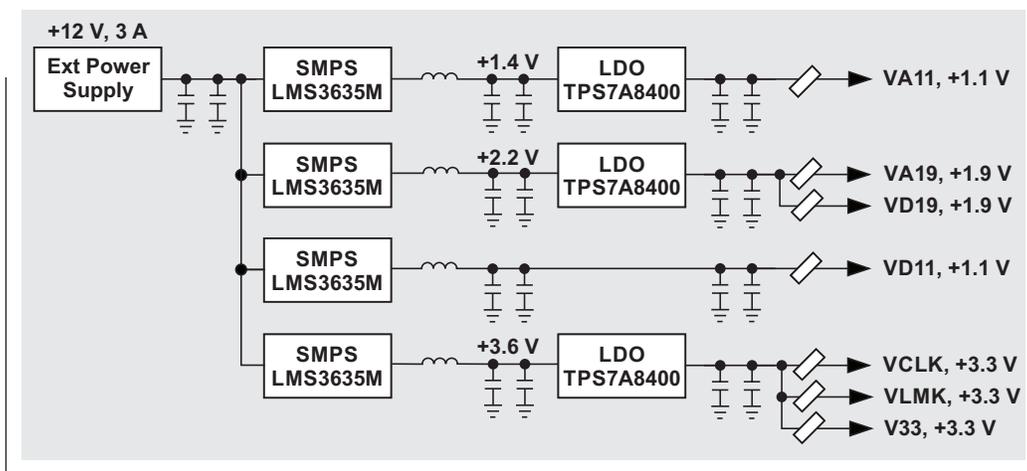


Figure 7. An SMPS-only design for the ADC12DJ5200RF EVM

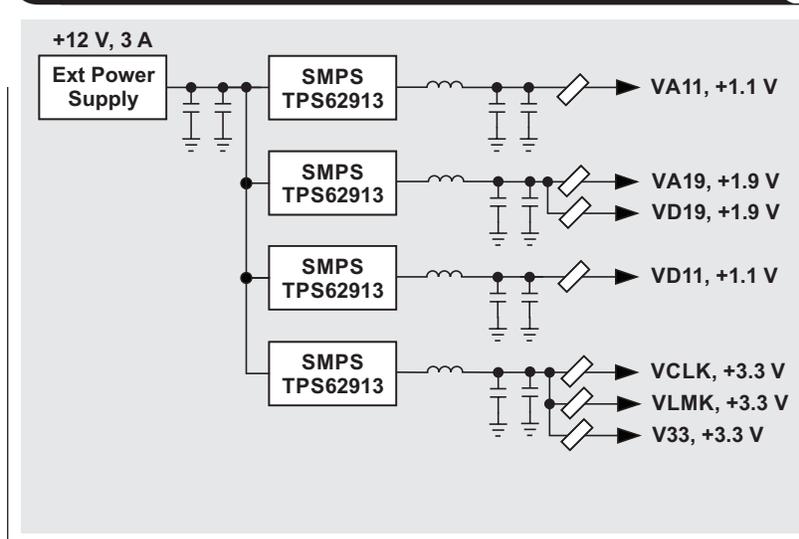
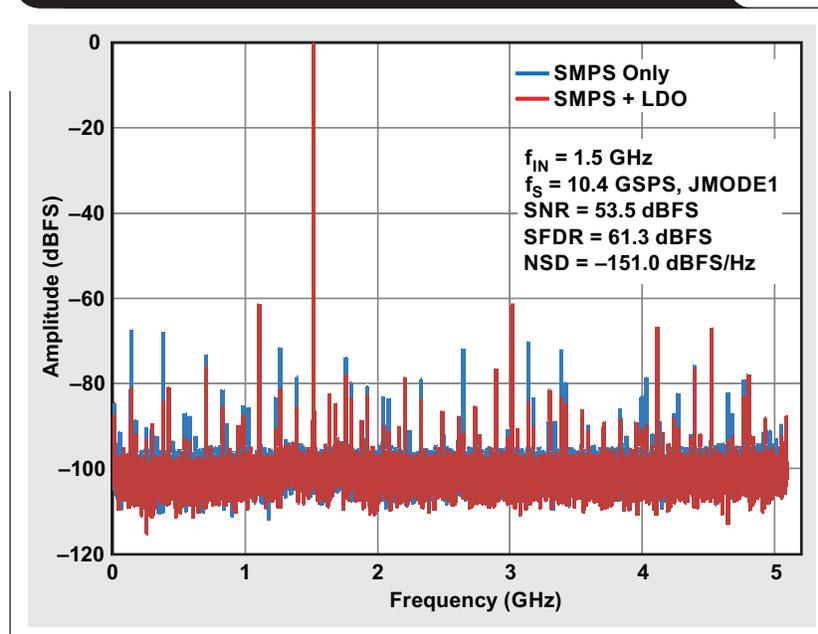


Figure 8. ADC12DJ5200RF AC performance comparison



As shown in Figure 8, the ADC's AC performance (SNR/SFDR) is on par between the two power supply designs as an analog input frequency of 1.5 GHz is applied while sampling at 10.4 GSPS. This basic test instills confidence that the SMPS design is robust and realizable.

Conclusion

New technology breakthroughs in power IC designs have given way to SMPS-only approaches, enabling the use of this methodology in many noise-sensitive applications such as radars and high-end instrumentation. The TPS62913 low-ripple and low-noise buck converter was used in this article to show the differences between these trade-offs. This buck converter was specifically designed to help power supplies be designed to meet the noise and ripple requirements of high-speed, noise-sensitive applications.

A Part-2 follow-up article will define and measure PSRR and the power-supply modulation ratio using the 12-bit ADC12DJ5200RF RF-sampling ADC, and provide an example of how to properly make power-management trade-offs.

Related Web sites

Rob Reeder and Steve Schnier, "Powering Sensitive ADC Designs with the TPS62913 Low-Ripple and Low-Noise Buck Converter," Application Report (SLVAEW7), September 2020.

High-Speed Data Converter Pro software, Texas Instruments Design Resources.

Product information:

ADC12DJ5200RF

LMS3635-Q1

TPS7A84

TPS62913

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