Application Report

SNAA023A – May 2004 – Revised April 2013

AN-1275 Optimizing LMX243x Input Sensitivity Using Simple Matching Techniques

ABSTRACT

The following application report describes how maximum power can be delivered from the voltage controlled oscillator (VCO) output to the FinRF input of a LMX243x frequency synthesizer by means of performing a single element match.

Contents

List of Figures

List of Tables

1 Overview

Maximum power transfer is achieved by designing a matching network that transforms the FinRF input (load) impedance to an impedance that is equivalent to the VCO output (source) impedance. In most applications, the VCO has an output impedance equivalent to 50 Ω. Furthermore, the trace impedance of the printed circuit board (PCB) is typically designed to be 50 Ω. This means that the matching network should be designed to transform the FinRF input impedance to 50 Ω. Figure 1 demonstrates the principal of impedance matching (transformation). The VCO output is represented as a Thevenin equivalent of a voltage source and a 50 Ω series resistance.

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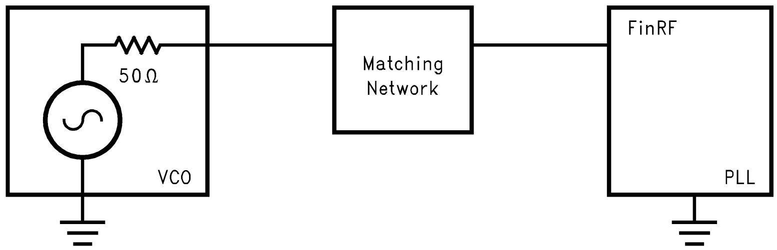

Figure 1. Impedance Matching

A typical plot for the LMX243x UTCSP FinRF input impedance is illustrated in Figure 2. The Smith chart shows that for frequencies less than 3400 MHz, the reactance is primarily dominated by the capacitance from the PCB and CSP package. On the other hand, for frequencies greater than 3400 MHz, the reactance, for the most part, becomes dominated by the internal lead inductance from the package bond wires. It's worth mentioning that the FinRF input impedance is very dependent upon the type of package used.

Ideally, a perfect match is preferred everywhere within the FinRF input's range. This means that the matching network designed should be able to 'tune out' the effects of the package capacitance at the lower frequencies, as well as the effects of the lead inductance at the higher frequencies. In practice however, since the load is comprised of imaginary elements, which are frequency dependent, the perfect match can only occur at one frequency. Therefore, the matching network is only optimized for a particular frequency. In the case of PLLs, this corresponds to the VCO output frequency, f_{FinRF}.

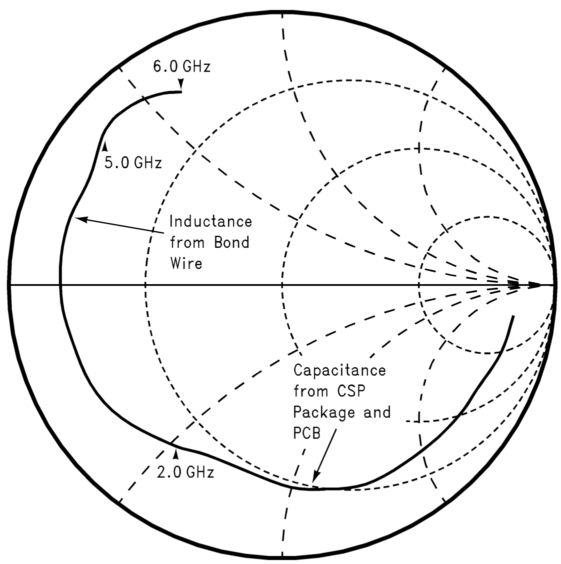

Figure 2. LMX243x UTCSP FinRF Input Impedance

2 Evaluation Methodology

To keep the matching network simple and to demonstrate that indeed an improvement in performance is achieved, a single element match is used. In order to assess the improvement achieved, the device's input sensitivity level is determined before and after the matching network is included. Therefore, an open loop sensitivity test is implemented. The purpose of this test is to measure the acceptable signal level to the FinRF input of the PLL. Outside the acceptable signal range, the feedback divider begins to divide incorrectly and miscount the frequency. Minimum sensitivity is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz.

In most applications, the lower sensitivity limit is of concern because it determines the minimum acceptable signal level that is required to maintain lock. The objective of the matching network, therefore, is to push the lower sensitivity limit downwards. This means that at the particular frequency of interest, the VCO output frequency, the matching network should improve the FinRF input sensitivity.

Furthermore, a good match should also improve the frequency response of the PLL. In most applications, it is desirable to increase the upper frequency limit, push the sensitivity curve further right. In most cases however, as seen with the LMX243x UTCSP, this is difficult to achieve due to internal circuit limitations.

To demonstrate the discussion above, several examples are provided here.

3 1.0 Optimizing Sensitivity at 5.0 GHz

Suppose the requirement is to optimize the performance at 5.0 GHz for an LO to be used in a particular 802.11a WLAN application. According to Figure 2, the FinRF input impedance lies on the upper half of the Smith chart. This means that the FinRF input impedance at 5.0 GHz can be represented by a series combination of a resistor and an inductor. From the Table 1, ZFinRF = 4.92 + j19.79Ω at 5.0 GHz.

To move closer to 50 Ω and to an ideal match, a 1.0 pF shunt capacitor is placed between the VCO output and the FinRF input of the PLL as shown in Figure 3. The closer the impedance gets to 50 Ω, the better the sensitivity is. The impedance at 5.0 GHz is then illustrated in Figure 4.

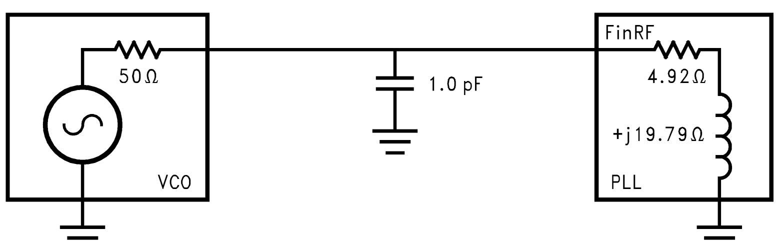

Figure 3. 1.0 pF Shunt Match at 5.0 GHz

The capacitor used should exhibit a self resonace frequency that's higher than the frequency of interest. High Q (low ESR), temperature compensating (NPO) ceramic capacitors are recommended here. Today, it is not too difficult to find 1.0 pF capacitors that have self resonance frequencies well above 5.0 GHz, such as the 600S series capacitors from American Technical Ceramics.

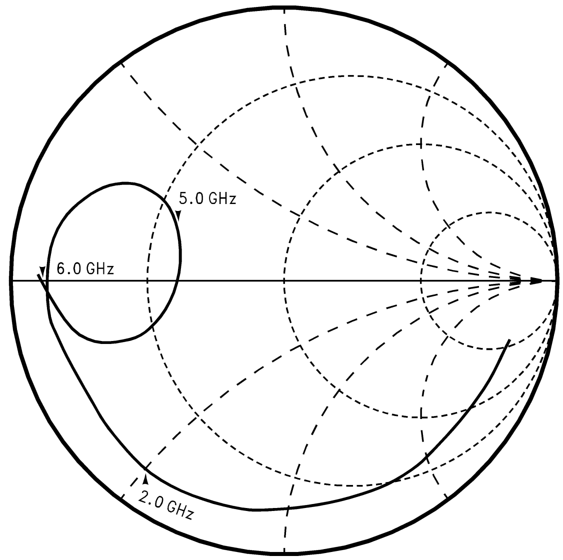

Figure 4. LMX243x UTCSP FinRF Input Impedance With 1.0 pF Shunt Match

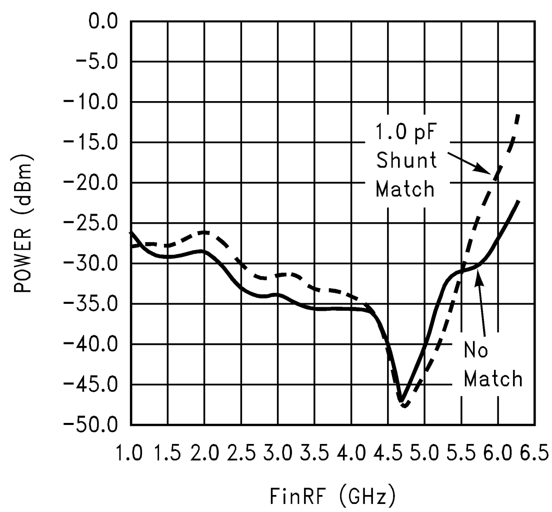

Figure 5. LMX243x UTCSP FinRF Input Sensitivity Improvement at 5.0 GHz

Figure 5 shows that an approximate 3.4 dB improvement in sensitivity is achieved at 5.0 GHz with the addition of the 1.0 pF shunt capacitor. Figure 5 also demonstrates that the sensitivity gets worse at frequencies other than 5.0 GHz. This evaluation is performed under typical conditions, with V_{CC} = 2.50 V and T_A = 25°C.

NOTE: A DC blocking capacitor is typically included at the PLL's FinRF input. For all the evaluations performed in this document, the impedance and loss characteristics of the DC blocking capacitor are included in the calibration and removed from any test results.

4 2.0 Optimizing Sensitivity at 6.0 GHz

Now suppose the requirement is to optimize the performance at 6.0 GHz for an LO to be used in a particular cordless phone application. According to Figure 2, the FinRF input impedance again lies on the upper half of the Smith chart. From Table 1, ZFinRF = 7.11 + j28.00Ω at 6.0 GHz.

This time a 0.5 pF shunt capacitor is placed between the VCO output and the FinRF input of the PLL as shown in Figure 6. This makes the impedance at 6.0 GHz close to 50 Ω as illustrated in Figure 7.

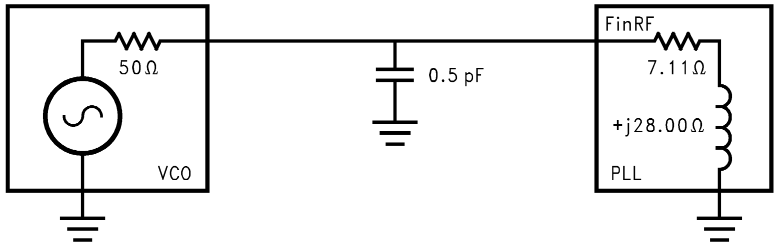

Figure 6. 0.5 pF Shunt Match at 6.0 GHz

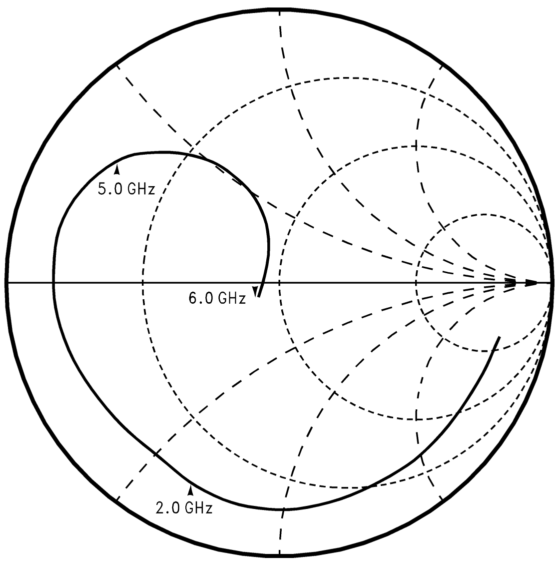

Figure 7. LMX243x UTCSP FinRF Input Impedance With 0.5 pF Shunt Match

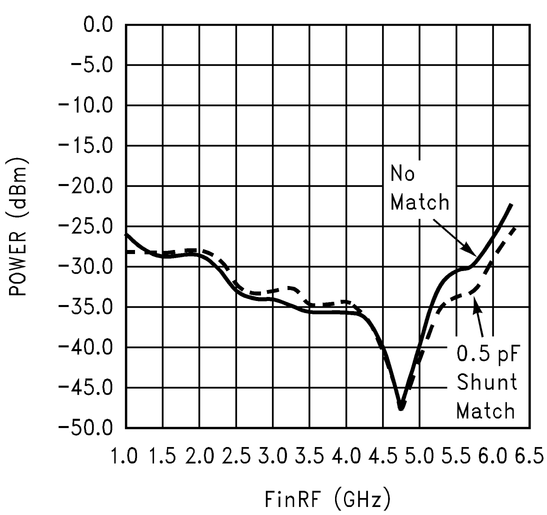

Figure 8. LMX243x UTCSP FinRF Input Sensitivity Improvement at 6.0 GHz

Figure 8 shows that an approximate 3.0 dB improvement in sensitivity is achieved at 6.0 GHz with the addition of the 0.5 pF shunt capacitor. Again, this evaluation is performed under typical conditions, with V_{CC} = 2.50 V and T_A = 25°C.

NOTE: The LMX2434 is only guaranteed for operation up to 5.0 GHz. For further information, see the LMX2430/33/34 data sheet.

5 3.0 Optimizing Sensitivity at 2.0 GHz

Now suppose the requirement is to optimize the performance at 2.0 GHz for an LO to be used in a particular US TBQM handset application. Figure 2 now shows that the FinRF input impedance lies on the lower half of the Smith chart. From Table 1, ZFinRF = 14.32 - j38.66Ω at 2.0 GHz.

To move closer to 50 Ω and to an ideal match, a 4.7 nH series inductor is placed between the VCO output and the FinRF input of the PLL as shown in Figure 9. The impedance is then illustrated in Figure 10.

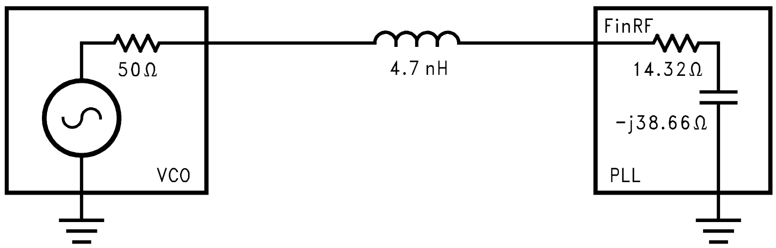

Figure 9. 4.7 nH Series Match at 2.0 GHz

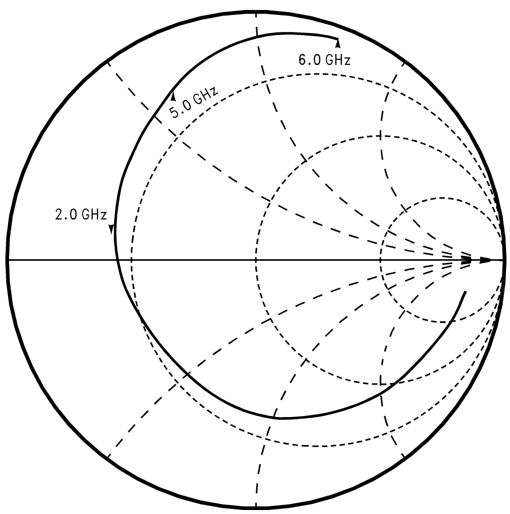

Figure 10. LMX243x UTCSP FinRF Input Impedance With 4.7 nH Series Match

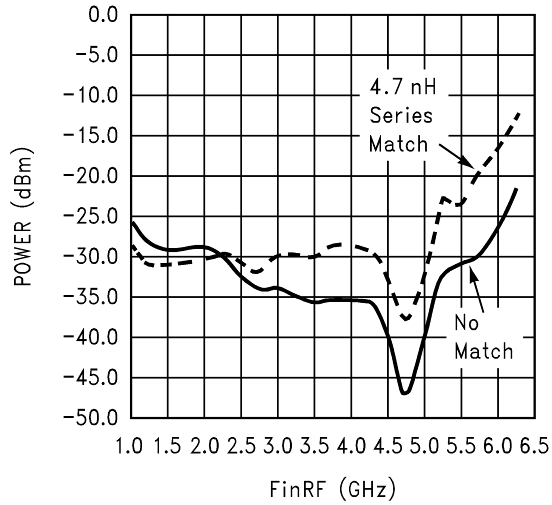

Figure 11. LMX243x UTCSP FinRF Input Sensitivity Improvement at 2.0 GHz

Figure 11 shows that an approximate 2.0 dB improvement in sensitivity is achieved at 2.0 GHz with the addition of the 4.7 nH series inductor. Figure 11 also shows that the sensitivity gets much worse at frequencies other than 2.0 GHz. Similarly, this evaluation is performed under typical conditions, with V_{CC} = 2.50 V and T_A = 25°C.

6 Summary

The results shown in this application report reflect conditions using a PCB with optimized grounding around 5.0 GHz. Most PCB designs may not be well grounded at 5.0 GHz and, therefore, may not achieve the sensitivity shown in the graphs above. However, this document demonstrates that a single element match offers a seemingly good solution for today's stringent PCB space and cost reduction requirements with an enhancement in sensitivity performance over a non-matched solution.

Table 1. LMX243x UTCSP FinRF Input Impedance Table V_{CC} = EN = 2.50 V, T_A = +25°C

FinRF (MHz)	|Γ|	Angle (Γ) (º)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
100	0.86	-8.63	334.27	-339.55	476.48
200	0.86	-10.72	265.44	-313.48	410.77
300	0.85	-13.48	202.09	-281.42	346.46
400	0.84	-17.01	150.76	-245.31	287.93
500	0.83	-21.05	112.18	-212.85	240.60
600	0.82	-25.32	85.96	-185.41	204.37
700	0.82	-29.78	67.32	-162.49	175.88
800	0.81	-34.35	54.27	-143.15	153.09
900	0.80	-39.02	44.76	-127.07	134.72
1000	0.80	-43.83	37.32	-113.62	119.59
1100	0.79	-48.76	31.65	-102.07	106.86
1200	0.79	-53.90	27.30	-91.89	95.86
1300	0.78	-59.07	23.84	-82.83	86.19
1400	0.78	-64.41	21.34	-74.84	77.82
1500	0.77	-70.04	19.20	-67.56	70.24
1600	0.76	-75.84	17.46	-60.88	63.33
1700	0.75	-82.06	16.27	-54.72	57.09
1800	0.73	-88.56	15.36	-48.89	51.25
1900	0.72	-95.19	14.90	-43.34	45.83

Table 1. LMX243x UTCSP FinRF Input Impedance Table V_{CC} = EN = 2.50 V, T_A = +25°C (continued)

FinRF (MHz)	|Γ|	Angle (Γ) (º)	Re {ZFinRF} (Ω)	Im {ZFinRF} (Ω)	|ZFinRF| (Ω)
2000	0.70	-101.45	14.32	-38.66	41.23
2100	0.68	-107.85	14.10	-34.26	37.05
2200	0.67	-114.12	13.81	-30.35	33.34
2300	0.66	-120.12	13.27	-27.09	30.17
2400	0.66	-126.01	12.50	-24.00	27.06
2500	0.67	-131.82	11.68	-21.22	24.22
2600	0.69	-137.96	10.55	-18.24	21.07
2700	0.71	-144.21	9.53	-15.58	18.26
2800	0.72	-150.25	8.55	-12.92	15.49
2900	0.74	-156.23	7.75	-10.25	12.85
3000	0.75	-161.92	7.22	-7.77	10.61
3100	0.76	-167.18	6.87	-5.48	8.79
3200	0.77	-172.05	6.63	-3.42	7.46
3300	0.77	-177.55	6.40	-1.49	6.57
3400	0.78	179.16	6.18	0.35	6.19
3500	0.79	174.92	5.99	2.18	6.37
3600	0.79	170.77	5.85	3.99	7.08
3700	0.80	166.54	5.74	5.80	8.16
3800	0.80	162.52	5.73	7.56	9.49
3900	0.80	158.74	5.73	9.22	10.86
4000	0.80	155.06	5.68	10.84	12.24
4100	0.80	151.49	5.69	12.38	13.62
4200	0.80	148.28	5.70	13.78	14.91
4300	0.80	146.02	5.73	14.88	15.95
4400	0.80	144.12	5.60	15.84	16.80
4500	0.82	142.31	5.41	16.66	17.52
4600	0.83	140.78	5.29	17.42	18.21
4700	0.83	139.65	5.14	17.95	18.67
4800	0.84	138.75	4.99	18.38	19.05
4900	0.84	137.79	4.84	18.85	19.46
5000	0.84	136.82	4.92	19.79	20.39
5100	0.84	135.77	4.88	18.89	19.51
5200	0.84	134.64	4.99	20.44	21.04
5300	0.84	133.33	5.11	21.16	21.77
5400	0.84	131.68	5.25	21.96	22.58
5500	0.83	129.77	5.43	23.01	23.64
5600	0.83	127.55	5.70	24.16	24.82
5700	0.82	125.41	6.03	25.33	26.04
5800	0.82	123.35	6.42	26.41	27.18
5900	0.81	121.68	6.75	27.30	28.12
6000	0.80	120.42	7.11	28.00	28.89

7 References

1. Bowick, Christopher, *RF Circuit Design*, 1st ed, 1990
2. Pozar, David M., *Microwave and RF Design of Wireless Systems*, 1st ed, 2000
3. Banerjee, Dean, *PLL Performance, Simulation, and Design*, 2nd ed, 2001