Application Report
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# Frequency Margining Using TI High Performance Programmable Oscillators

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**ABSTRACT**

Crystal oscillators and/or multiple output clock generators are critical in today's high performance consumer, computing, and communications systems. Deciding an optimal clock rate for the system can sometimes require several rounds of prototyping and validation. Clock Generators and Oscillator ICs - with the right hooks to margin synthesized clocks - can help to streamline the overall product development cycle and optimize performance of the end system. LMK61E2 is TI's high performance programmable oscillator with 90 fs (typical) integrated RMS jitter (12 kHz – 20 MHz) that also supports frequency margining. This application note will describe the benefits of frequency margining in various applications, highlight common approaches in the industry for frequency margining, and describe the flexible frequency margining features on LMK61E2 that are preferred by system architects.

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# 1 Frequency Margining using TI High Performance Programmable Oscillators

There are various applications that could benefit from frequency margining. Some of the potential use cases of frequency margining are explained below.

FPGA-based applications can optimize their power and throughput by selecting an optimal reference clock rate. The ability to quickly change the FPGA reference clock enables system designers to make the necessary logic updates to improve overall system performance and time to market. Serializer/ Deserializer (SerDes) transceivers in complex FPGA implementations can potentially benefit from clock rate optimization as well.

Using 10Gb/s Ethernet applications as an example, it is critical to stress every node in the network to the full 10Gb/s rate to find potential errors in frame reception and forwarding. System throughput is defined as the highest rate at which the system under test can forward the payload without losses. In order to guarantee interoperability within the framework of the IEEE802.3ae standard for 10Gb/s Ethernet, every node in the network must be tested at the maximum achievable throughput. The reference clock rate impacts the maximum achievable throughput and IEEE802.3ae standard allows the reference clock to be skewed from nominal rate by +/-100 ppm. The frequency margining features on LMK61E2 allows customers to margin the reference clock by +/- 100ppm to test Ethernet nodes at maximum throughput.

Dynamically modulating the reference frequency of CPUs/DSPs in certain data processing applications can potentially enhance system efficiency. As an example, the reference frequency of CPUs/DSPs can dynamically scale down under low load operation and scale back up for operation under heavy load. In another scenario, CPU clock speeds can be reduced when the temperature of the board exceeds a certain threshold, thereby protecting the system from thermal issues.

The ability to margin the reference frequency helps to uncover, isolate, or even work-around system timing margin or signal integrity issues early on in the design cycle. System architects can then quickly make the necessary course corrections thereby improving the overall system robustness.

Previous approaches to frequency margining have proven to be highly inefficient and time-consuming. One approach involves procuring fixed frequency oscillators from vendors that are offset by fixed amounts of frequency ppm error with respect to each other. Reworking boards to support these various oscillators proved to be inefficient especially when multiple boards needed to be tested over voltage and temperature corners.

The alternate option of including a multiplexer on-board to select between multiple oscillators proves to be rather limiting because of the small number of discrete frequencies that the system could be potentially tested with. In addition, a significant amount of phase discontinuity was introduced when switching between the frequencies.

The use of external frequency references like signal generators for frequency margining testing of ICs typically requires long PCB traces from the IC to edge or vertical mount SMA connectors that could result in a sub-optimal layout of the prototype board.

High performance oscillators such as LMK61E2 with frequency margining capabilities are able to address all the shortcomings of the approaches described above. These oscillators offer the flexibility to adjust the output frequency in coarse or fine frequency increments and decrements. The LMK61E2 features a high performance Fractional-N PLL that can be programmed to output a wide range of frequencies overcoming the frequency coverage inflexibility of fixed frequency oscillators. Using programmable crystal capacitance based fine frequency margining allows the LMK61E2 to offer improved performance over competition.

LMK61E2 offers coarse and fine frequency margining capabilities. Coarse margining refers to margining the output frequency in large steps. This is often in terms of % change with respect to the nominal frequency. This form of margining is primarily used for CPU performance testing, FPGA logic timing analysis, etc.

On LMK61E2, coarse margining is accomplished by changing the output dividers via $I^2C$ register writes. This method is valid for changes in the output divide anywhere between 5 and 511 (where maximum output frequency is 1 GHz). Output frequency changes initiated by changing between output divider values could result in glitches in the output frequency. The waveforms below highlight the response observed at the output when the output divider is updated via $I^2C$.

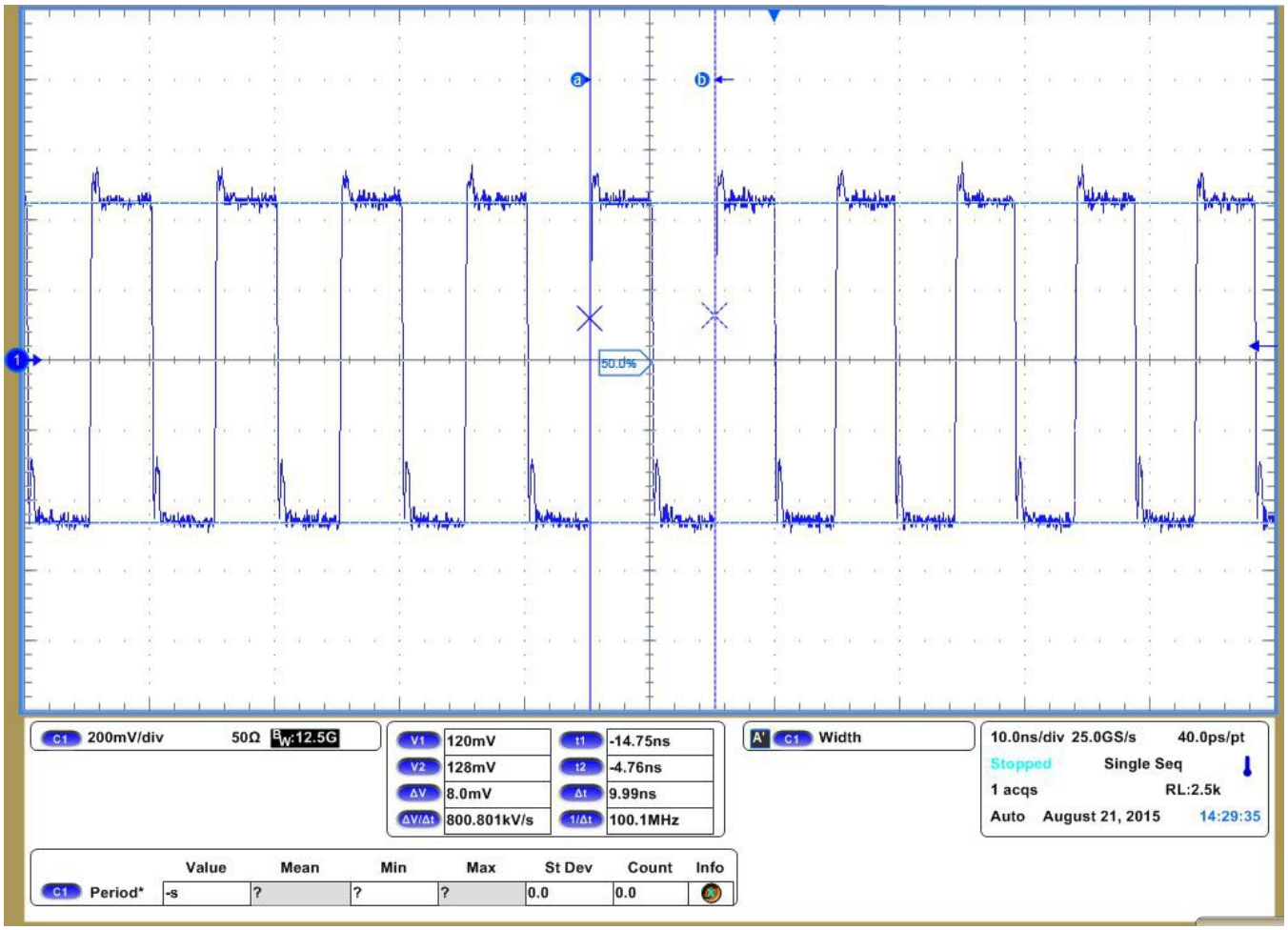


**Figure 1. Coarse Frequency Margining Reference Frequency = 50 MHz, VCO Frequency = 5000 MHz, Output Divider = 50**

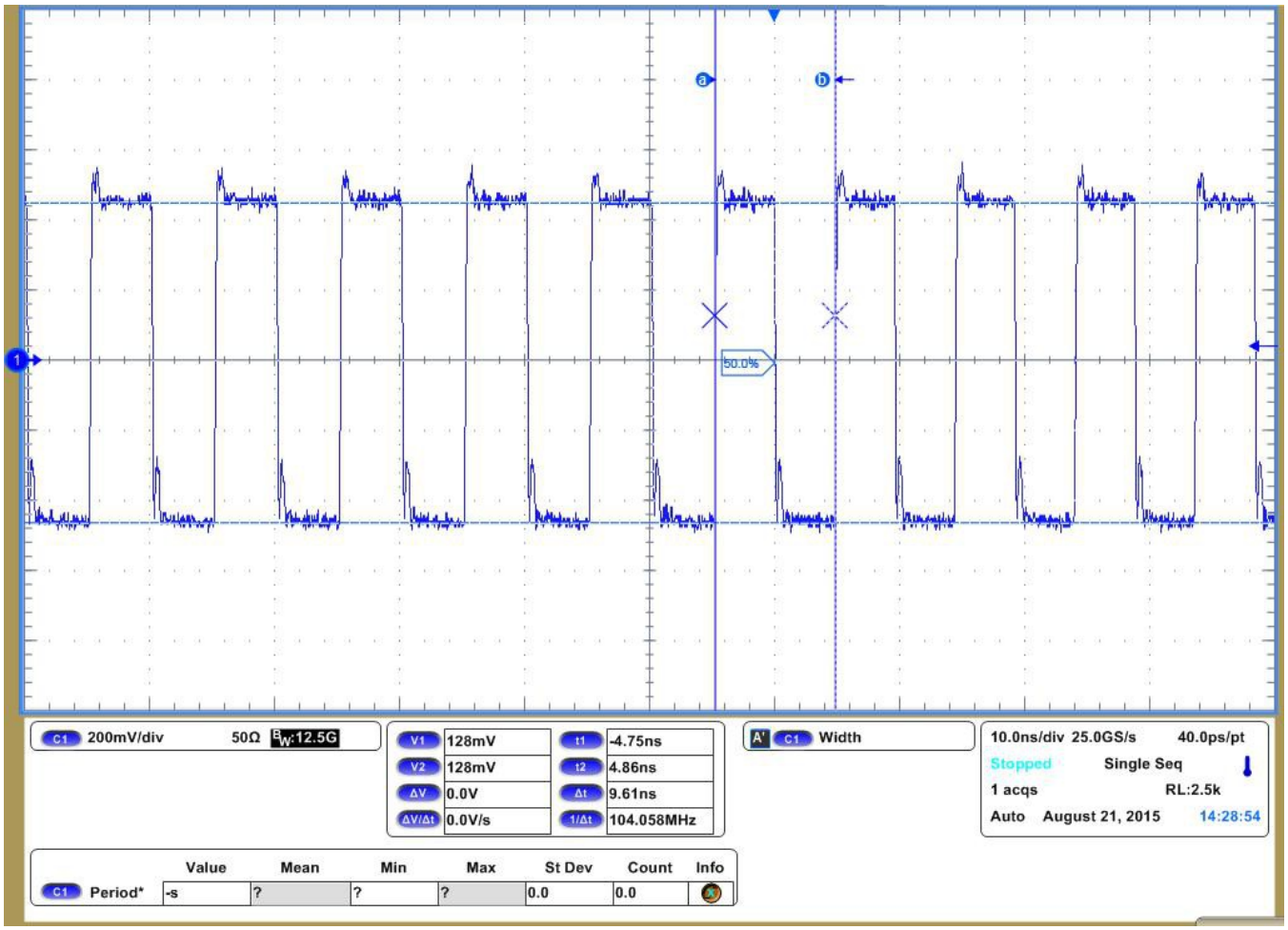


**Figure 2. Coarse Frequency Margining Reference Frequency = 50 MHz, VCO Frequency = 5000 MHz, Output Divider = 48 (Bottom)**

The waveform shown in Figure 1 corresponds to an output divider setting of 50 with a respective output frequency of 100 MHz. The waveform shown in Figure 2 corresponds to output divider setting of 48, resulting in an output frequency of 104.167 MHz.

Fine frequency margining, also known as ppm margining, could be used to evaluate Ethernet-based systems for standards compliance as well as improving system throughput. On LMK61E2, fine frequency margining can be achieved in two ways. The first approach is via tuning the fractional portion of the feedback divider. The numerator and denominator of the fractional portion of the feedback divider are 22 bits in depth, allowing for both the denominator and numerator to range between 1 (0 in the numerator disables fractional mode) to 4194303. It is highly recommended to re-calibrate the PLL after the fractional portion of the feedback divider has been updated via $I^2C$.

The second approach for fine frequency margining is done by programming the LMK61E2 on-chip crystal load capacitance. Under nominal conditions, the LMK61E2 on-chip crystal load capacitance can be programmed to operate the crystal at its fundamental frequency (50 MHz @ 9 pF load effective capacitance). The crystal frequency can be increased or decreased by adjusting the load capacitance away from the nominal capacitance. The amount of pullability (ppm per load capacitance) is dependent on the trim sensitivity of the integrated crystal. In LMK61E2, the crystal load capacitance can be programmed via $I^2C$. On power-up, a default value for the crystal load capacitance stored in the EEPROM is loaded into the active registers.

In order to estimate the binary code required to be programmed into the LMK61E2 crystal margining registers to cause a desired shift in the output clock frequency, the methodology stated in Section 2 can be followed.

Fine frequency margining achieved by varying the crystal load capacitance could result in significant improvement in the overall integrated RMS phase noise compared to fractional feedback divider based margining. In the case of the former, the PLL can be configured in integer mode and allowing the reference crystal frequency is varied. In the case of the latter, the PLL's configuration in fractional mode could result in spurs in the output phase noise. The figures below highlight the difference in the output clock phase noise using the two fine frequency margining approaches. Additionally, PLL re-calibration is not required when programming the binary code for fine frequency margining.

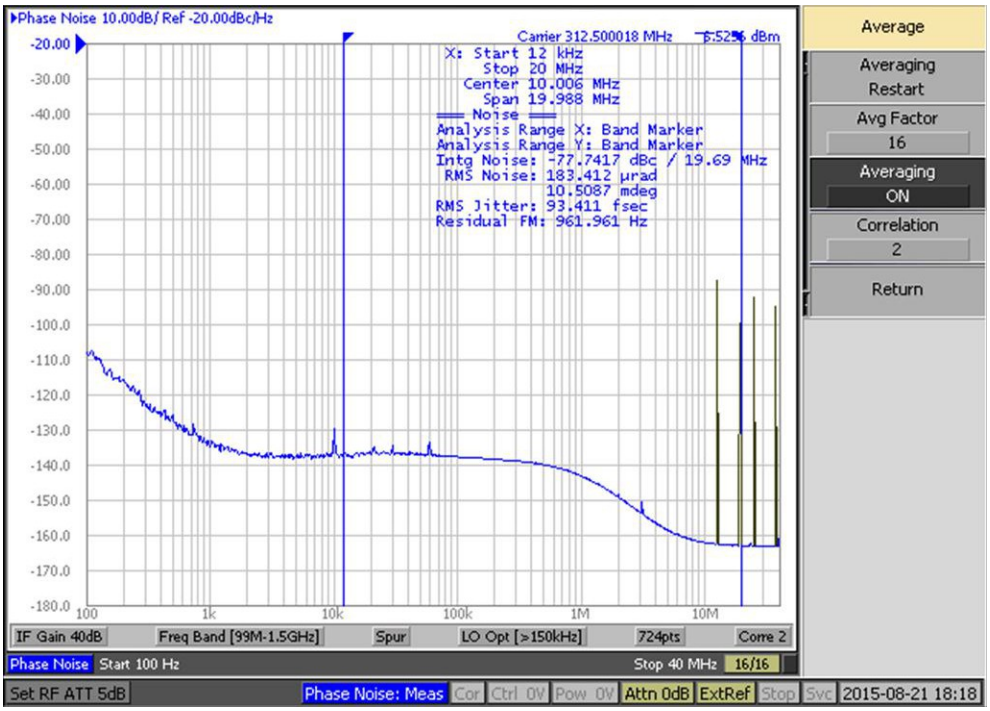


**Figure 3. Output Clock = 312.5 MHz, Nominal Binary Code = 475 (0 ppm)**

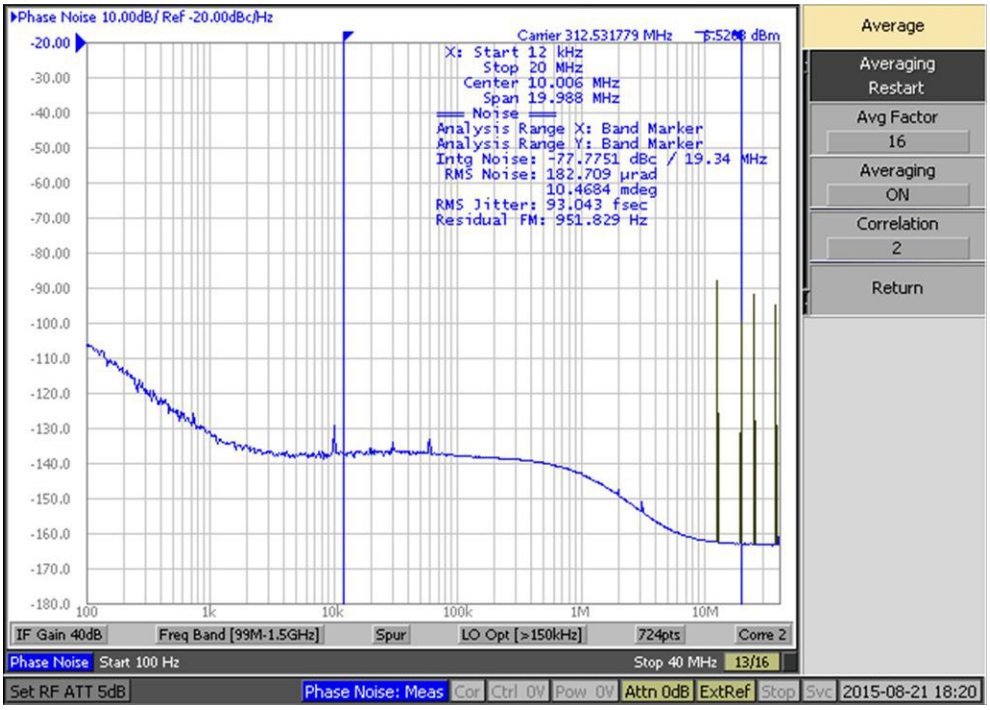


**Figure 4. Output Clock = 312.5 MHz + 100ppm, Binary Code = 180**

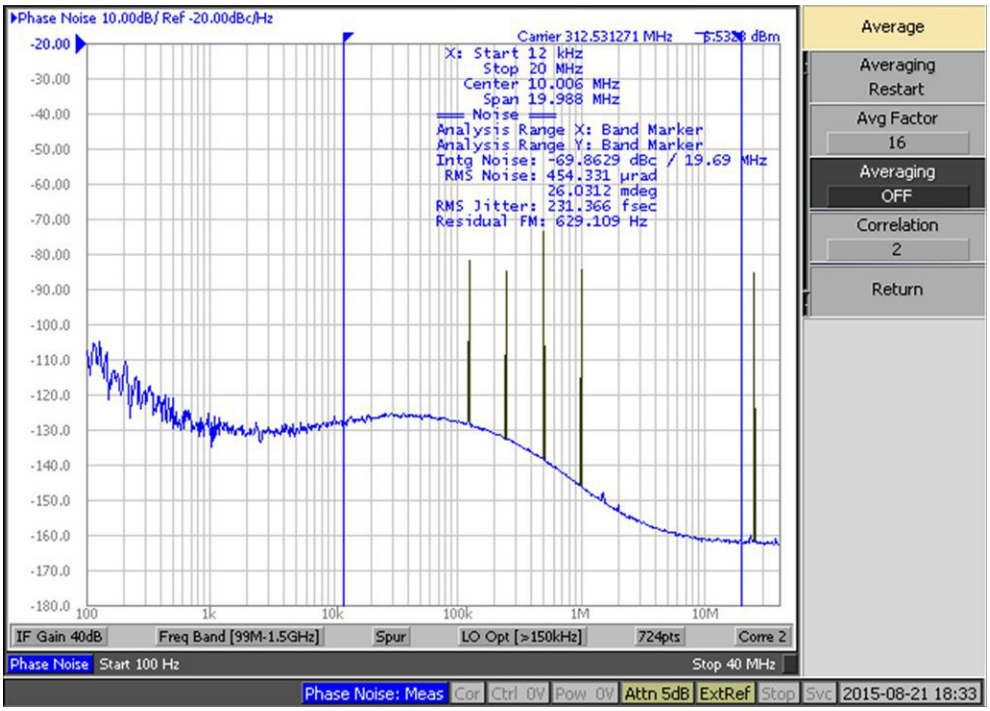


**Figure 5. Output Clock = 312.5 MHz + 100ppm, PLL in Fractional-N Mode**

From Figure 5, it can be seen that operating the PLL in Fractional-N mode to change the output frequency by +100ppm results in additional spurs. The integrated RMS jitter goes up from ~93 fs (nominal) to ~231 fs (+100 ppm) using this approach. In contrast, by programming the binary code for the crystal to result in the 100 ppm shift in the output frequency has minimal impact on the integrated RMS jitter. From the crystal pullability vs binary code measurement data, -100 ppm margining cannot be achieved using this method (pull range limited to ~ -50 ppm typical). However, applications tend to prefer to margin the frequency in the positive direction to increase system throughput. When evaluating high performance systems while using fine frequency margining, changing the crystal load capacitance by programming the required binary code into the device via $I^2C$ is the preferred option. Ideally, the setup for frequency margining should not add significant jitter to the output clock.

In summary, frequency margining provides system designers and architects the necessary flexibility to evaluate the performance of today's highly complex systems. In addition to proving ultra-low integrated RMS jitter, high performance programmable oscillators from Texas Instruments, such as LMK61E2, have flexible frequency margining hooks to enhance system productivity.

# 2 Appendix 1: Design Procedure for Programming the Crystal Frequency Margining Offset for LMK61E2

Following describes the steps needed to compute the required binary code to be programmed to LMK61E2 to generate a particular frequency offset.

## 2.1 Step 1

Power-up the LMK61E2 and readback Registers 0x10, Bits [1:0] and 0x11 Bits [7:0]. These 10 bits represent a binary code [0 to 1023] that determines the crystal internal load capacitance on the LMK61E2. Record this value. The LMK61E2 device comes trimmed from the factory to support +/-50ppm overall frequency accuracy. The binary code read back from the device on power-up could vary from one device to another.

## 2.2 Step 2

Program the device registers to achieve the desired frequency on the output. Measure the ppm error of the output frequency from the device using a frequency counter. Record this value.

## 2.3 Step 3

From the above crystal data, using a curve fitting tool (such as Excel), compute the trendline equation.

$$y = -0.000000000000027125843x^5 + 0.000000001202513717 74x^4 - 0.00000217108617709023x^3 + 0.00207223010091 0840x^2 - 1.147662299239980x + C \quad (1)$$

where

- ‘y’ is the frequency error in ppm
- ‘x’ is the binary code that sets internal crystal load capacitance
- C is a constant

Replace ‘x’ in the above equation with the binary code read back from the device in Section 2.3. Replace ‘y’ with the frequency error in ppm measured from Section 2.2. Compute the value of the constant C.

## 2.4 Step 4

Re-write the equation from Section 2.3 in terms of ‘x’, ‘y’ and the constant C. Plot the function in excel for values of ‘x’ over the range 0 to 1023. The binary code for the desired ppm margining can be inferred from this plot.

**NOTE:** Please send a request to clock_support@list.ti.com for assistance with this Steps 3 and 4.

### 2.4.1 Example

If ‘x’ is read back to be 512 (decimal) and ‘y’ is measured to be 0 ppm, the constant C can be calculated to be approximately 262.

Equation 1 can be re-written as

$$y = -0.000000000000027125843x^5 + 0.000000001202513717 74x^4 - 0.000002171086177090 23x^3 + 0.002072230100910840x^2 - 1.147662299239980x + 262 \quad (2)$$

Plotting the function gives

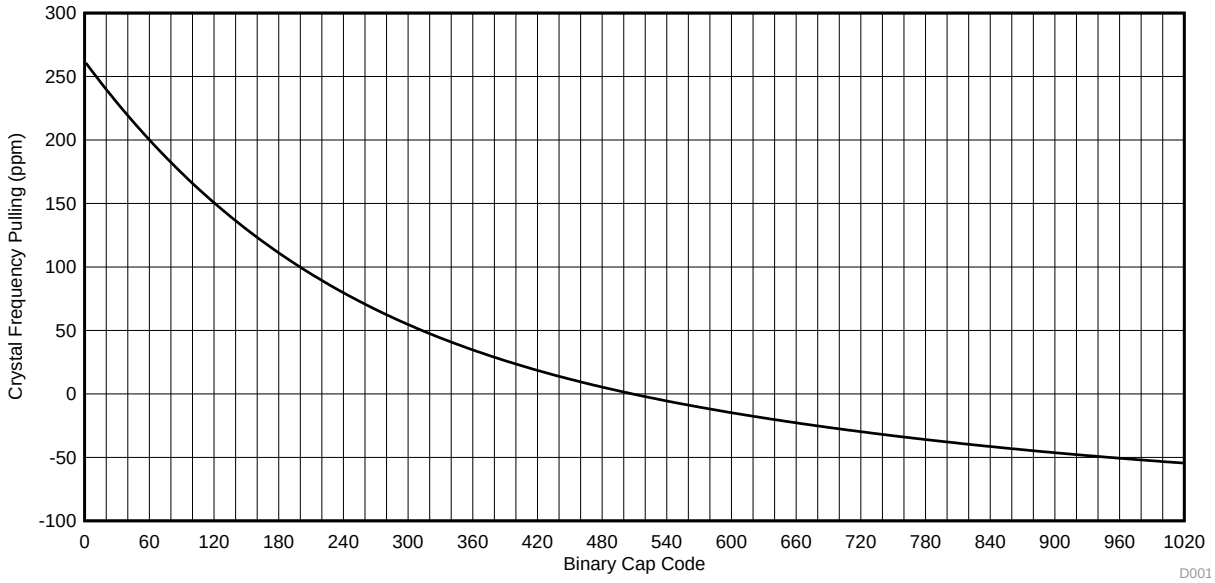


**Figure 6. Crystal Frequency Pulling vs Binary Cap Code Setting**

From Figure 6, the binary cap code setting that needs to be programmed into the device registers in order to margin the output frequency by a required ppm amount can be inferred.

Under nominal conditions, the steps highlighted above will allow the user to frequency shift the desired amount of ppm at the output within reasonable accuracy; further fine tuning could be required to achieve the exact ppm desired however.

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