Application Report
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Designing a TMS320F280x Based Digitally Controlled DC-DC Switching Power Supply

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ABSTRACT

This application report presents a TMS320F280x based digital control design and implementation of a high frequency dc-dc switching power supply. Starting with a dc-dc buck converter and a given set of performance specifications, different control blocks and parameters, used as in the analog control design approach, are reviewed prior to the control design in digital domain. The control loop is then analyzed and the digital controllers are designed using different control design approaches. Code examples are provided illustrating the controller implementation using TMS320F280x DSP controller. MATLAB based digital control design approaches presented here are finally validated with multiple test results from a prototype converter. The sample code described in this document can be downloaded from http://www.ti.com/lit/zip/SPRAAB3.

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1 Introduction

Digital control of switching power supplies is becoming more and more common in industry today because of the availability of low cost, high performance DSP controller with enhanced and integrated power electronic peripherals such as analog-to-digital (A/D) converters and pulse width modulator (PWM).

DSP based digital control allows for the implementation of more functional control schemes, standard control hardware design for multiple platforms and flexibility of quick design modifications to meet specific customer needs. Digital controllers are less susceptible to aging and environmental variations and have better noise immunity. Modern 32-bit DSP controllers, such as TMS320F280x, with processor speed up to 100MHz and enhanced peripherals such as, high resolution PWM module, 12-bit A/D converter with conversion speed up to 160nSec, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability, gives the power supply designers all the benefits of digital control and allows implementation of high bandwidth, high frequency power supplies without sacrificing performance [1-4]. The extra computing power of such processors also allows implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor and optimize the total system cost. However, the power supply engineers, mostly familiar with analog control design, are faced with new challenges as they start to adopt these digital control techniques in their designs.

Since DSPs just started to gain some serious considerations in controlling power supplies, many pertinent factors in the design and implementation of a digital control loop need to be addressed. Accurate representation of the control blocks and the associated control parameters is critical for the analog designers in order to enable them to implement the DSP based digital control techniques using the well-known analog control design approaches. This application report, therefore, describes a step-by-step DSP based digital control design and implementation of a high frequency dc-dc converter. Starting with a dc-dc buck converter and a given set of performance specification, it discusses different control blocks, different control design approaches and highlights the significant differences in designing control in the digital domain compared to the analog approach. Two approaches to the digital control design are illustrated namely, the design by emulation and the direct digital design. These are first shown in MATLAB and then verified by experimental results. In this process the effects of sampling delay and the computation delay are also analyzed in MATLAB and then verified experimentally. Finally the assembly code listings implementing the designed controllers are provided in order to aid the users quickly validate these controllers using a similar DSP controlled dc-dc converter set up.

2 Digital Control Implementation for DC-DC Converter

Figure 1 shows a simplified block diagram of a digitally controlled dc-dc converter interfaced to a TMS320F280x DSP controller.

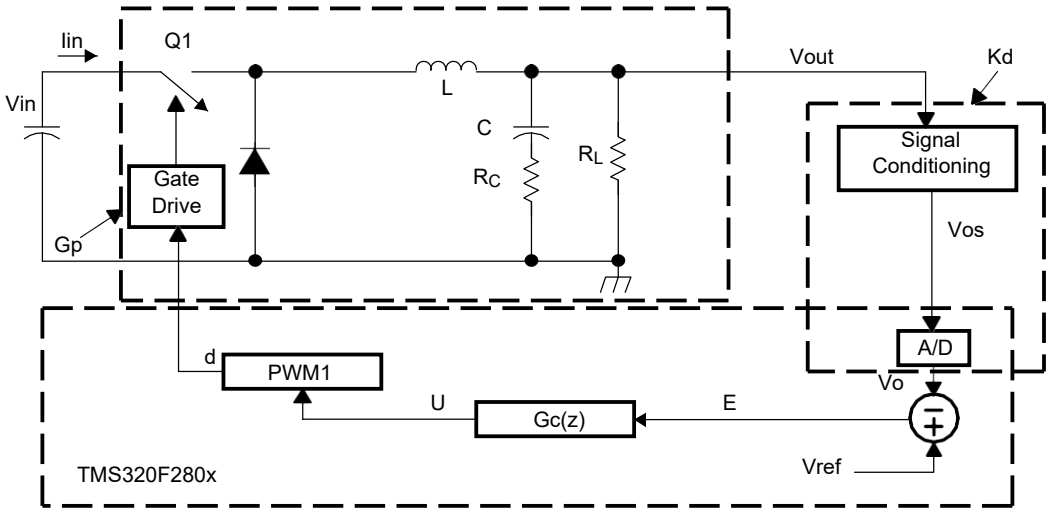

Figure 1. DSP based Digital Control of DC-DC Converter

As indicated in Figure 1, a single signal measurement is needed to implement the voltage mode control of the dc-dc converter. The instantaneous output voltage Vout is sensed and conditioned by the voltage sense circuit and then input to the DSP via the ADC channel. The digitized sensed output voltage Vo is compared to the reference Vref. The voltage loop controller Gc is designed to make the output voltage Vout track the reference Vref and at the same time achieve the desired dynamic performance. The digitized output U of this controller provides the duty ratio command for the buck regulator switch Q1. This command output is used to calculate the appropriate values for the timer compare registers in the on-chip PWM module. The PWM module uses this value to generate the PWM output, PWM1 in this case, that finally drives the buck converter switch Q1.

2.1 Digital Sampling Loop Implementation

Figure 2 shows one example of a digital sampling scheme using the DSP on-chip peripherals.

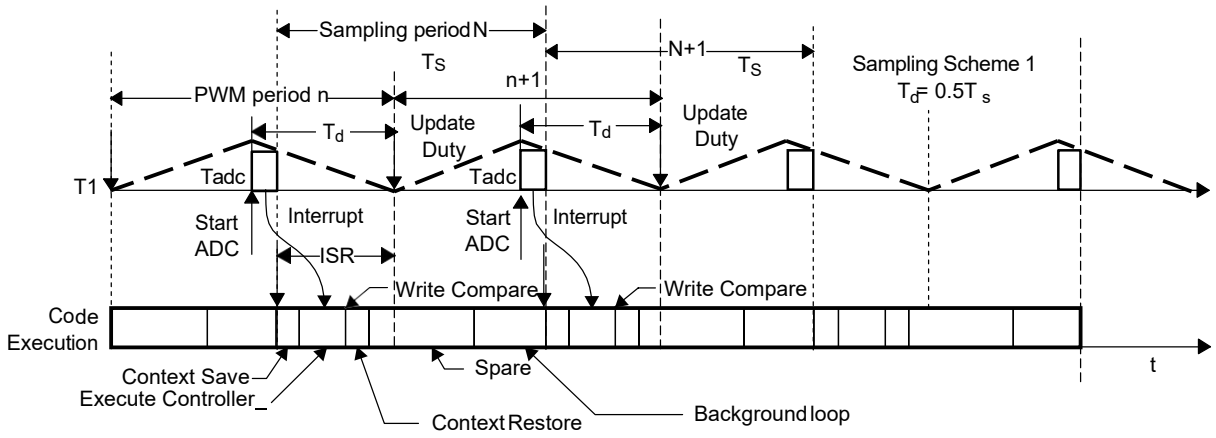

Figure 2. DC-DC Converter Digital Control Loop Sampling Scheme

The sampling scheme affects the digital controller design and, therefore, needs appropriate attention. PWM output frequency is set up by configuring one of the on-chip Timers, T1 in this case. In this example, T1 generates a dual edge modulated (symmetric), 250 kHz PWM output. These timers have associated compare registers which are used to write the calculated duty ratio values. These values then get compared with the timer counter value in order to generate the PWM output. The time at which a newly written compare value affects the actual PWM output duty ratio is controlled by associated PWM control registers. In this example, the PWM control registers are set up such that a new value written in the compare register, changes the actual PWM output duty ratio at the start of the subsequent timer (T1) period. Also, the ADC control registers are set up such that the AD conversion is triggered at the middle of the ON pulse of the PWM output. As soon as the conversion is complete, the ADC module is set up to generate an interrupt. The time delay between the start of AD conversion and this interrupt is shown in Figure 2, as Tadc. This time includes the AD conversion time and the processor interrupt latency. Inside the interrupt service routine (ISR), the user software reads the converted value from the ADC result register, implements the controller and then writes the new PWM duty ratio value to the appropriate PWM compare register. However, this new duty ratio value takes affect at the start of the subsequent PWM cycle. From Figure 2, it is clear that the time delay Td, between the ADC sampling instant and the PWM duty ratio update, is half the PWM period. In this case, the PWM period and the sampling period (Ts) are equal and so the computation delay is, Td = Ts/2. Also shown in Figure 2, the calculation of a new duty ratio value inside the ISR is completed well before a subsequent interrupt is generated. This means that, at this sampling frequency, the processor bandwidth (100 MHz) allows for sufficient spare time to extend the ISR and execute multiple controllers or other time critical tasks. Some of this spare time can also be used for non-time critical tasks by running them from a background loop.

2.2 DC-DC Controller Design

The system parameters used in this design are:

- Vin = 4~6V, Vout = 1.6V, Max output current Iout = 16A, RL = Vout/Iout = 0.1 ohm (Minimum)
- Maximum output voltage (used for ADC signal scaling) Vomax = 2V
- PWM frequency fpwm = 250kHz; Voltage loop sampling frequency fs = 250kHz
- Output filter components, L = 1.0uH, C = 1620uF, RC = 0.004 Ohm
- Desired voltage loop bandwidth fcv = 20kHz
- Phase Margin = 45 deg, Settling time < 75uSec

In order to design the digital controller, two approaches are discussed. These are, 1. Design by Emulation and 2. Direct Digital Design.

2.2.1 Design by Emulation

This is also known as Digital Redesign Approach. In this method, an analog controller is first designed in the continuous domain as if one were building continuous time control system, by ignoring the effects of sampling and hold associated with the AD converter and the digital PWM circuits. The analog controller is then converted to a discrete-time compensator by some approximate techniques. Figure 3 represents a simplified block diagram of the system in Figure 1. It shows all the different components of this closed loop control system in s-domain.

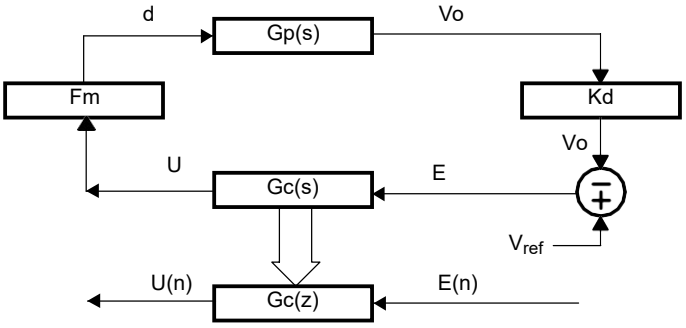

Figure 3. DC-DC Converter Control Loop Block Diagram in s-domain

The small signal power stage model of the buck converter in s-domain is indicated as Gp(s). For the given system parameters with Vin = 5.0V and R_L = 0.1 ohm, this is derived as,

$$G_P(S) = V_{in}\frac{(sR_CC+1)}{\left[s^2LC\left(1+\frac{R_C}{R_L}\right)+s\left(R_CC+\frac{L}{R_L}\right)+1\right]}$$

$$= \frac{(3.24\times 10^{-5}s + 5.0)}{(1.685\times 10^{-9}s^2 + 1.648\times 10^{-5}s + 1.0)}$$

If the maximum output voltage is Vomax, then the voltage feedback factor is, Kd = 1/Vomax, provided that the digital output voltage Vo is represented in Q31 fixed-point format for this 32-bit DSP controller [6]. The PWM modulator gain is Fm = 1. This is so because the user software together with the on-chip PWM hardware can be configured such that as the controller output U (in Q31) varies between 0 ~ 7FFFFFFFh, the PWM output duty ratio d varies between 0 ~ 1, [6].

Now for this plant Gp(s), a suitable analog controller Gc(s) is designed in MATLAB using the available control design tool called 'sisotool'. The Bode plot for this design is shown in Figure 4 where the system bandwidth (BW) is set at 25 kHz with a phase margin (PM) of 71 deg.

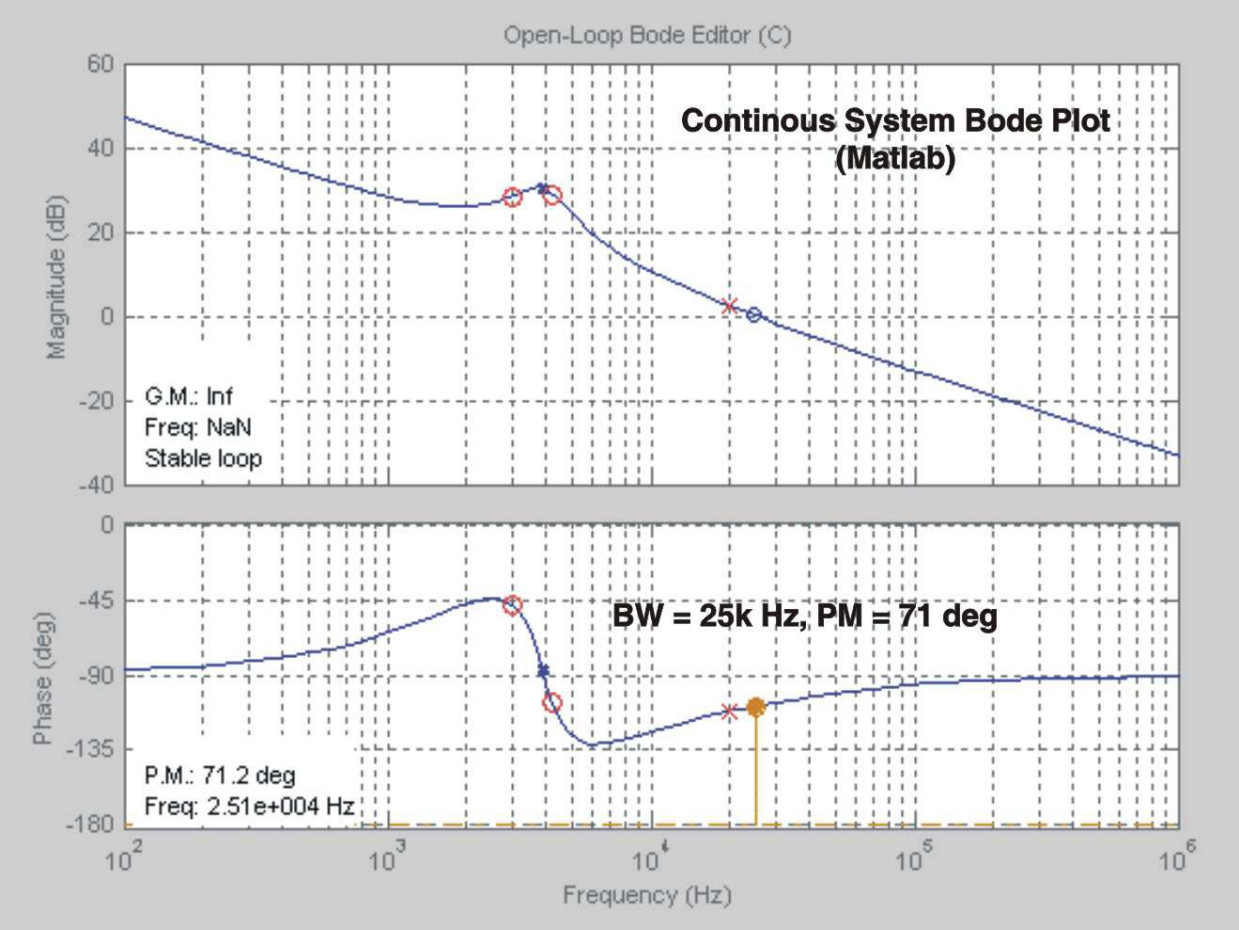

Figure 4. DC-DC Converter Control Loop Bode Plot Gp(s) * Gc1(s)*Kd*Fm (MATLAB)

The corresponding controller Gc1(s) can be easily imported from the MATLAB control design toolbox. This is found as,

$$G_{C1}(s) = \frac{(14.3s^2 + 6.514 \times 10^5 s + 7.2 \times 10^9)}{s(s + 1.256 \times 10^5)}$$

This analog controller Gc1(s) can be discretized by any of the commonly used discretization methods such as, Bilinear, Pole-Zero match and Forward etc. [5, 9]. This can be performed in MATLAB simply by writing the MATLAB script as:

```
Gc1_s=tf([14.3 6.514e005 7.2e009],[1 1.256e005 0]);%Controller in s-domain%
Gc1_z = c2d(Gc1_s, Ts, 'matched'); % Digital Controller %
```

This generates the following digital controller Gc1(z):

$$G_{C1}(z) = \frac{U}{E} = \frac{12.34 - 22.53z^{-1} + 10.28z^{12}}{1 - 1.605z^{-1} + 0.6051z^{-2}}$$

where, the sampling time is Ts = 1/fs = 4uSec. In discrete form, this controller is written as,

$$U(n) = 1.605U(n-1) - 0.605U(n-2) + 12.34E(n) - 22.53E(n-1) + 10.28E(n-2)$$

where, U is the control output and E is the error voltage. The quantities with (n) denote the sampled values for the current sampling cycle, the quantities with (n-1) denote one sample old values and so on.

This controller was implemented using the TMS320F280x DSP instruction set. During the code initialization the coefficients of the above controller are first converted to a suitable fixed point format (Q format) in order to get the best accuracy out of this 32-bit processor. An example code listing is given in the zip file for a similar controller. The fixed point format used for the controller coefficients in this code example is Q26.

Once the controller was implemented in the DSP, its closed loop dynamic performance was tested on a prototype dc-dc converter. This transient load response is shown in Figure 5:

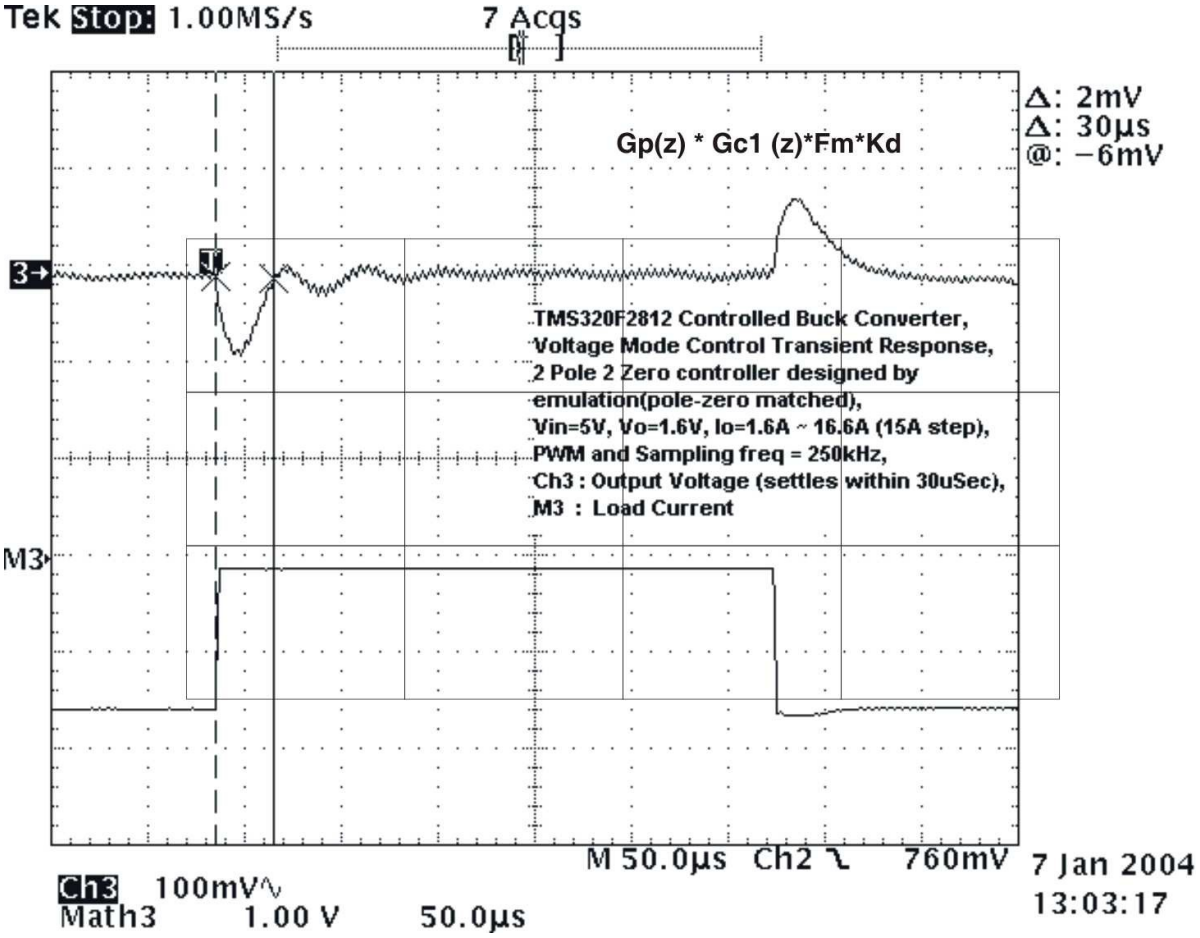

Figure 5. DC-DC Converter Load Transient Response (loop gain = Gp*Gc1*Fm*Kd)

For a step load change of 15A, the output voltage settles within 30uSec (1% band). The converter has a satisfactory time response. However, the damping of the transient response does not reflect a phase margin of 71 deg as shown in MATLAB Bode plot (see Figure 4). This difference in the designed and actual phase margin is because of the fact that we completely ignored the effect of sampling and hold and the computation delay. In digital control design the effect of these delays can be taken into account prior to the control design that results in a more predictable and accurate dynamic performance. This is illustrated next.

2.2.2 Direct Digital Design

Figure 1 is now drawn as in Figure 6 to show all the different components of this closed loop control system including the effect of sampling and hold.

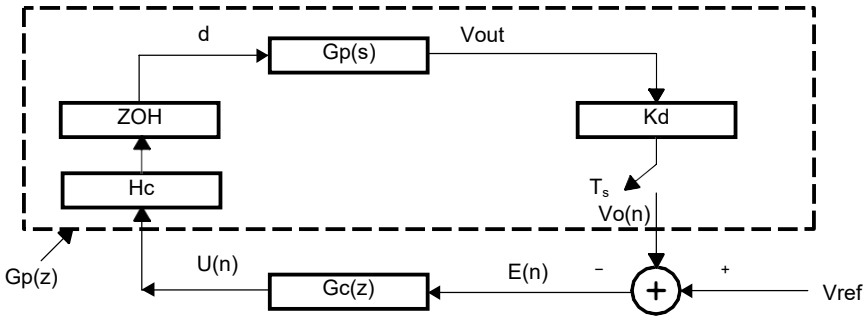

Figure 6. DC-DC Converter Digital Control Loop Block Diagram

The sampling process by the on-chip ADC is represented by an ideal sampler with time period Ts. ADC can be represented this way as compared to the model given in [7], since the ADC gain is taken into account in the block labeled Kd and ADC conversion time is included in the computation delay block labeled Hc. The on-chip PWM module acts as a hold device. Representing this as a zero-order-hold (ZOH), the ADC and the PWM module together form a sampling and hold device. The effect of such sample and hold action is to introduce a time delay of Ts/2 or a phase lag of ωTs/2 as illustrated in Figure 7. Here a signal is sampled at time interval of Ts and then reconstructed through ZOH. The reconstructed signal is found to lag the original signal by ωTs/2 radian or 180f/fs degree.

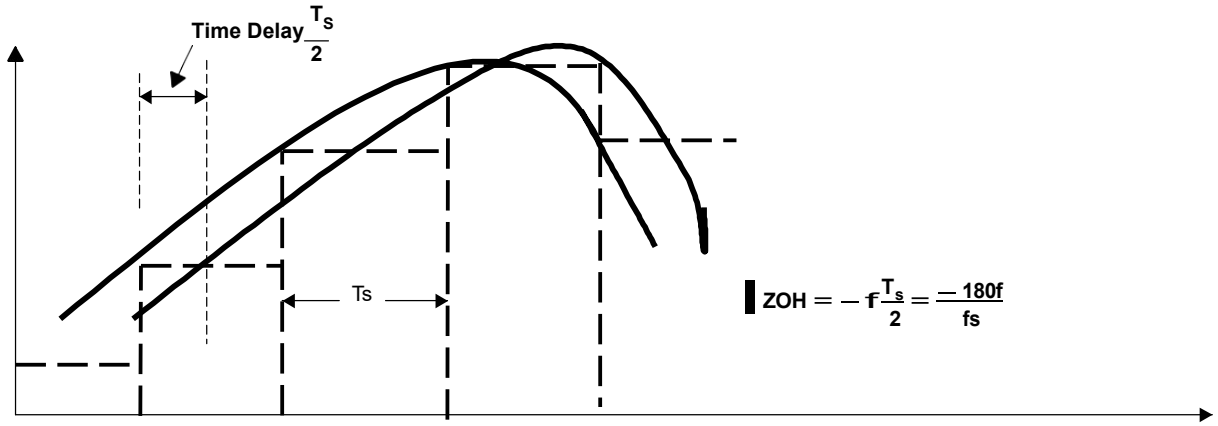

Figure 7. Sample and Hold Process in a Digital System

The s-domain transfer function of such a device can be expressed as [9],

$$SH(s) = \frac{(1 \quad e^{\ ST_s})}{s}$$

Thus we see that the effect of the sampling and hold process in a digitally controlled power supply is that it introduces an additional phase delay of 180f/fs degree compared to an equivalent analog controlled power supply. Here, f is the frequency of interest, i.e. the bandwidth, where the phase is calculated. So, for the Bode plot shown in Figure 4, where we ignored the effect of sampling and hold, the actual phase margin is at least reduced by 18 degree (=180x25kHz/250kHz). This means that this system can have a PM of at most 53 degree (=71-18). In reality this will be further reduced by the computation delay associated with any digital system. This explains the reason for the under-damped response of this system as shown in Figure 5. The computation delay block Hc, models the time delay between the ADC sampling instant and the subsequent PWM duty ratio update. This time delay is denoted by Td and the transfer function for Hc is,

$H_C(s)$ e^{ST_d}

In direct digital design approach, the continuous time power stage model is first discretized with ZOH and the sampler. Once this is available, the discrete-time compensator. i.e., a digital controller Gc(z) is designed directly in the z-domain using methods similar to the continuous-time frequency response methods. This has the advantage that the poles and zeros of the digital controllers are located directly, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop power converter. The discrete-time transfer function Gp(z) of the converter plant, including the ZOH, the sampler, the voltage sensing gain Kd and the computation delay model Hc is [8],

$$G_P(z) = Z\left\{\frac{1}{s}\left(1 - e^{-ST_s}\right).H_C(s).G_P(s).K_d\right\}$$

where, Z denotes the z-transform of the function inside the parenthesis {}. This can be computed in MATLAB by writing the MATLAB script as:

```
Vin=5.0; Vo=1.6; Io=16; Kd=0.5; L=1e-6; C=1620e-6; Rc=4e-3; RL=Vo/Io; Ts=4.0e-6; Td=0.0*Ts;
num_Gps=Vin*[Rc*C 1]; denom_Gps=[L*C*(1+Rc/RL) (L/RL+Rc*C) 1];
Gps_dly=tf(num_Gps,denom_Gps,'inputdelay',Td); %s-domain plant with computation delay Td%
Gpz=c2d(Gps_dly*Kd,Ts,'zoh'); %Discrete plant with ZOH, Kd and Td%
```

The resulting discrete plant obtained from MATLAB is,

$$G_{P1}(Z) = 0.0494\frac{(z - 0.5283)}{(z^2 - 1.952z + 0.962)}$$

Where Kd = 1/Vomax = ½, Ts = 1/fs = 4uSec and the computation delay Td, for now, is taken as Td = 0, i.e., Hc = 1.

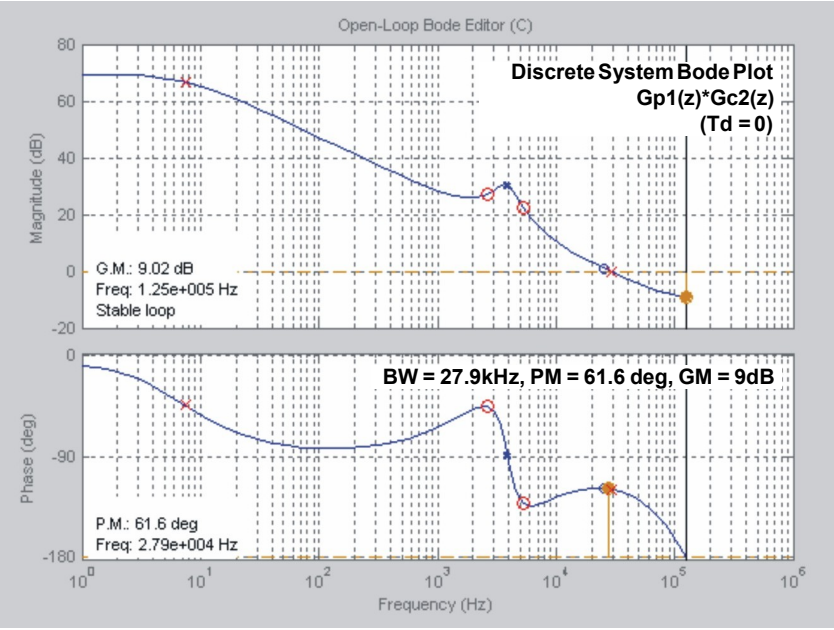

Figure 8. DC-DC Converter Digital Control Loop Bode Plot Gp1*Gc2 (MATLAB)

For this plant G_{P1}, a suitable digital controller is designed in MATLAB using the 'sisotool'. The system bandwidth is set at 27.9 kHz with a phase margin of 61.6 deg. The Bode plot is shown in Figure 8. The corresponding controller GC2 is derived from MATLAB as,

$$G_{C2}(z) = \frac{U}{E} = \frac{14.87 - 26.91z^{-1} + 12.16z^{-2}}{1 - 1.473z^{-1} + 0.473z^{-2}}$$

In discrete form, this controller is written as,

$$U(n) = 1.473U(n-1) - 0.4731U(n-2) + 14.87E(n) - 26.91E(n-1) + 12.16E(n-2)$$

This controller was implemented using the TMS320F280x DSP instruction set. The corresponding code listing is given in the zip file associated with this application report. The fixed point format used for these controller coefficients is Q26.

Case 1 : Computation Delay Td = 0.5Ts

For the controller just designed we assumed Td = 0, which is not the case if we implement this controller using the sampling scheme shown in Figure 2. So, we recalculate Gp(z) for T= 0.5Ts to include the effect of the sampling scheme shown in Figure 2. Thus, by setting Td=0.5Ts in the MATLAB script shown before, the modified plant model is obtained as,

$$G_{P2}(z) = \frac{(0.022z^2 + 0.017z - 0.0158)}{z(z^2 - 1.952z + 0.962)}$$

The corresponding Bode plot for this plant Gp2(z) with the controller Gc2(z) is shown in Figure 9. From the two plots of Gp1*Gc2 and Gp2*Gc2, it is clear that the same controller Gc2 results in a phase margin reduction by 20.6 deg (= 61.6-41.0) for the latter system. This reduction in phase margin can be accounted for by the computation time delay of Td = 0.5Ts associated with Gp2. This time delay translates to a phase lag of,

$$LH_C = wT_d = (360f)(0.5Ts) = 20 \text{ deg}$$

where, Ts = 4uS, and f ≈ 27kHz is the cross-over frequency at which the phase lag is calculated.

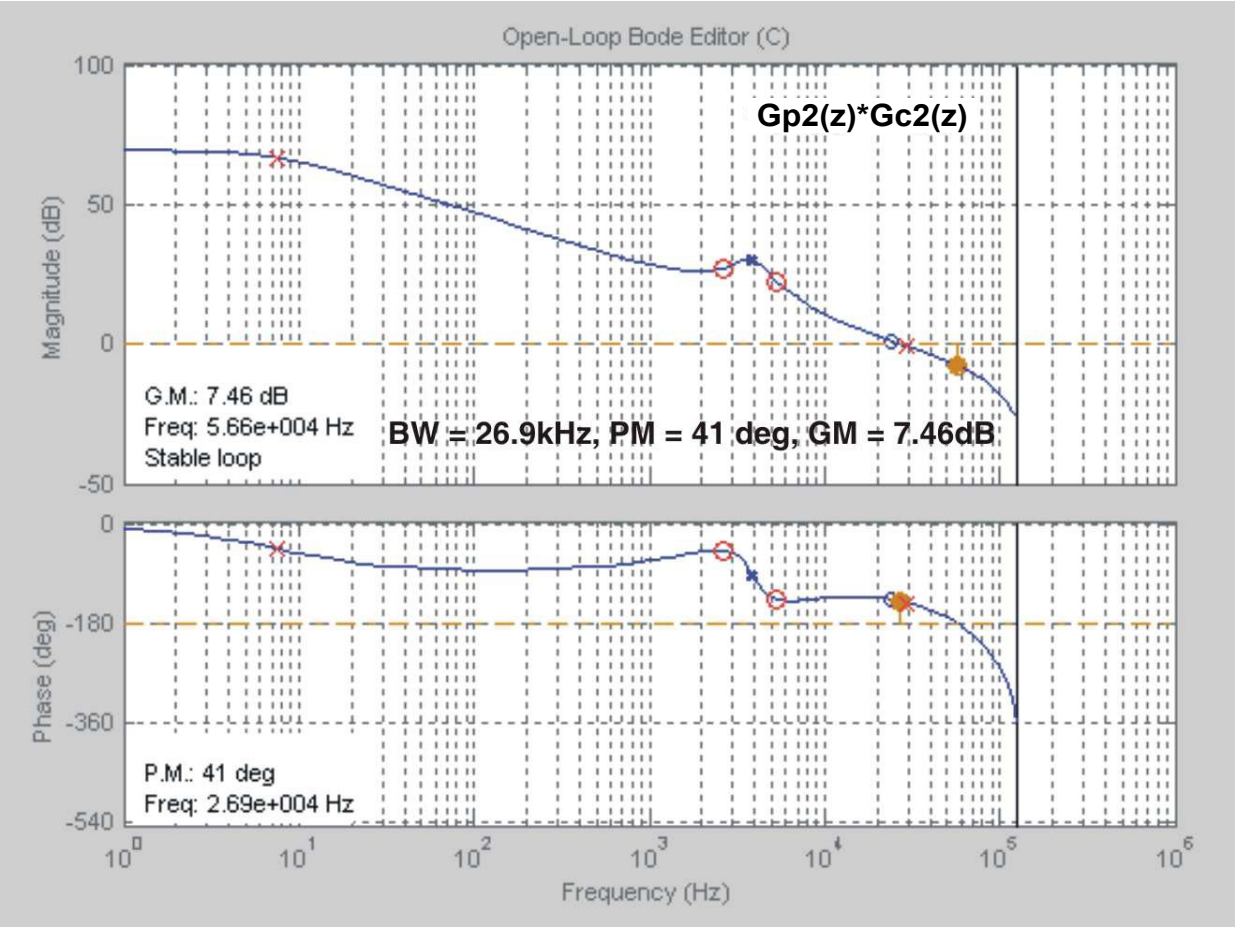

Figure 9. DC-DC Converter Digital Control Loop Bode Plot Gp2*Gc2 (MATLAB)

The actual system Bode plot for the digitally controlled dc-dc converter represented by the plant model Gp2(z) and controlled by the controller Gc2(z) is shown in Figure 10. Notice that the frequency domain performance parameters (bandwidth, phase margin and gain margin) agree quite well between the actual and the designed values. The time domain dynamic performance of the converter is shown in Figure 11. For a step load change of 15A, the output voltage settles within 28uSec (1% band). These test results on the frequency and time domain characteristics of the digitally controlled converter show the validity of the MATLAB based design approach as illustrated by Figure 8 and Figure 9 above.

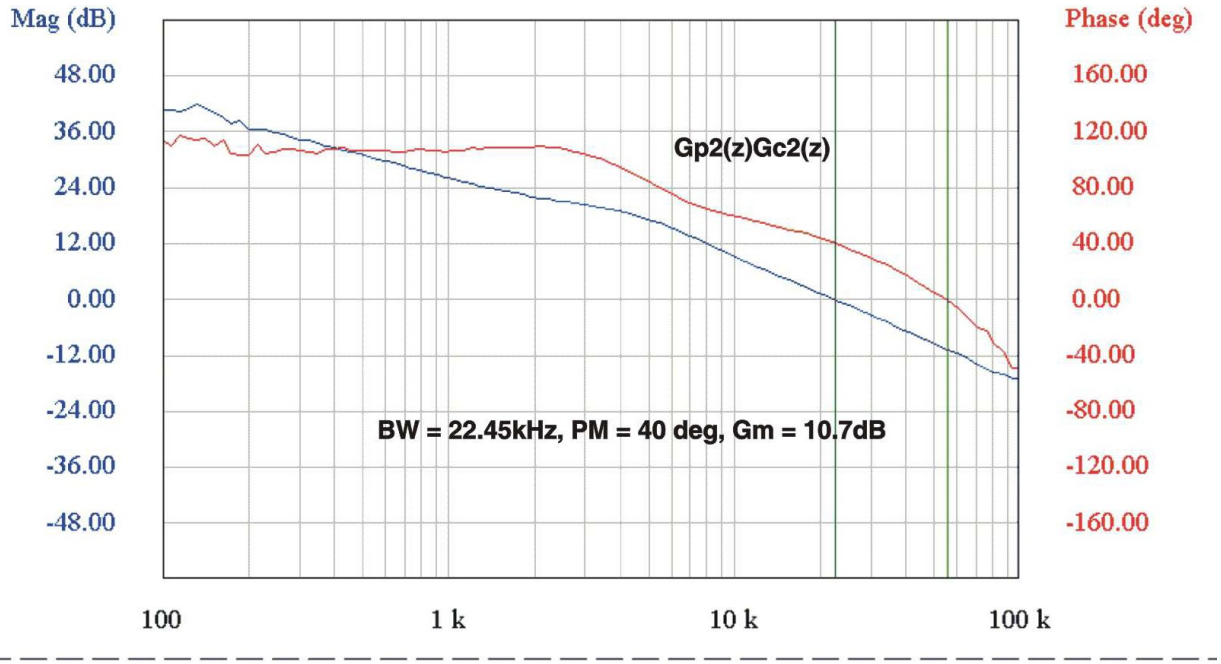

Figure 10. DC-DC Converter Control Loop Bode Plot Gp2*Gc2 (Test result from prototype h/w)

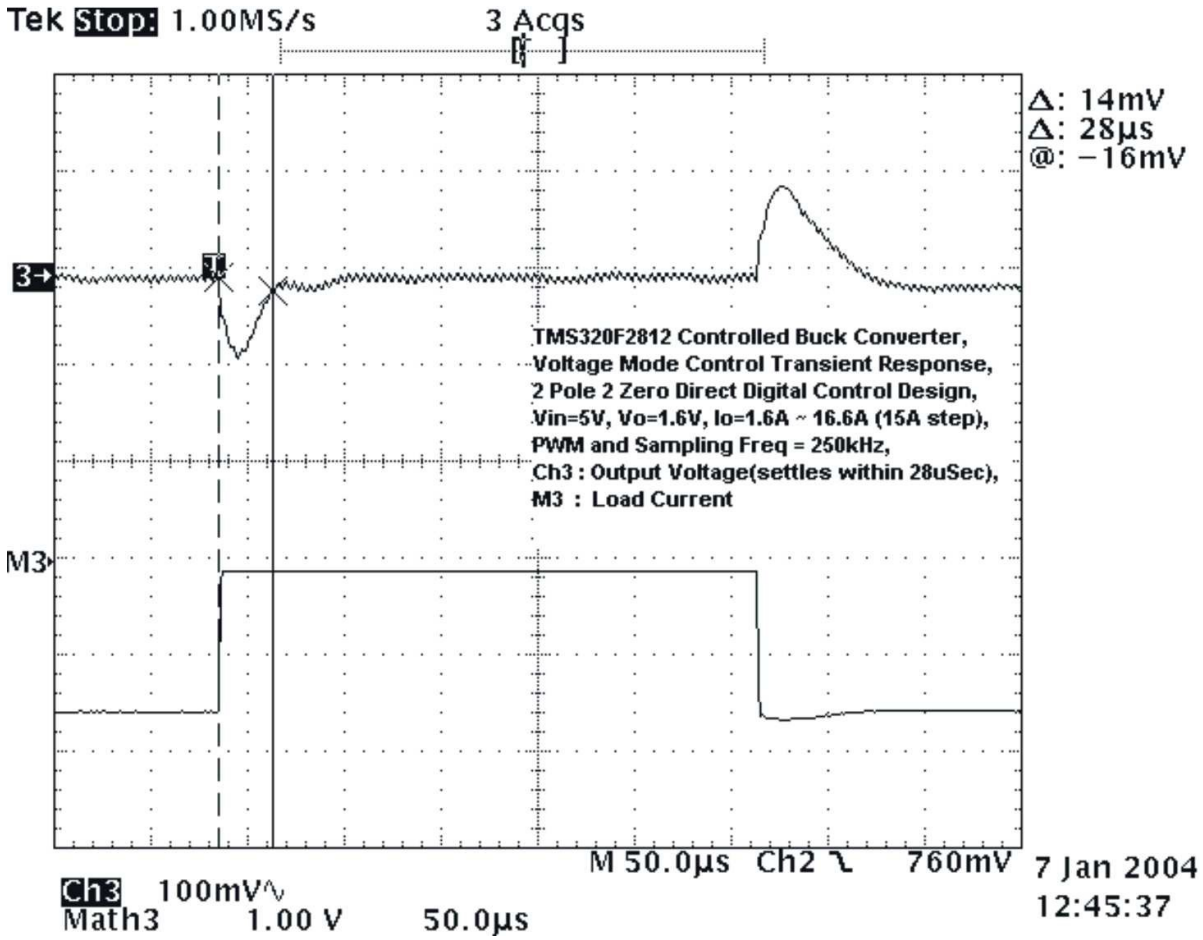

Figure 11. DC-DC Converter Load Transient Response (Loop gain = Gp2*Gc2)

Case 2 : Computation Delay Td = 2.0Ts

The sampling scheme shown Figure 2 can be modified to investigate the effect of a more severe computation delay of Td = 2.0Ts. This is easily done in software by changing the interrupt scheme and the way the actual PWM duty ratio is updated following a new AD conversion of the output voltage. Once this is done in software, the new plant model Gp3, for Td = 2Ts, is computed using MATLAB as,

$$G_{P3}(z) = \frac{(0.022z^2 + 0.017z - 0.0159)}{z^2(z^2 - 1.954z + 0.963)}$$

The corresponding Bode plot for this plant Gp3(z) with the controller Gc2(z) is shown in Figure 12.

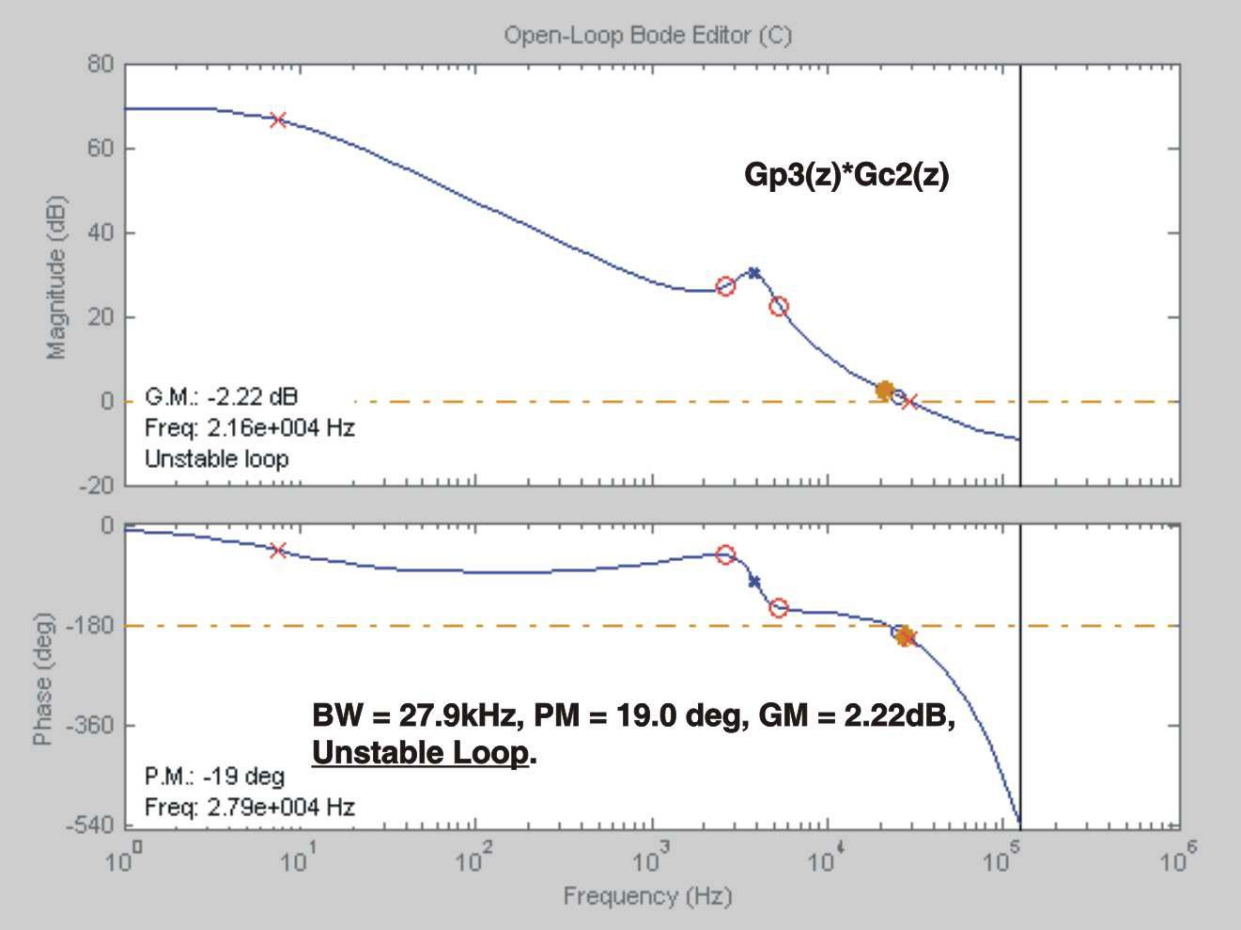

Figure 12. DC-DC Converter Digital Control Loop Bode Plot Gp3*Gc2 (MATLAB)

From the plot of Figure 12 it is clear that this system is completely unstable when controlled by the controller Gc2. Comparing the plots of Gp1*Gc2 and Gp3*Gc2 we note that the controller Gc2 results in a phase margin reduction by 80.6 deg [= 61.6-(-19.0)] for the latter system. This reduction in phase margin is again accounted for by the computation time delay of Td = 2.0Ts associated with Gp3. This time delay translates to a phase lag of,

$$LH_C = wT_d = (360\ f)(2.0Ts) = 80\ \text{deg}$$

where, Ts = 4uS, and f ≈ 27kHz is the loop cross-over frequency at which the phase lag is calculated. In order to find a stable controller for Gp3, we note that this plant has 4-poles and 2 zeros and, therefore, the 2-pole 2-zero controller Gc2 cannot stabilize the system. So, using MATLAB a new 3-pole 3-zero controller Gc3 is designed as,

$$G_{c3}(z) = \frac{U}{E} = \frac{14.4 - 31.1z^{-1} + 20.1z^{-2} - 3.376z^{-3}}{1 - 1.235z^{-1} + 0.2362z^{-2} - 0.00115z^{-3}}$$

$$== U(n) = 1.235U(n-1) - 0.2362U(n-2) + 0.00115U(n-3)$$
$$+ 14.4E(n) - 31.1E(n-1) + 20.1E(n-2) - 3.376E(n-3)$$

The corresponding Bode plot for this plant Gp3(z) with the new controller Gc3(z) is shown in Figure 13.

The actual system Bode plot for the dc-dc converter represented by this plant model Gp3(z) and controlled by the redesigned controller Gc3(z) is shown in Figure 14. It is again clear that the frequency domain characteristics match very closely between the actual and the designed values.

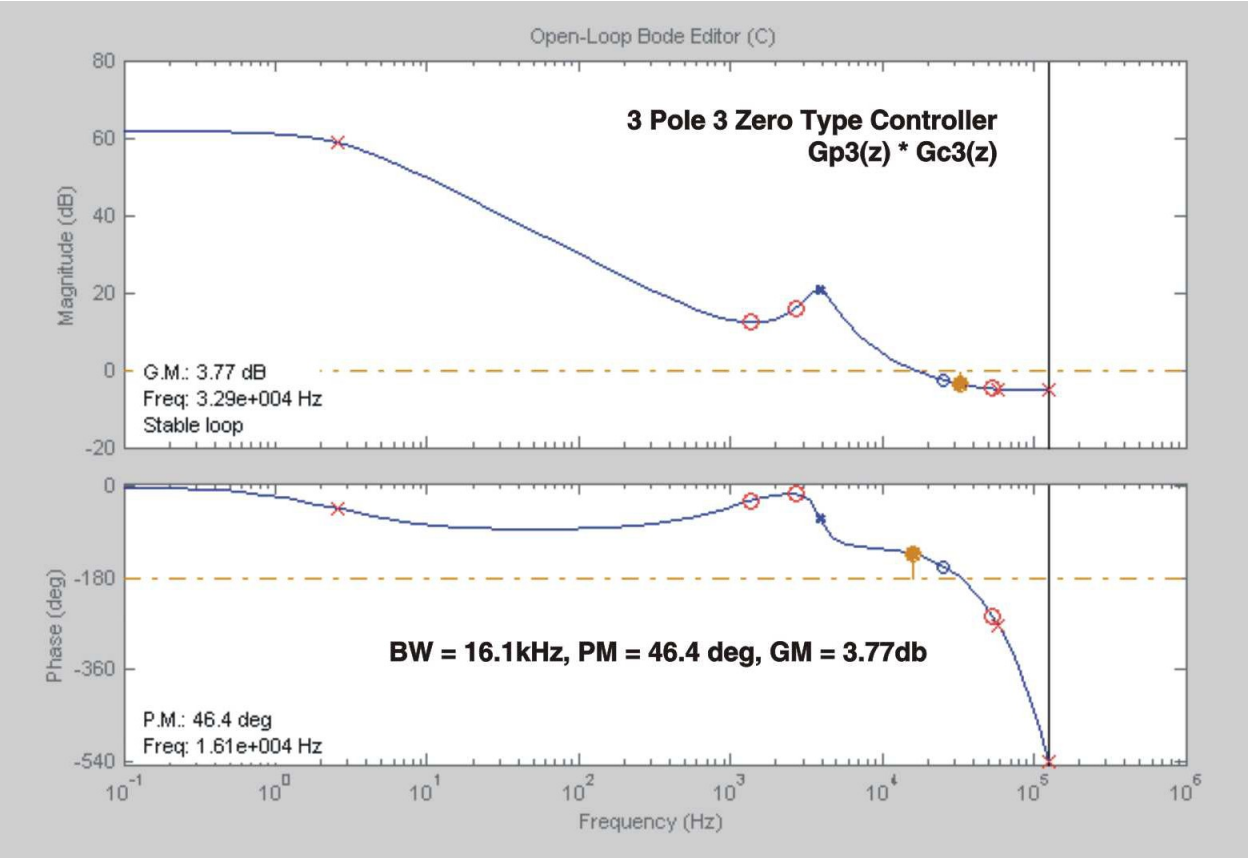

Figure 13. DC-DC Converter Digital Control Loop Bode Plot Gp3*Gc3 (MATLAB)

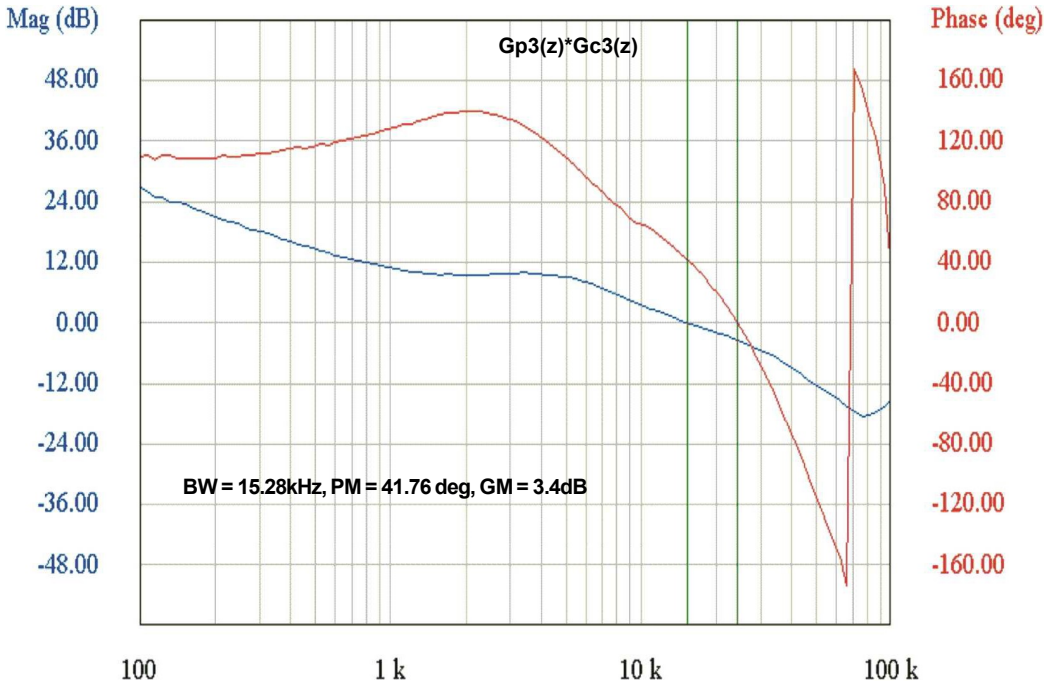

Figure 14. DC-DC Converter Load Transient Response (Loop gain = Gp3*Gc3)

Figure 15 shows the converter output voltage transient response with this controller. For a step load change of 15A, the output voltage settles within 50uSec (1% band). These test results again show the validity of the MATLAB based design approach as depicted in Figure 12 and Figure 13 above.

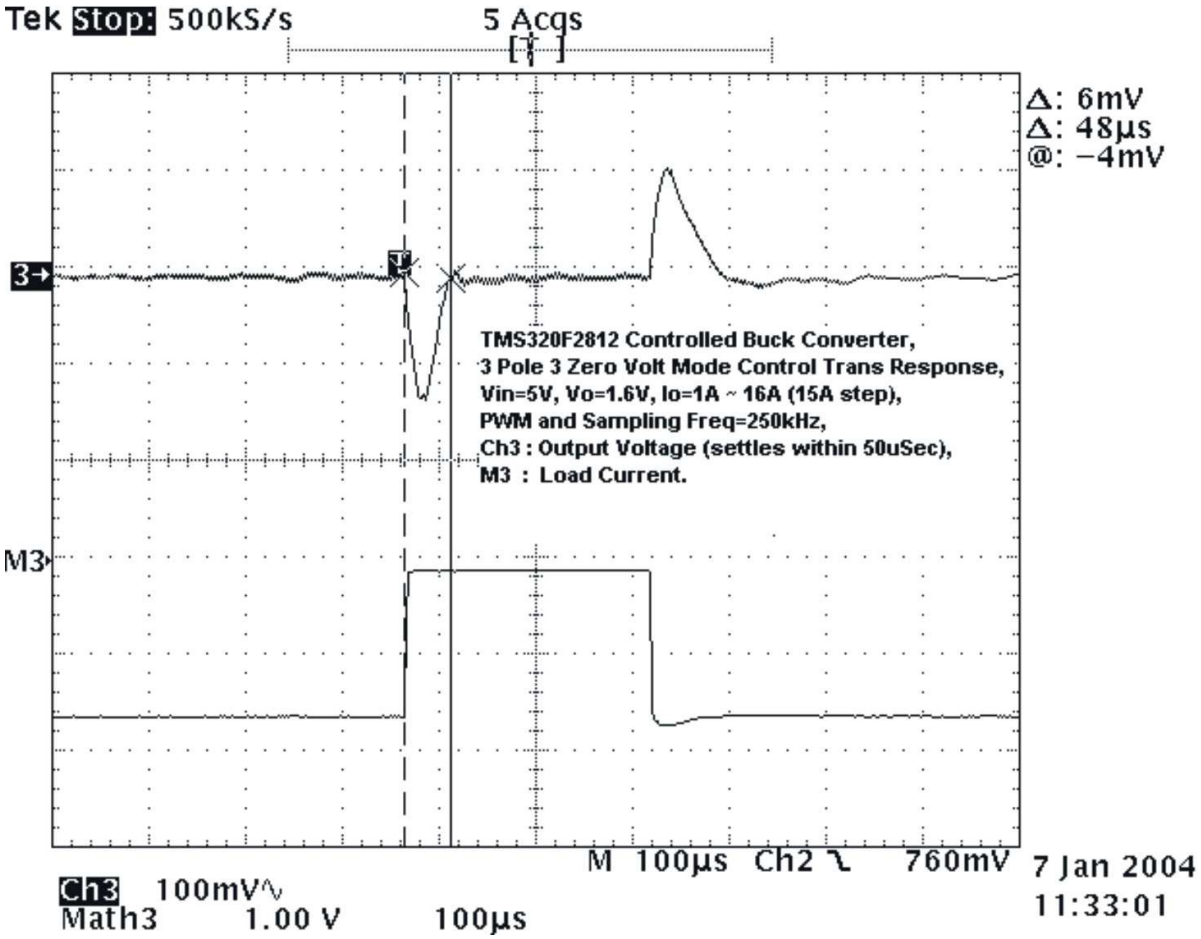

Figure 15. DC-DC Converter Load Transient Response (Loop gain = Gp3*Gc3)

3 Conclusion

DSP based digital control design methods for high frequency dc-dc buck converter is investigated using MATLAB based control design tools. Starting with a buck converter interfaced to a DSP controller, different control blocks and associated parameters are identified prior to the digital controller design. Two approaches to the digital controller design are presented. The first method, namely design by emulation, allows the power supply designers to do the control design in the familiar s-domain and then convert it to a discrete/digital controller. The second approach known as direct digital design, illustrates digital controller design directly in z-domain. It was found that the later approach results in a better dynamic performance for the closed loop operation of the converter. All of these MATLAB based designed controllers were finally validated by experimental results.

4 References

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