DM816x Easy CYG Package PCB Escape Routing

ABSTRACT

The DM816x CYG package is designed with a new technology called a Via Channel™ array. This technology allows for easy routing of the device in two signal and two power layers using large through-hole via diameters and standard trace widths; it is cost and time effective. Where more than four printed circuit board (PCB) layers are used, the routing is much more open and flexible than a regular BGA. This application report shows how to route the entire package by showing each quadrant up close and explaining the PCB feature sizes used. For this document, the Allegro® layout tool was used, although any PCB layout tool can be used.

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1 DM816x PCB Layout Technology

1.1 Via Channel Layout Advantages

Via Channel technology is a way of depopulating balls on the BGA chip package in a shape that makes it possible to have the vias concentrated in channels. This allows two important advantages.

- The via outside diameter (also known as the annular ring) can be larger than it normally would be if it had to be placed in between the balls, since all of the vias are placed in special areas called via channels. This makes manufacturing the PCB less expensive because 20/10 vias (vias with an outside diameter of 20 mils and a finished hole size of 10 mils) are possible. Smaller vias can also be used, but are not required.
- The vias are grouped in a radial pattern instead of a series of concentric rings around the middle of the chip, which is the case with normal BGA array PCB routing. The traces are more easily routed out of the inner parts of the chip because they are not restricted to the narrow paths in between many rows of through-hole vias. This allows reduced PCB layers because of the increased routing efficiency (more traces for every PCB layer). In the case of this chip, a four layer design is possible for all systems if PCB size is not crucial.

Figure 1 shows the resulting DM816x footprint. This shape has been separated down into quadrants. A quadrant is defined as one of four equal size squares making up the whole. The upper left square is called quadrant 1 and so on.

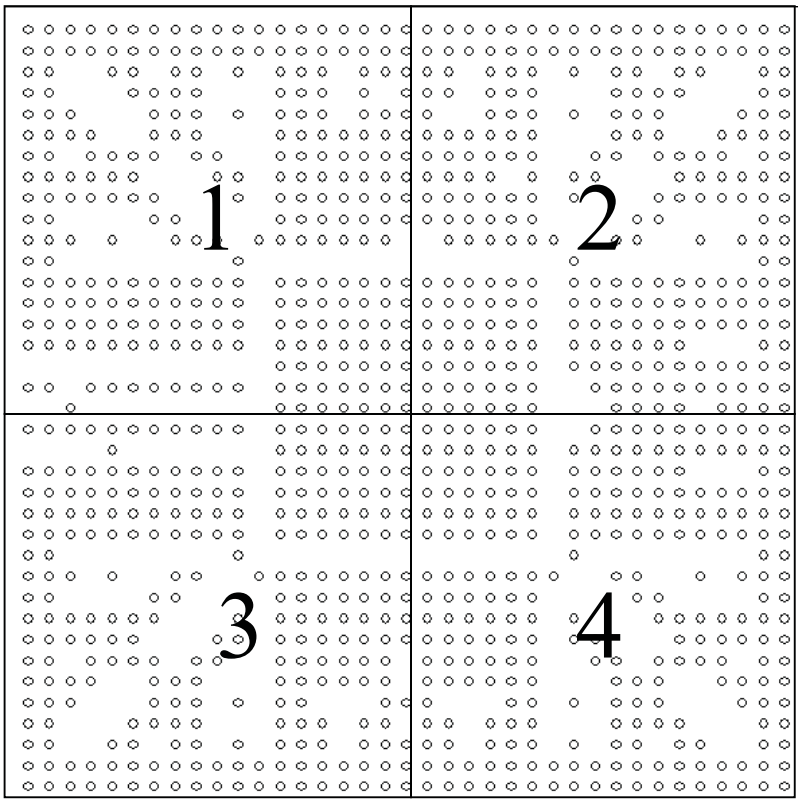

Figure 1. DM816x Footprint With Via Channel Array

NOTE: The finished routing from the EVM (as shown) is available on the TI website (in the DaVinci SoC Products) located at: http://www.ti.com/lsds/ti/dsp/video_processors/dm81x/products.page in Allegro format. This layout is a six layer PCB due to time constraints, but uses only two signal layers as shown here.

1.2 DM816x PCB Layout Feature Sizes and Constraints

The overall PCB layout rules for routing this footprint (and the sizes used in this document) are as follows:

- 0.3mm BGA pad (as suggested by IPC standard 7351A and TI reliability studies)
- 4 mil (0.1mm) minimum trace size
- 4 mil (0.1mm) minimum clearance between traces and vias
- 20 mil (0.50mm) minimum via diameter
- 10 mil (0.25mm) minimum finished hole diameter

NOTE: It is helpful to do all routing using a metric measurement system on the CAD software. Using standard measurements (mils) with successive copy commands will compound rounding errors and can result in design rule violations.

If done correctly, the results will be:

- No blind, stacked, buried, or micro vias necessary
- Only two signal layers required

This application report shows one example of a DM816x routing. There are many ways to route the same chip. Feel free to use this example in any way that is helpful.

The following illustrations show the EVM layout on the only two signal layers (top and bottom).

2 DM816x PCB Routing Detail

2.1 Package Quadrant Pictures

Figure 2 shows the overall routing of the first quadrant. In the following pages it will be broken up into simpler parts.

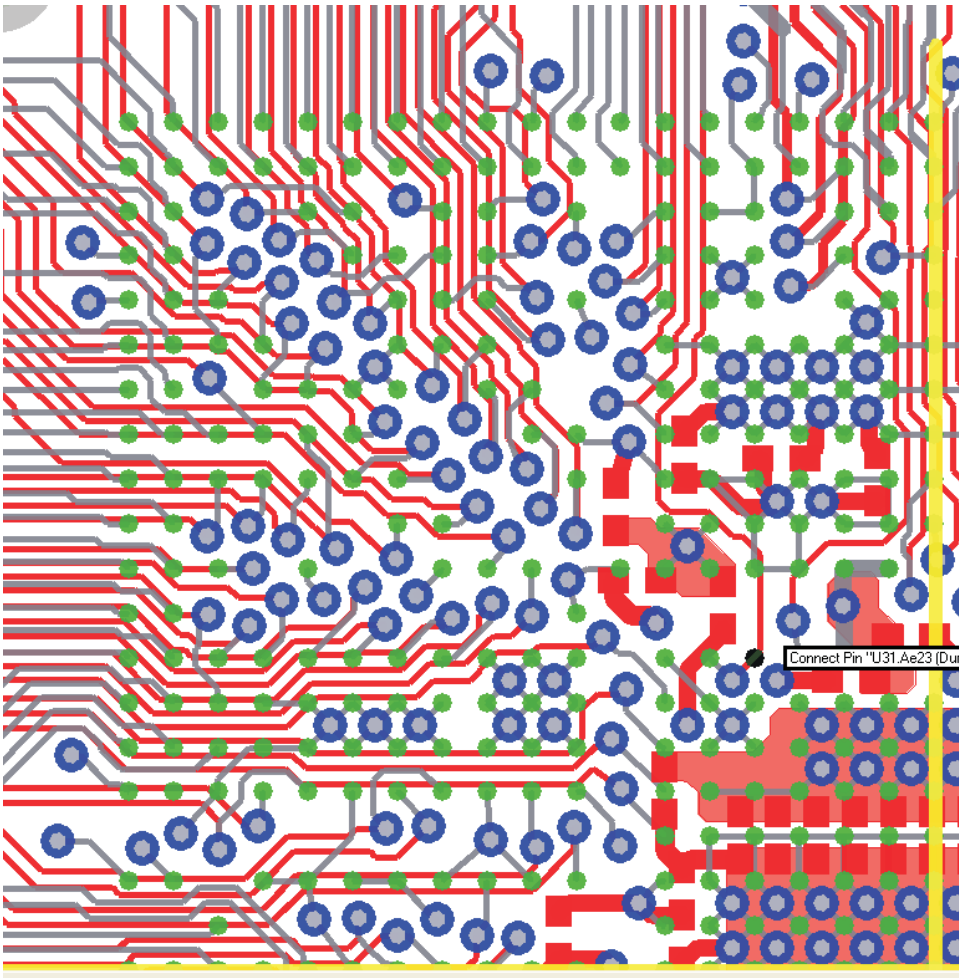

Figure 2. First Quadrant (Upper Left) Routing (top and bottom layers)

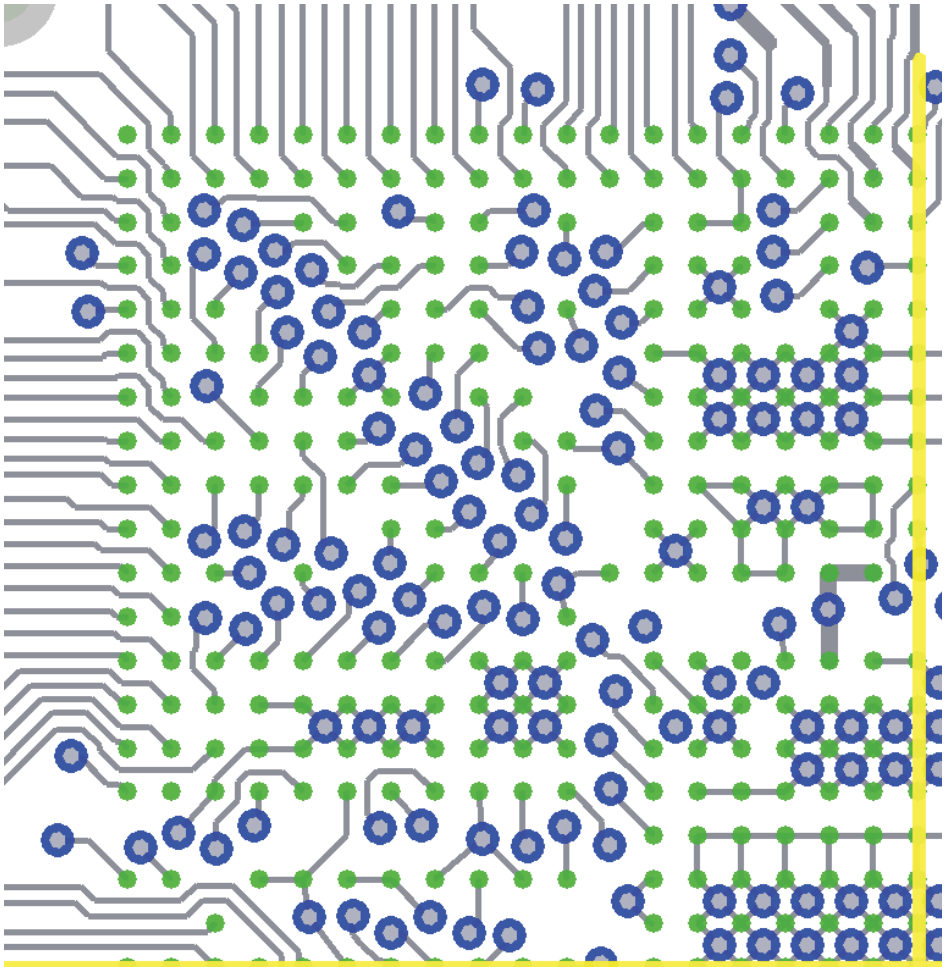

Figure 3. First Quadrant Top Layer

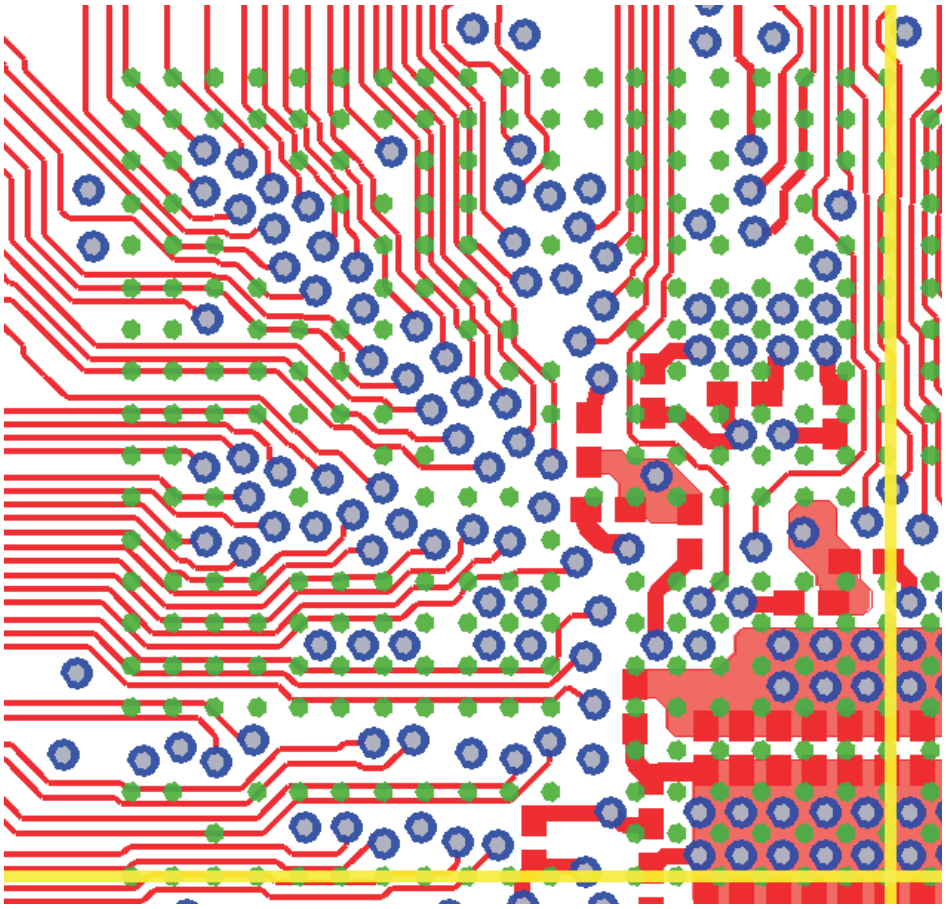

Figure 4. First Quadrant Bottom Layer

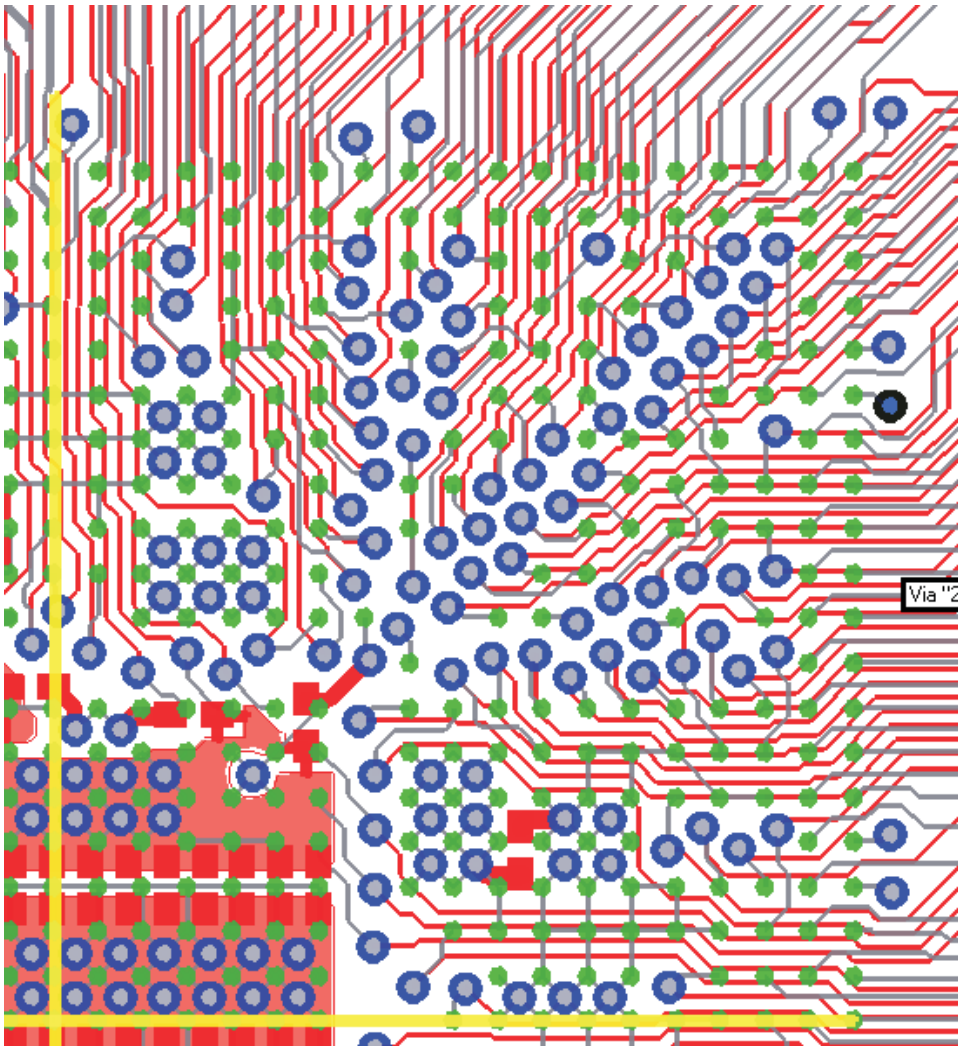

Figure 5. Second Quadrant Routing (top and bottom layers)

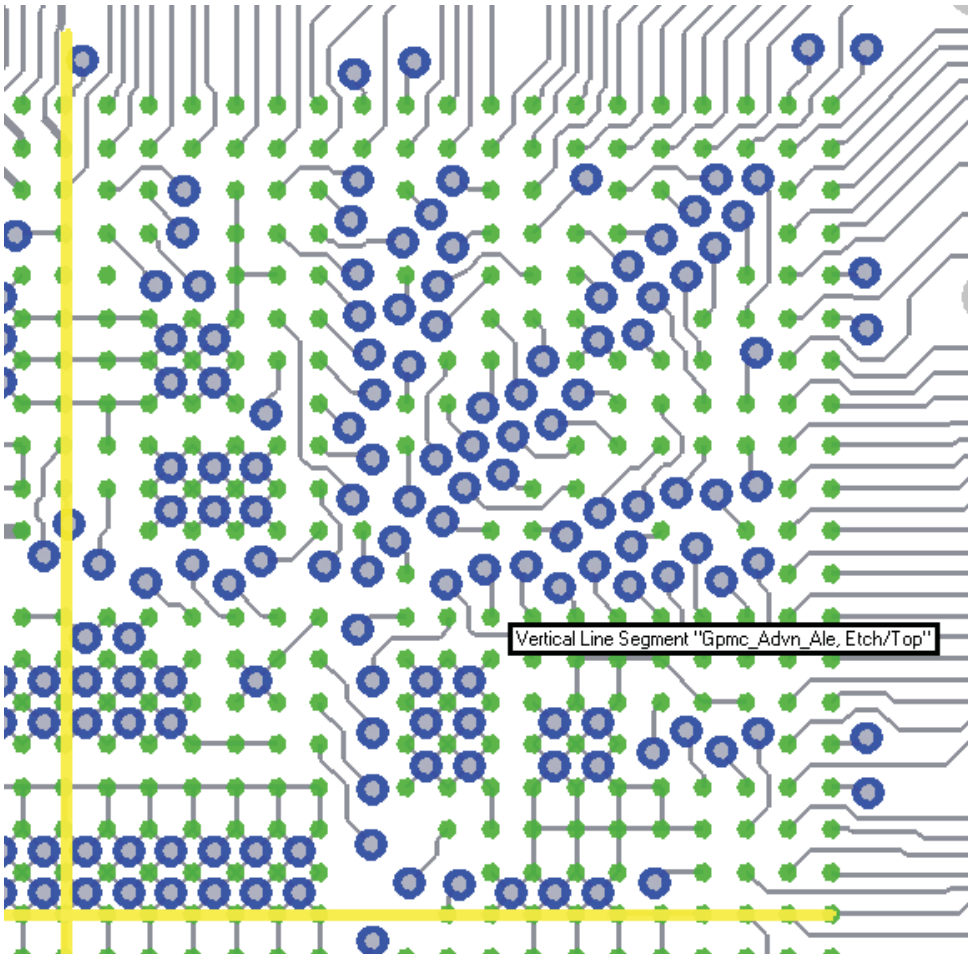

Figure 6. Second Quadrant Top Layer

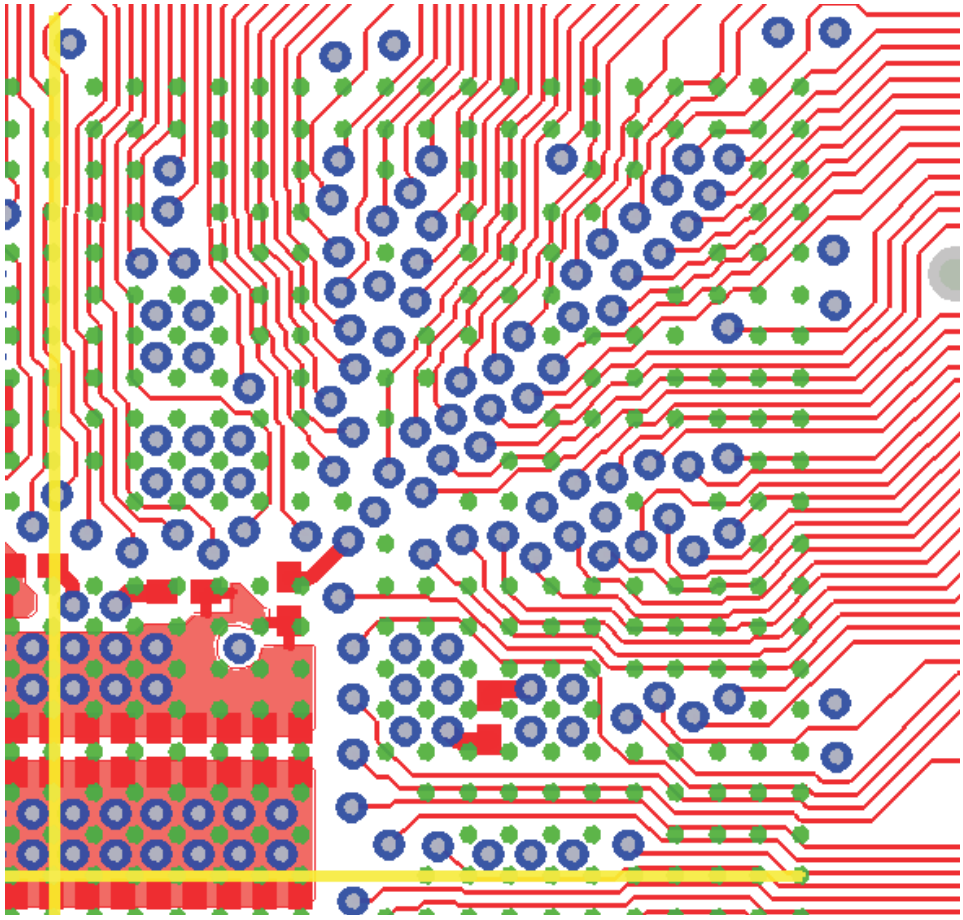

Figure 7. Second Quadrant Bottom Layer

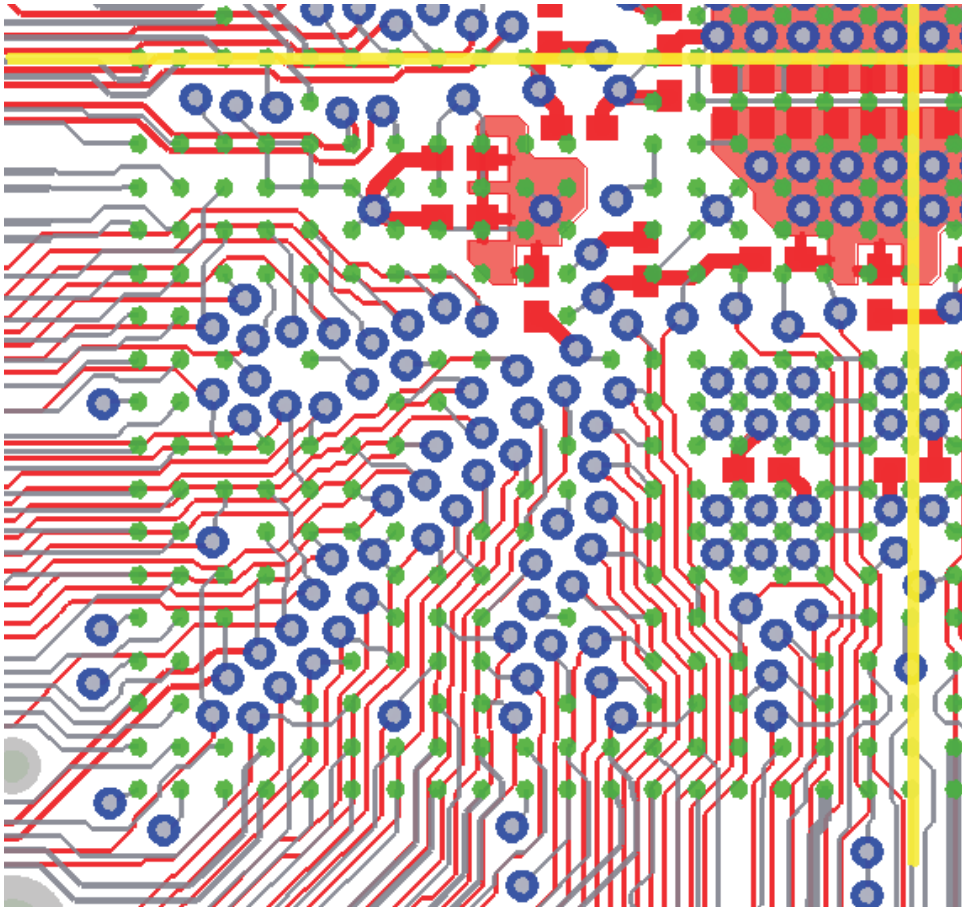

Figure 8. Third Quadrant Routing (top and bottom layers)

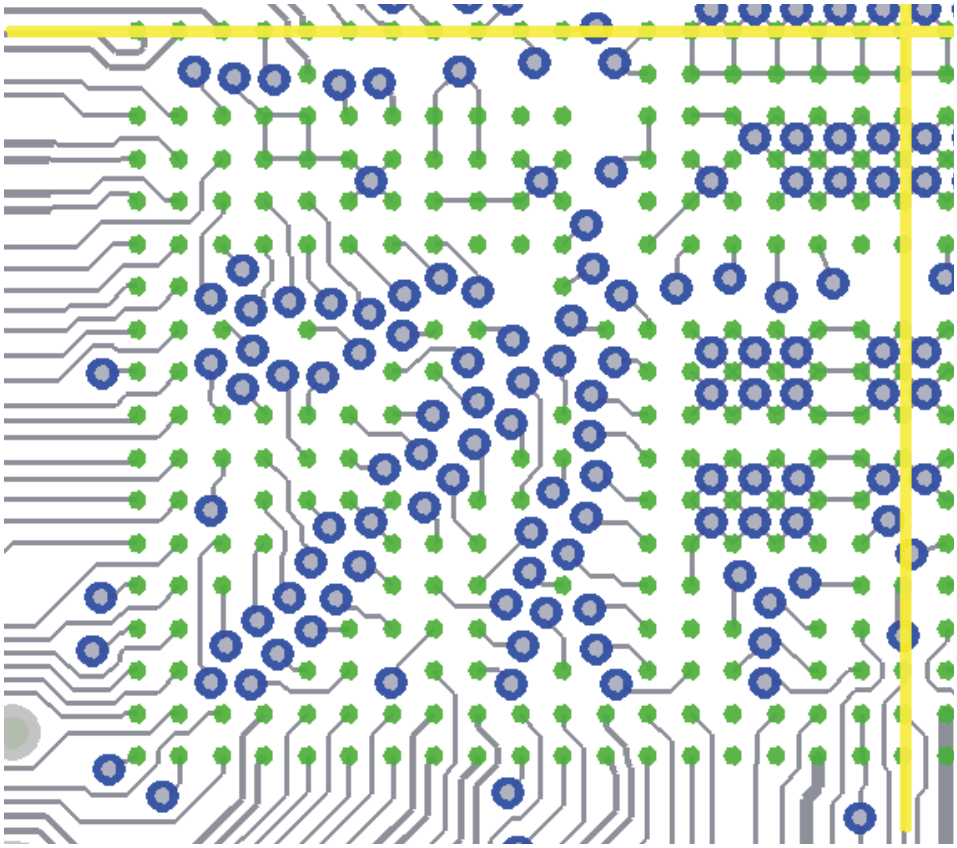

Figure 9. Third Quadrant Top Layer

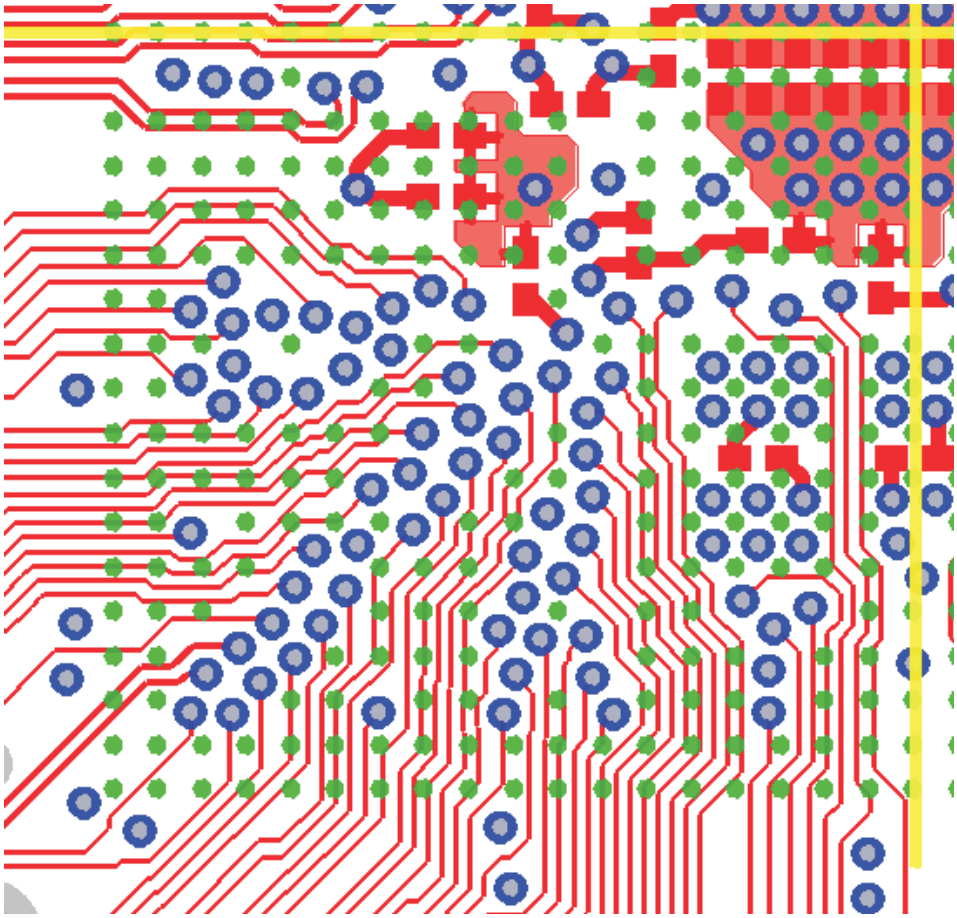

Figure 10. Third Quadrant Bottom Layer

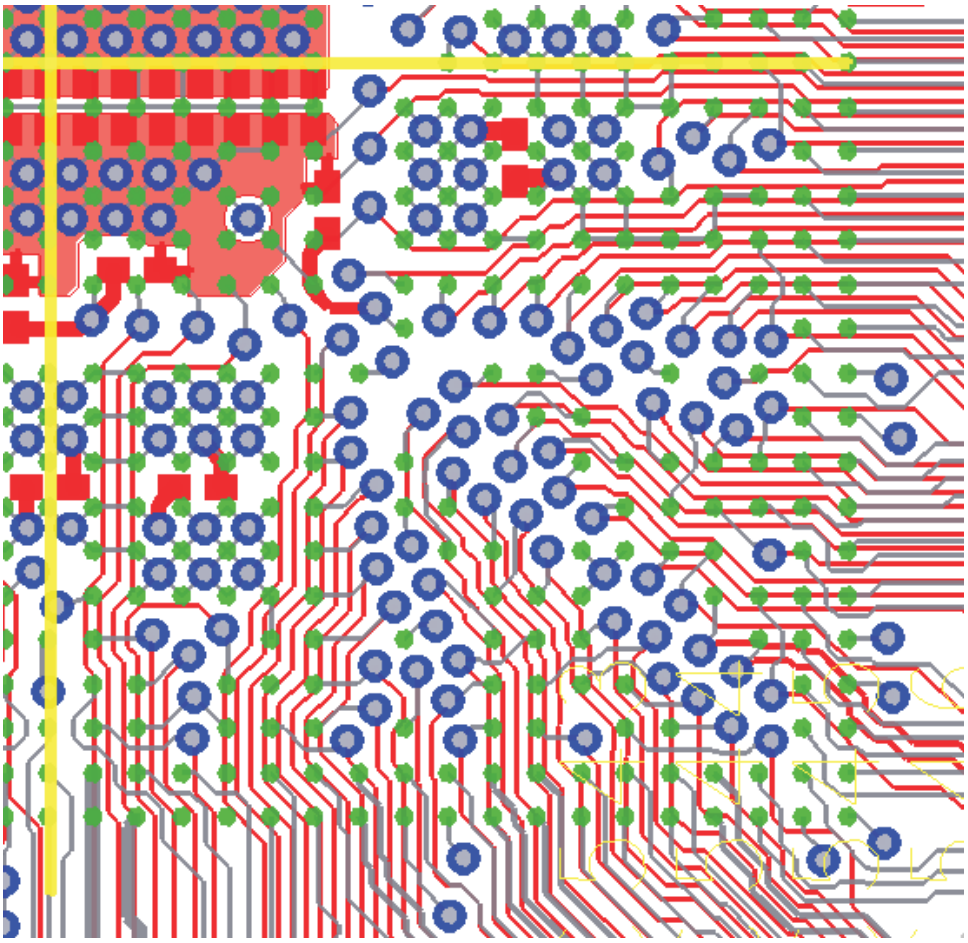

Figure 11. Fourth Quadrant Routing (top and bottom layers)

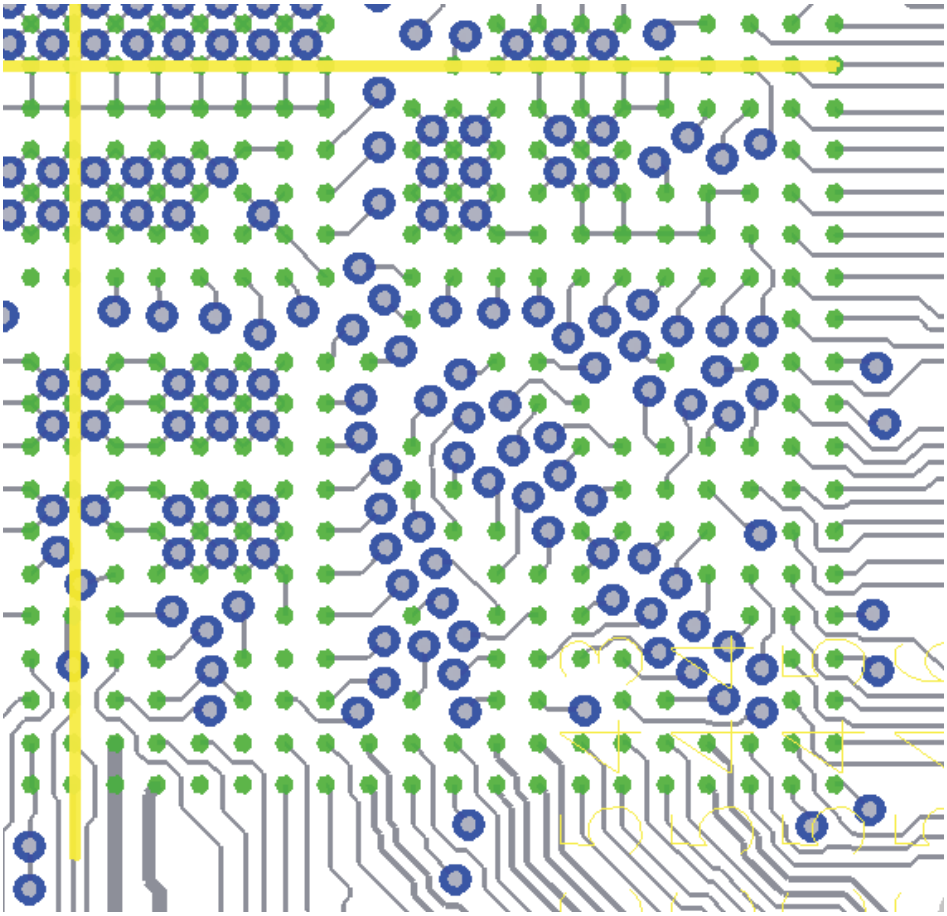

Figure 12. Fourth Quadrant Top Layer

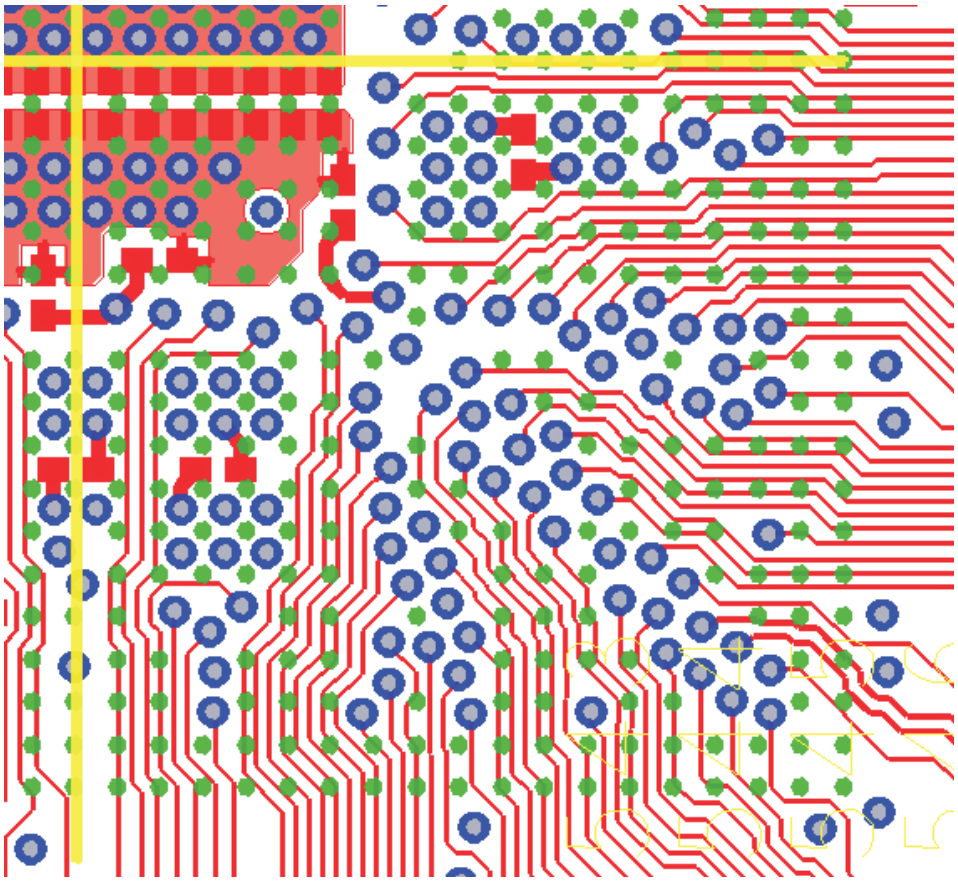

Figure 13. Fourth Quadrant Bottom Layer

2.2 Special Vias in Power/Gnd Area

Shown here in the center of the chip are vias placed between balls. These vias are only used in the power/ground area between balls of the same net.

It is possible to put vias with a large diameter pad in between four balls of the same net in the power and ground area since the copper pour of this area will take the place of the upper pad. Putting vias with a 20 mil (0.5 mm) pad in between four 0.3 mm ball pads of a 0.65 mm pitch part would normally cause design rule check (DRC) errors because there isn't 0.1 mm of room on all sides for a pad this size. However, since the copper pour of the area takes the place of the pad on the top layer anyway, the size of the top layer pad is not important.

There are several options to avoid an intentional DRC in these cases:

- Turn off the minimum clearance between nets of the same name (Allegro and probably many other CAD tools can do this). This will ignore what would otherwise be clearance violations between two PCB features on the same net. This is suggested as the best option since it doesn't require altering the PCB.
- Define and use a special via in these areas (only in between four balls of the same net) with this stackup:

Top layer:	→	16 mil (0.4 mm) diameter via pad
Middle layers:	→	20 mil (0.5 mm) or 18 mil (0.45 mm) diameter via pad
Bottom layer:	→	20 mil (0.5 mm) or 18 mil (0.45 mm) diameter via pad
Hole size:	→	10 mil (0.25 mm) finished hole

A 16 mil (0.4 mm) top layer pad diameter will fit in between four ball pads without a DRC on a 4 mil (0.1 mm) clearance and 20 mil (0.5 mm) lower and bottom layer pad diameters with a 10 mil (0.25 mm) finished hole size. This should not violate most board shop's rules, however, it may be necessary to explain to the board shop that you are not actually designing a 16 mil via pad with a 10 mil hole since the upper pad size does not affect the copper pour.

By doing one of the above it is possible to put in extra power and ground vias to more closely couple the power and ground voltages on the top and power and ground layers.

Now, you are done and ready to route the rest of your design!

Revision History

Changes from Original (August 2011) to A Revision	Page
• Update was made in Section 2.2.	16

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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