Application Report
SPRABM1A–November 2011–Revised December 2011

Migrating from TMS320C5515/05 to TMS320C5535/34/33/32

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ABSTRACT

This document provides the minimum changes required to migrate from TMS320C5515/05 to TMS320C5535/34/33/32. Enhancements or new features of the TMS320C5535/34/33/32 devices that do not affect migrating from the TMS320C5515/05 devices will also be briefly mentioned in this document.

All efforts have been made to provide a comprehensive list of changes. An update will be provided if additional changes are identified.

The TMS320C5515/05 devices will henceforth be referred to as C5515/05 in this document. The TMS320C5535/34/33/32 devices will henceforth be referred to as C5535/34/33/32 in this document.

More information on the C5535/34/33/32 DSP can be found in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Fixed-Point Digital Signal Processors Data Manual* (literature number SPRS737).

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1 Overview

The following table shows the major differences between the two devices. Peripherals that are not included in the table have no changes.

Table 1. Device Differences

	C5535/34/33/32		C5515/05
Max CPU Speed (PLL output)	50 MHz at 1.05 V 50/100 MHz at 1.3 V		60/75 MHz at 1.05 V 100/120 MHz at 1.3 V 150 MHz at 1.4 V (only C5505)
On-chip Memory	C5535	320KB	320KB
	C5534	256KB	
	C5533	128KB	
	C5532	64KB	
USB_LDO	C5535, C5534, and C5533		C5515
DSP_LDO	C5535 and C5534		C5515
Bootloader	Boot both encrypted and unencrypted images from 16-bit SPI EEPROM, 24-bit SPI serial flash, I2C EEPROM, SD/SDHC/eMMC/moviNAND, UART, and USB		Boot both encrypted and unencrypted images from NAND, NOR, 16-bit SPI EEPROM, 24-bit SPI serial flash, I2C EEPROM but only encrypted images from SD/SDHC/MMC/eMMC, and USB
Pins and Peripherals	144-pin BGA (ZHH Suffix) No EMIF support		196-pin BGA (ZCH Suffix) EMIF Support
FFT Coprocessor (C5535 only)	HWA FFT API Address 00fefe9c _hwafft_br 00fefeb0 _hwafft_8pts 00feff9f _hwafft_16pts 00ff00f5 _hwafft_32pts 00ff03fe _hwafft_64pts 00ff0593 _hwafft_128pts 00ff07a4 _hwafft_256pts 00ff09a2 _hwafft_512pts 00ff0c1c _hwafft_1024pts		HWA FFT API Address 0x00ff6cd6 _hwafft_br 0x00ff6cea _hwafft_8pts 0x00ff6dd9 _hwafft_16pts 0x00ff6f2f _hwafft_32pts 0x00ff7238 _hwafft_64pts 0x00ff73cd _hwafft_128pts 0x00ff75de _hwafft_256pts 0x00ff77dc _hwafft_512pts 0x00ff7a56 _hwafft_1024pts

2 Operating Conditions

2.1 Operating Voltages and CPU Speeds

Table 2. Operating Voltages and CPU Speeds for C5535/34/33/32 and C5515/05

Supply Pins	C5535/34/33/32		C5515/05	
CV_{DD}	1.05 V	50 MHz	1.05 V	60/75 MHz
	1.3 V	50/100 MHz	1.3 V	100/120 MHz
	N/A	N/A	1.4 V	150 MHz (C5505 only)
All other power domains	No changes			

Table 3. On-Chip RAM Availability

On-Chip RAM	Device				
	C5535	C5534	C5533	C5532	C5515/05
320KB	x(1)	-(2)	-	-	x
256KB	x	x	-	-	x
128KB	x	x	x	-	x
64KB	x	x	x	x	x

(1) x — Supported
(2) - — Not supported

3 Low-Dropout Regulators (LDOs)

Table 4. LDO Availability

LDO	Device					
	C5535	C5534	C5533	C5532	C5515	C5505
ANA_LDO	x(1)	x	x	x	x	x
USB_LDO	x	x	x	-(2)	x	-
DSP_LDO	x	x	-	-	x	-

(1) x — Supported
(2) - — Not supported

For the 50-MHz devices, DSP_LDO must be programmed to 1.05 V to match the core voltage, CV_{DD}, for proper operation after reset. This is because DSP_LDO is enabled to 1.3 V when coming out of reset.

4 Pin and Package Considerations

4.1 Package

The C5535/34/33/32 uses the 144-pin, 12x12 mm, Green (Pb-free and environmentally friendly) ZHH package. For more information, see the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number SPRS737). The C5515/05 uses the 196-pin, 10x10 mm, Green (Pb-free and environmentally friendly) ZCH package.

4.2 Pin Compatibility

Due to differences between the C5535/34/33/32 and C5515/05 packages, they are **not** pin-to-pin compatible.

4.3 Peripheral Changes

Table 5. Peripheral Availability

Peripheral	Device				
	C5535	C5534	C5533	C5532	C5515/05
USB	x(1)	x	x	-(2)	x
LCD Interface	x	-	-	-	x
HWA FFT	x	-	-	-	x
SAR ADC	x	-	-	-	x

(1) x — Supported
(2) - — Not supported

4.4 Pin Maps

Figure 1 through Figure 4 show the pin maps of the C5535/34/33/32 devices.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	V_{SS}	LCD_D[4]/ GP[14]	LCD_D[6]/ GP[16]	$\overline{TRST}$	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	LCD_D[7]/ GP[17]	LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	V_{SS}
N	TDO	LCD_RW_ WRB/SPI_ CS2	TCK	LCD_D[0]/ SPI_RX	LCD_D[3]/ GP[13]	TMS	LCD_D[5]/ GP[15]	DV_{DDIO}	CV_{DD}	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	DV_{DDIO}	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV_{DDIO}
M	EMU1	LCD_CS1_E1/ SPI_CS1	DV_{DDIO}	DV_{DDIO}	LCD_RS/ SPI_CS3	CV_{DD}	V_{SS}	SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}	SD0_CMD/ I2S0_FS/ GP[1]	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	LCD_CS0_ E0/SPI_CS0	EMU0	LCD_EN_ RDB/ SPI_CLK	DV_{DDIO}	V_{SS}					V_{SS}	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	LCD_D[1]/ SPI_TX	TDI	V_{SS}	V_{SS}							CV_{DD}	RSV1	USB_V_{DD1P3}	USB_V_{SS1P3}
J	SD0_D0/ I2S0_DX/ GP[2]	LCD_D[2]/ GP[12]	XF									USB_V_{SSA1P3}	V_{SS}	USB_DM
H	RSV10	CV_{DD}	V_{SS}									USB_ V_{DDA1P3}	USB_V_{SSA3P3}	USB_DP
G	RSV9	RSV12	CV_{DD}									USB_V_{DDA3P3}	USB_V_{DDPLL}	USB_R1
F	RSV8	CV_{DD}	V_{SS}									USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DD1P3}
E	RSV7	RSV11	V_{SS}	V_{SS}							V_{SS}	USB_V_{DD1P3}	USB_V_{DDOSC}	USB_MXI
D	CLK_SEL	$\overline{RESET}$	CV_{DD}	V_{SS}	V_{SS}					V_{SS}	CV_{DD}	USB_V_{SSOSC}	USB_LDOO	USB_MXO
C	CLKIN	$\overline{INT0}$	DV_{DDRTC}	SCL	V_{SSRTC}	DV_{DDIO}	V_{DDA_PLL}	V_{SS}	V_{SSA_ANA}	BG_CAP	CV_{DD}	V_{SS}	$\overline{DSP\_LDO\_EN}$	LDOI
B	$\overline{INT1}$	V_{SS}	V_{SS}	CV_{DDRTC}	CV_{DDRTC}	V_{SSA_ANA}	V_{DDA_ANA}	GPAIN1	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V_{SSA_PLL}	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	GPAIN0	GPAIN2	GPAIN3	RSV4	RSV0	DSP_LDOO	V_{SS}

Figure 1. C5535 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	V_{SS}	GP[14]	GP[16]	$\overline{TRST}$	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V_{SS}
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV_{DDIO}	CV_{DD}	I2S2_FS/ GP[19]/ SPI_CS0	DV_{DDIO}	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV_{DDIO}
M	EMU1	SPI_CS1	DV_{DDIO}	DV_{DDIO}	SPI_CS3	CV_{DD}	V_{SS}	SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV_{DDIO}	V_{SS}					V_{SS}	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	SPI_TX	TDI	V_{SS}	V_{SS}							CV_{DD}	RSV1	USB_V_{DD1P3}	USB_V_{SS1P3}
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_V_{SSA1P3}	V_{SS}	USB_DM
H	RSV10	CV_{DD}	V_{SS}									USB_ V_{DDA1P3}	USB_V_{SSA3P3}	USB_DP
G	RSV9	RSV12	CV_{DD}									USB_V_{DDA3P3}	USB_V_{DDPLL}	USB_R1
F	RSV8	CV_{DD}	V_{SS}									USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DD1P3}
E	RSV7	RSV11	V_{SS}	V_{SS}							V_{SS}	USB_V_{DD1P3}	USB_V_{DDOSC}	USB_MXI
D	CLK_SEL	$\overline{RESET}$	CV_{DD}	V_{SS}	V_{SS}					V_{SS}	CV_{DD}	USB_V_{SSOSC}	USB_LDOO	USB_MXO
C	CLKIN	$\overline{INT0}$	DV_{DDRTC}	SCL	V_{SSRTC}	DV_{DDIO}	V_{DDA_PLL}	V_{SS}	V_{SSA_ANA}	BG_CAP	CV_{DD}	V_{SS}	$\overline{DSP\_LDO\_EN}$	LDOI
B	$\overline{INT1}$	V_{SS}	V_{SS}	CV_{DDRTC}	CV_{DDRTC}	V_{SSA_ANA}	V_{DDA_ANA}	NC	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V_{SSA_PLL}	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_LDOO	V_{SS}

Figure 2. C5534 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	V_{SS}	GP[14]	GP[16]	$\overline{TRST}$	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V_{SS}
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV_{DDIO}	CV_{DD}	I2S2_FS/ GP[19]/ SPI_CS0	DV_{DDIO}	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV_{DDIO}
M	EMU1	SPI_CS1	DV_{DDIO}	DV_{DDIO}	SPI_CS3	CV_{DD}	V_{SS}	SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV_{DDIO}	V_{SS}					V_{SS}	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	SPI_TX	TDI	V_{SS}	V_{SS}							CV_{DD}	RSV1	USB_V_{DD1P3}	USB_V_{SS1P3}
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_V_{SSA1P3}	V_{SS}	USB_DM
H	RSV10	CV_{DD}	V_{SS}									USB_ V_{DDA1P3}	USB_V_{SSA3P3}	USB_DP
G	RSV9	RSV12	CV_{DD}									USB_V_{DDA3P3}	USB_V_{DDPLL}	USB_R1
F	RSV8	CV_{DD}	V_{SS}									USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DD1P3}
E	RSV7	RSV11	V_{SS}	V_{SS}							V_{SS}	USB_V_{DD1P3}	USB_V_{DDOSC}	USB_MXI
D	CLK_SEL	$\overline{RESET}$	CV_{DD}	V_{SS}	V_{SS}					V_{SS}	CV_{DD}	USB_V_{SSOSC}	USB_LDOO	USB_MXO
C	CLKIN	$\overline{INT0}$	DV_{DDRTC}	SCL	V_{SSRTC}	DV_{DDIO}	V_{DDA_PLL}	V_{SS}	V_{SSA_ANA}	BG_CAP	CV_{DD}	V_{SS}	$\overline{DSP\_LDO\_EN}$ (1)	LDOI
B	$\overline{INT1}$	V_{SS}	V_{SS}	CV_{DDRTC}	CV_{DDRTC}	V_{SSA_ANA}	V_{DDA_ANA}	NC	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V_{SSA_PLL}	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_LDOO (2)	V_{SS}

(1) DSP_LDOO is not supported on the TMS320C5533. An external power supply is used to provide power to CV_{DD}, $\overline{DSP\_LDO\_EN}$ should be tied to LDOI, and DSP_LDOO should be left unconnected. The $\overline{RESET}$ pin must be asserted appropriately for device initialization after power up.

(2) DSP_LDOO is not supported on the TMS320C5533. For proper device operation, this pin must be left connected. DSP_LDOO can be enabled to provide a regulated 1.3- or 1.05-V output only to the internal POR to support the RTC-only mode. For more information, see the *RTC Only Mode* section in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number SPRS737).

Figure 3. C5533 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
P	V_{SS}	GP[14]	GP[16]	$\overline{TRST}$	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V_{SS}
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV_{DDIO}	CV_{DD}	I2S2_FS/ GP[19]/ SPI_CS0	DV_{DDIO}	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV_{DDIO}
M	EMU1	SPI_CS1	DV_{DDIO}	DV_{DDIO}	SPI_CS3	CV_{DD}	V_{SS}	SD0_CLK/ I2S0_CLK/ GP[0]	CV_{DD}	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV_{DDIO}	V_{SS}					V_{SS}	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_V_{BUS}
K	SPI_TX	TDI	V_{SS}	V_{SS}							CV_{DD}	RSV1	USB_V_{DD1P3}	USB_V_{SS1P3}
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_V_{SSA1P3}	V_{SS}	USB_DM
H	RSV10	CV_{DD}	V_{SS}									USB_ V_{DDA1P3}	USB_V_{SSA3P3}	USB_DP
G	RSV9	RSV12	CV_{DD}									USB_V_{DDA3P3}	USB_V_{DDPLL}	USB_R1
F	RSV8	CV_{DD}	V_{SS}									USB_V_{SSREF}	USB_V_{SSPLL}	USB_V_{DD1P3}
E	RSV7	RSV11	V_{SS}	V_{SS}							V_{SS}	USB_V_{DD1P3}	USB_V_{DDOSC}	USB_MXI
D	CLK_SEL	$\overline{RESET}$	CV_{DD}	V_{SS}	V_{SS}					V_{SS}	CV_{DD}	USB_V_{SSOSC}	USB_ LDOO(1)	USB_MXO
C	CLKIN	$\overline{INT0}$	DV_{DDRTC}	SCL	V_{SSRTC}	DV_{DDIO}	V_{DDA_PLL}	V_{SS}	V_{SSA_ANA}	BG_CAP	CV_{DD}	V_{SS}	$\overline{DSP\_LDO\_EN}$(2)	LDOI
B	$\overline{INT1}$	V_{SS}	V_{SS}	CV_{DDRTC}	CV_{DDRTC}	V_{SSA_ANA}	V_{DDA_ANA}	NC	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V_{SSA_PLL}	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_ LDOO(3)	V_{SS}

(1) USB_LDOO is not supported on the TMS320C5532. For proper device operation, this pin must be left unconnected.

(2) DSP_LDOO is not supported on the TMS320C5532. An external power supply is used to provide power to CV_{DD}, $\overline{DSP\_LDO\_EN}$ should be tied to LDOI, and DSP_LDOO should be left unconnected. The $\overline{RESET}$ pin must be asserted appropriately for device initialization after power up.

(3) DSP_LDOO is not supported on the TMS320C5532. For proper device operation, this pin must be left connected. DSP_LDOO can be enabled to provide a regulated 1.3- or 1.05-V output only to the internal POR to support the RTC-only mode. For more information, see the *RTC Only Mode* section in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number SPRS737).

Shaded pins are not supported on this device. To ensure proper device operation, these pins must be hooked up properly. For more information, see the *Unsupported USB 2.0 Terminal Functions* section in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number SPRS737).

Figure 4. C5532 Pin Map

5 Bootloader

The C5535/34/33/32 bootloader includes the following changes to support new features:

- Adds unencrypted boot image from SD/SDHC/eMMC/moviNAND, UART, and USB
- Supports reauthoring for 16-bit SPI EEPROM, I2C EEPROM, and SD/SDHC/eMMC/moviNAND
- Does not support NOR, NAND, and MMC

See the *Boot Sequence* section in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number SPRS737) for details.

Revision History

Changes from Original (November, 2011) to A Revision **Page**

- Changed description of $\overline{\text{DSP\_LDO\_EN}}$ pin 7
- Added description of DSP_LDOO pin 7
- Added description of USB_LDOO pin 8
- Added description of $\overline{\text{DSP\_LDO\_EN}}$ pin 8
- Added description of DSP_LDOO pin 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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