

Digital Control of Two Phase Interleaved PFC and Motor Drive Using MCU With CLA

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ABSTRACT

Power factor correction (PFC) is used in power systems operating from single phase AC to correct for the non linearity of the rectifier. Use of PFC in motor drives is increasing because of increased regulation from the power utility side. However, integration of PFC and field oriented control of motor on a single controller remains challenging from a processor bandwidth point of view while keeping system costs down. The integration also brings challenges like better control of PFC output voltage under dynamic load and line condition while maintaining high input power factor. In this application report, a motor control and PFC development hardware platform using a low cost microcontroller (MCU) is presented. Software and system integration challenges are illustrated and improvements to PFC algorithm using non linear control technique and anti windup integral controller are shown. It is further shown how the use of small footprint control law accelerator (CLA) processor enables offloading control of PFC algorithm from the main core thus freeing up bandwidth to enable higher switching frequency operation of the power stage.

Contents

| | | |
|---|-------------------------------------|----|
| 1 | Introduction | 2 |
| 2 | Hardware Platform | 3 |
| 3 | System Design and Integration | 5 |
| 4 | Results | 9 |
| 5 | Conclusion | 12 |
| 6 | References | 12 |

List of Figures

| | | |
|----|--|----|
| 1 | Three Phase Motor Operating From Single Phase Supply | 2 |
| 2 | Motor Control and Power Factor Correction Hardware Platform | 3 |
| 3 | Motor Control and Power Factor Correction Hardware Platform | 4 |
| 4 | Control Law Accelerator | 5 |
| 5 | Interrupt vs Task Driven Machine..... | 5 |
| 6 | PFC Implemented on the CLA and Motor Control on C28x..... | 6 |
| 7 | Timing Diagram for PFC and Motor Control Application Integration | 7 |
| 8 | FOC of AC Induction Motor..... | 8 |
| 9 | Digital Control Algorithm of Interleaved PFC Stage | 8 |
| 10 | Non-Linear Control of PFC | 9 |
| 11 | Linear Volt Loop Control | 10 |
| 12 | Non-Linear Volt Loop | 10 |
| 13 | Linear Volt Loop Control | 10 |
| 14 | Non-Linear Volt Loop | 11 |
| 15 | No Anti-Integral Windup | 11 |
| 16 | With Anti-Integral Windup | 11 |

1 Introduction

Three phase motors are used in wide variety of applications operating from single phase AC supply. However, the use of the AC rectifier and capacitors causes the drawn current to be distorted, because of the nonlinearity of the rectification stage, therefore, the power factor is compromised. With various regulations limiting the input current harmonic content, especially with the IEC 61000-3-2 standard that defines the harmonic components that an electronic load may inject into the supply line, a PFC stage has become an integral part of most rectifier designs.

A typical 3-phase motor system operating from a single phase supply with power factor correction consists of three major power stages:

- AC rectifier to rectify the input AC voltage
- Boost PFC power stage
- Motor inverter stage

The system is illustrated in [Figure 1](#).

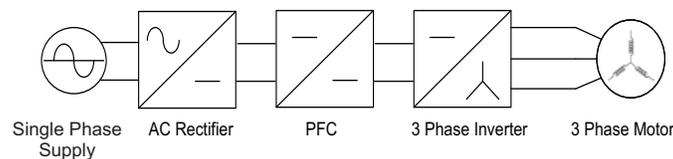


Figure 1. Three Phase Motor Operating From Single Phase Supply

In this 3 phase motor system PFC is used to improve the power factor of the input current waveform while regulating the DC Bus supplied to the inverter stage of the motor. Thus the motor stage acts as a load for the PFC stage. The PFC stage shapes the current drawn from the mains such that it follows the input AC voltage.

The use of PFC has been shown to result in several system advantages, some of which are listed below:

- Improvement in power factor and reduction in THD induced on the mains line
- Reduction in DC bus capacitance, reducing system cost
- Reduction in inrush current resistor size and losses
- Capability to implement variable DC bus control on a low-cost platform that enables efficient motor control application

Some of these improvements not only result in direct cost savings but also improve the system life span, resulting in compounded advantages. However, for these advantages to be real, the control for the PFC stage needs to be improved. The document discusses use of non linear control and anti-windup controller for improved PFC performance, which are enabled by the use of digital control of the PFC stage.

Real-time control of motors using complex control algorithm such as sensorless field oriented control (FOC) is increasingly becoming popular because of the efficient control possible using these techniques. However, keeping system costs low and using a single controller to integrate the PFC and FOC algorithm on a single controller is challenging. The typical PFC power stage would switch at 100-200 KHz switching frequency, whereas, the motor control stage at 10-20 KHz. This implies that cycle-by-cycle control needs to be enabled. The control loop must run at 100 KHz for the PFC, or at least 10 KHz.

An implementation of PFC and motor control on a low voltage platform using a single low cost MCU is discussed in [1], which uses a time slicing approach to split up the motor control algorithm to gain bandwidth for PFC. This implementation works well for applications dedicated to PFC and motor, where no or little communication requirements exist and not much diagnostics are required. Additionally, once the time slicing is fixed and the execution rates are tightly coupled, the use of advanced techniques (such as frequency dithering to reduce EMI) would not be possible. Use of a higher clock rate controller is prohibitive from the cost and power consumption point of view.

Furthermore, with advancement in the semiconductor technology, higher and higher switching frequency for power stages are possible [2], and need for higher control loop execution rate is rising. This exacerbates the processor bandwidth requirements for real-time control, posing the challenge of doing more at a low cost in a cost sensitive market.

In many of these integrated systems, the cost of two microcontrollers is prohibitive and also brings in additional components such as coordinating the applications between the controllers. An MCU from Texas Instruments F28035 that has a small footprint floating-point unit called the CLA was chosen for this implementation. Using the CLA, the control execution of the two stages was decoupled, thus, enabling flexibility in operations and freeing up bandwidth on the main controller to perform diagnostics and communications. The following sections highlight the design of a hardware platform for this application, system and software integration issues and use of non linear control techniques in the PFC algorithm for improved results under dynamic load to work for motor control applications.

2 Hardware Platform

A hardware platform was designed to act as a development platform for digital motor control and power factor correction applications. The platform (Figure 2) was designed such that individual control of PFC and motor control could be tested. The DC bus and the controller power domains were separated to safely debug the system. In addition to this, an auxiliary power supply was designed into the platform to derive power for the controller from the wall mains supply, for standalone operation. Several safety mechanisms were incorporated into the board design including over current protection on each leg of PFC, inverter faults trip, over current on inverter trip making use of the internal comparators and digital-to-analog comparators of the controller, which kept the total bill of materials (BOM) costs down. The inverter stage was designed with voltage and current sensing to enable brushless direct current (BLDC), ACI and permanent magnet synchronous motors (PMSM) motor control in both sensorless and sensed configuration. PWM's were used to implement DAC's to enable system debug. Isolated CAN was added to the board to enable communications along with on board isolated emulator to safely connect the high voltage board to computer for debug and development of code.

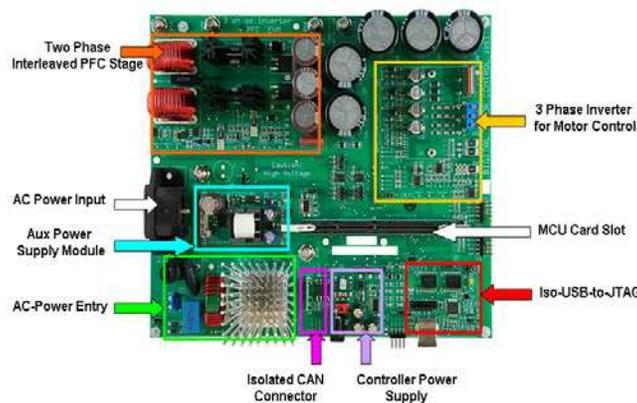


Figure 2. Motor Control and Power Factor Correction Hardware Platform

Figure 3 illustrates the power stages, the sense signals, and the interaction with the controller.

2.1 PFC Implementation

An interleaved PFC topology was implemented because of the advantages offered in reduction of the induction ripple and, thus, magnetic size. Optionally phase shedding is possible that can enable efficient operation of the PFC even at low load. The PFC stage is essentially a boost converter whose duty cycle is controlled such that the rectified input current, which is nothing but a numerical addition of the two phase currents, follows the rectified input voltage while providing load and line regulation at the same time.

2.2 Motor Inverter

The inverter stage was designed to implement sensed and sensorless control for induction, permanent magnet, and brushless DC motors. Options were provided such that the DC bus for the inverter stage could be sourced from either the AC power input, the PFC stage output or a DC power supply. The current feedback and voltage feedback along with interface circuit for encoders and position capture sensors were designed on the board to enable control of different style of motors.

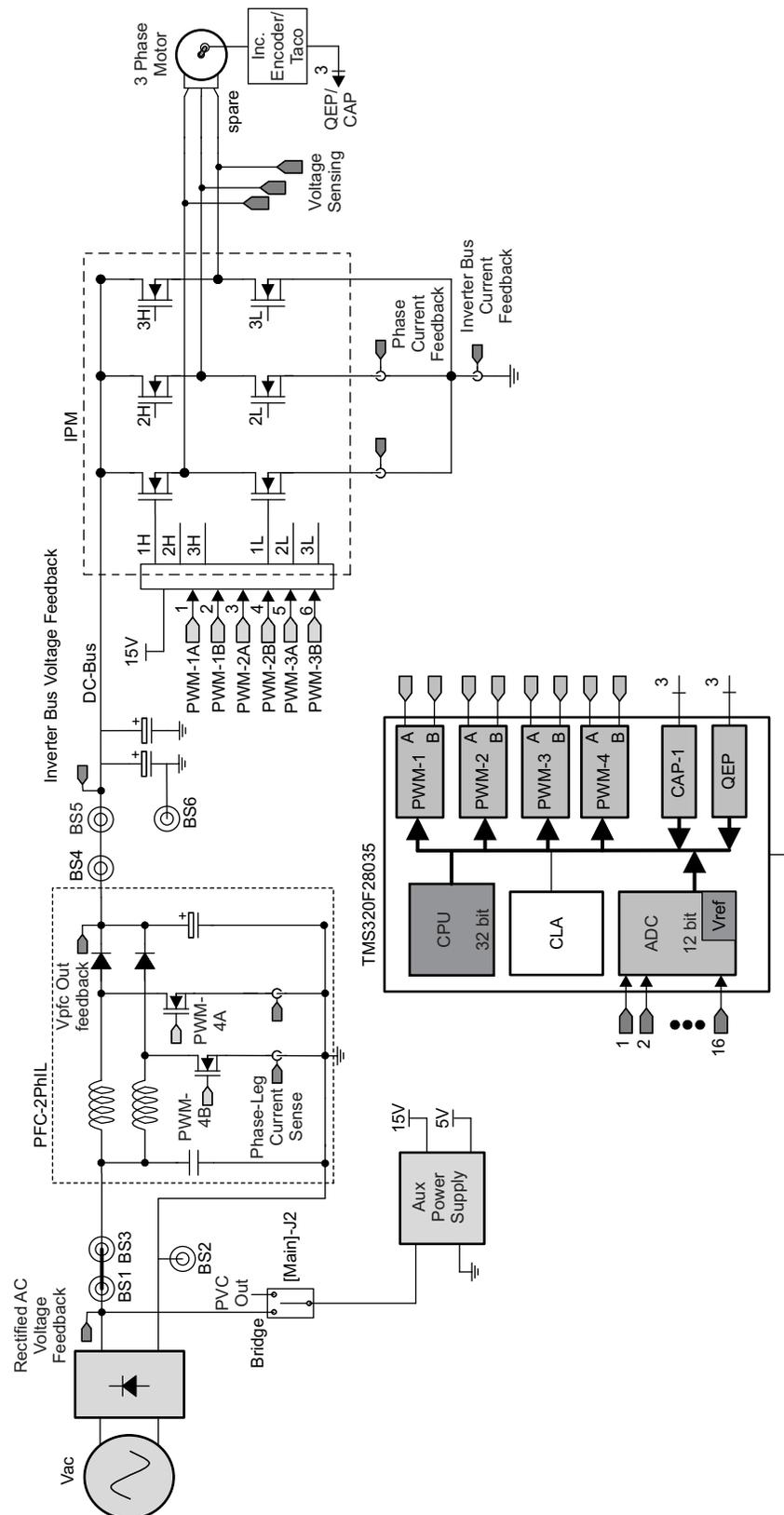


Figure 3. Motor Control and Power Factor Correction Hardware Platform

3 System Design and Integration

As discussed earlier, the integration of the PFC and motor control possesses bandwidth challenge on the controller. A solution using the Texas Instruments F28035 controller is presented that has a CLA is presented in this document.

3.1 Control Law Accelerator

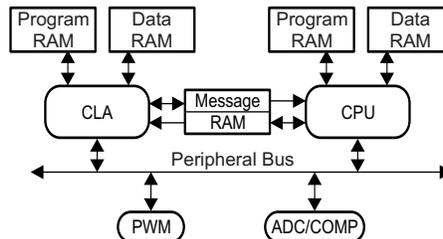


Figure 4. Control Law Accelerator

Most control algorithms can be split into three tasks:

- Excite the system
- Sample the system
- Control the system

Exciting the system for power and motor control type application implies changing duty cycle. Sampling the system would involve reading the ADC results value, or reading other sensor values such as QEP. The CLA is an independent floating-point unit that is present in addition to the main core on TMSF28035. The CLA is designed to offload the fast control algorithms task, thus, freeing up bandwidth on the main CPU (C28x) core to perform high level and communication tasks. The CLA has its own program and data bus, Figure 4, and executes independently of the main core on the MCU, enabling asynchronous control loop execution. The CLA interacts with the main core with use of message RAMs and has access to the control peripheral simultaneous to the main CPU [3].

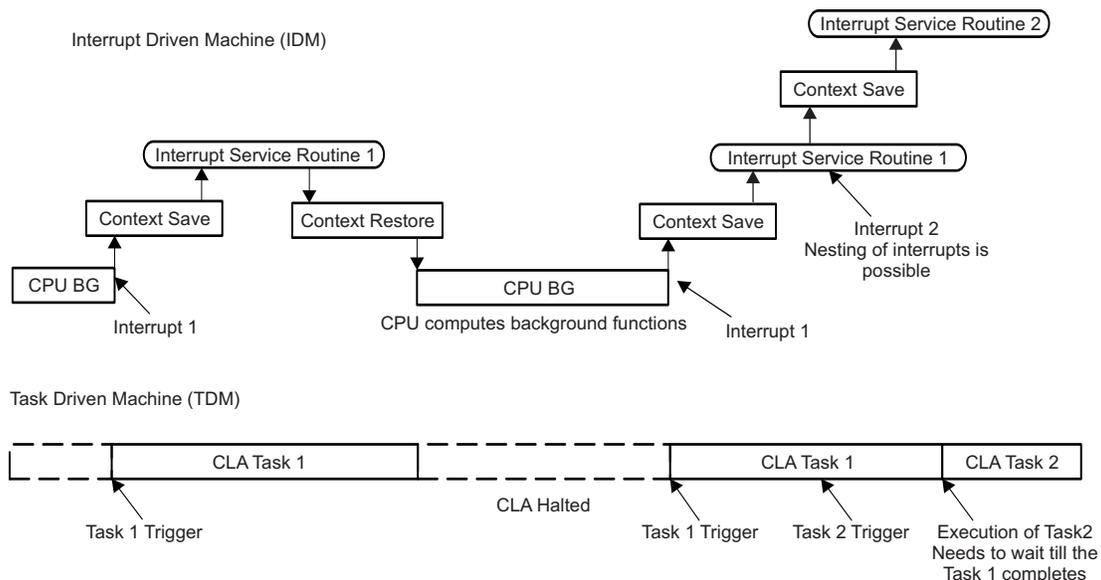


Figure 5. Interrupt vs Task Driven Machine

The CLA also offers additional benefits such as reduced sample to output delay, reduced jitter in execution, improved support for multi frequency loops. This is made possible because the CLA is task oriented instead of an interrupt service driven machine. In a pipelined CPU, the ISRs can be delayed by an “n” number of cycles if the CPU is executing branch type statements when the ISR is received. However, in a task-based machine this is not a problem as the auxiliary core waits for the periodic task to trigger before it begins execution. Therefore, the combination of CLA and CPU enables reduced jitter execution of the tasks, while maintaining the performance benefits of a pipelined machine for the main processor. Figure 5 illustrates the differences between a task driven machine (TDM) and an interrupt driven machine (IDM).

3.2 PFC Offloaded to the CLA

For the PFC and motor control implementation, the complete interleaved PFC algorithm was offloaded to the CLA and the sensorless field oriented control of the AC induction motor was implemented on the main core.

Figure 6 illustrates the execution of the algorithm of the PFC and motor control in CLA and the main core. The CLA executes the PFC algorithm independent of the main core. Therefore, periodic interrupts from the PFC algorithm to the main core are saved, thus, freeing up the main core, and leaving bandwidth for communication, diagnostics, and so forth.

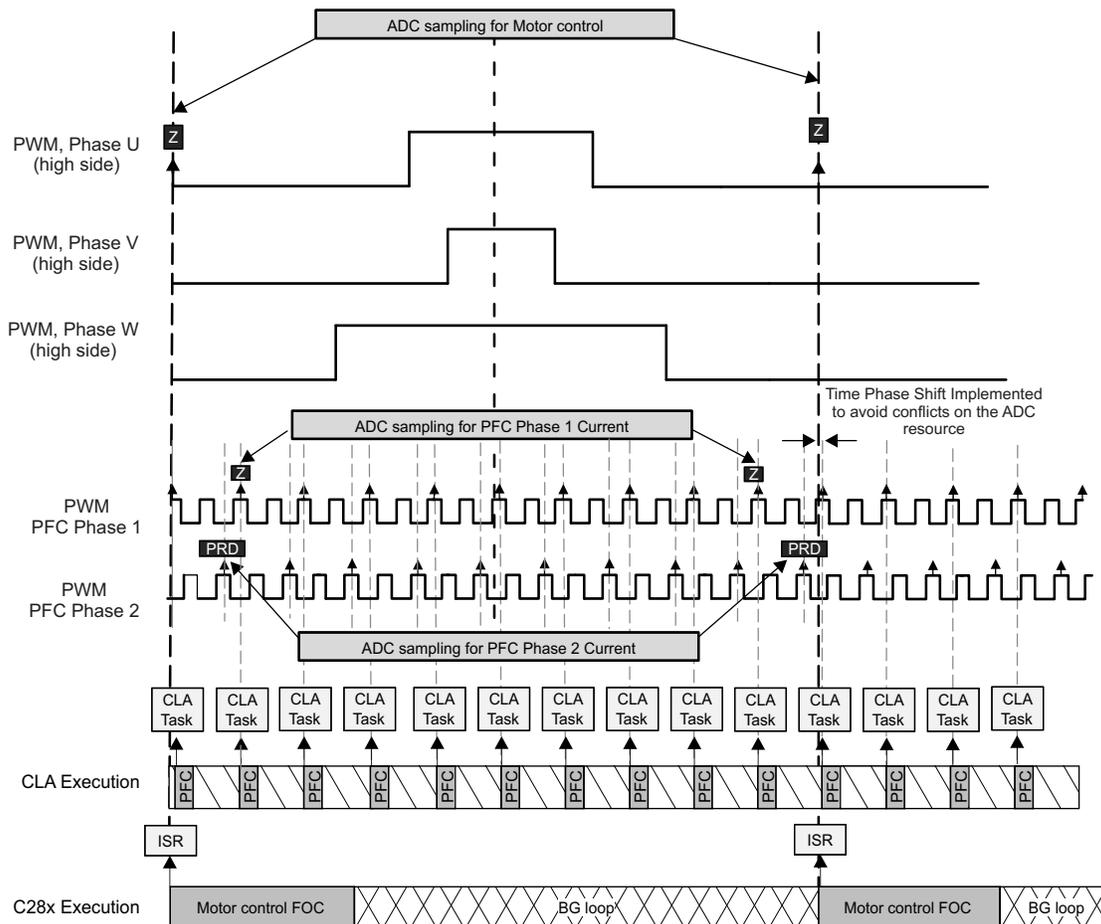


Figure 6. PFC Implemented on the CLA and Motor Control on C28x

3.3 Shared Resources Challenges

Even though the control loops can be executed independently, the peripherals are shared between the CLA and the main core and any conflicts for shared resources must be avoided. Digital control applications are sensitive to accurate timing for sensing the signals. In this application, the PFC periodically requests samples for the phase current and voltage, and the motor control would periodically request samples for the leg current and the DC bus voltage, and so forth. As the loops for the PFC and the motor control operate at varying frequencies, requests may be placed at the same time if care is not taken. Therefore, it is essential to implement a method that would avoid any resource conflict.

The phase shift mechanism of the PWM peripheral is employed. Figure 7 illustrates the timing diagram of the PWM for the motor control and the PFC stage and the synchronization mechanism used to avoid ADC conflicts. Figure 7 illustrates the PWM waveform generation on a 60 MHz device for 10 KHz motor control algorithm and a 100 KHz control loop rate of the PFC. Note that the switching rate is 200 KHz, this is dependent on the inductor present on the PFC power stage. The PWM peripheral offers the flexibility to trigger start of conversions (SOC's) for the ADC every switching cycle or alternate, avoiding any unnecessary load on the ADC. The motor control algorithm issues a synchronous pulse every zero event and provides a phase shift of 30 cycles to the PFC time base to avoid any shared resource conflict.

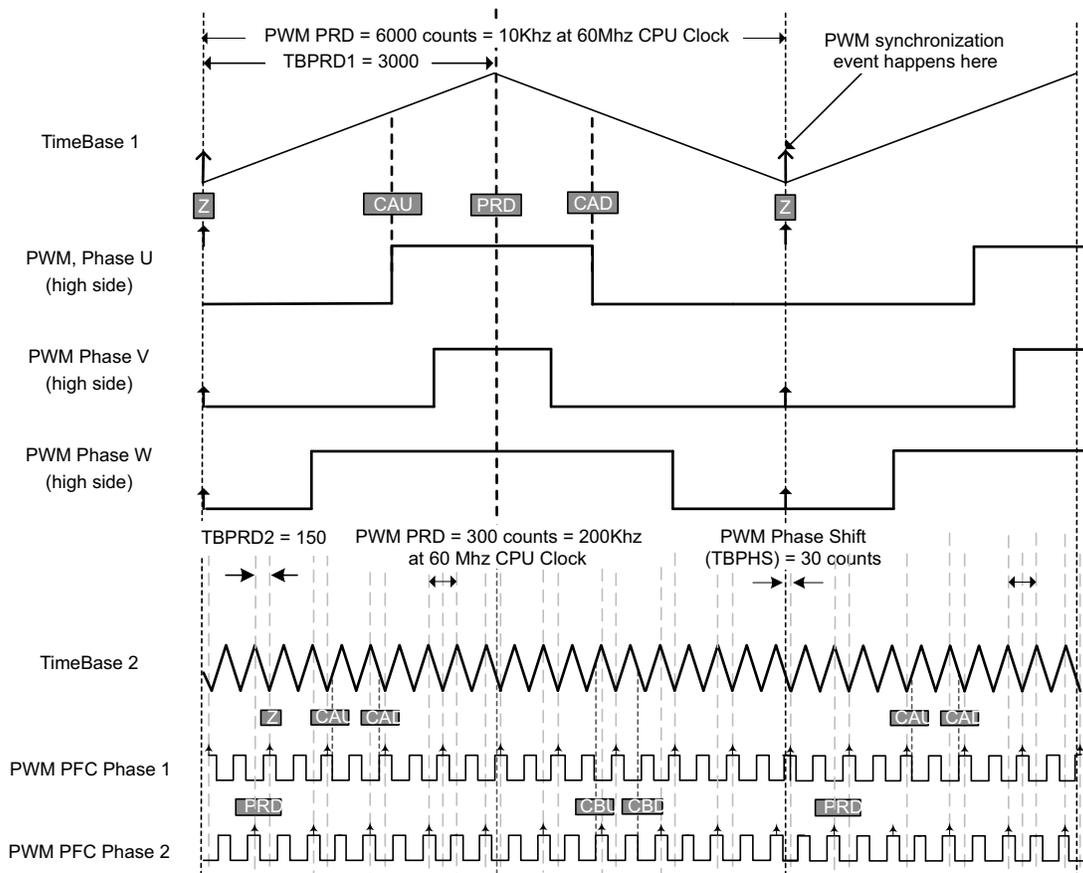
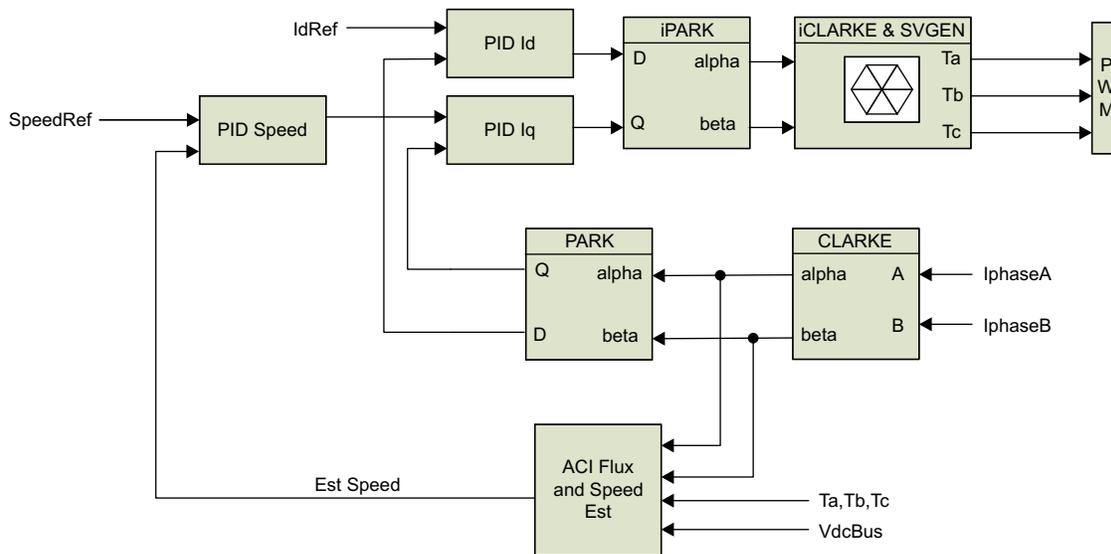


Figure 7. Timing Diagram for PFC and Motor Control Application Integration

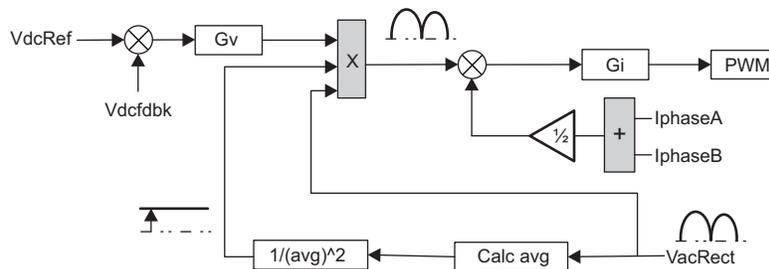
3.4 Field Oriented Control of ACI Motor

Sensorless field oriented control of AC Induction motor was implemented on the controller using shunt current sense from the two legs of the inverter. Figure 8 illustrates the FOC algorithm implemented.


Figure 8. FOC of AC Induction Motor

3.5 PFC Algorithm Improvements

A PFC implementation described in [4] was chosen. The PFC algorithm comprises of an inner current loop that wave shapes the current drawn from the mains for unity power factor. Whereas, the outer voltage loop keeps the DC bus constant. Figure 9 illustrates the control algorithm used for the interleaved PFC stage.


Figure 9. Digital Control Algorithm of Interleaved PFC Stage

The following section discusses improvement to the PFC algorithm for better transient response and AC drop recovery.

- Non-Linear Control of Voltage Loop:

In motor drive systems, the load on the motor can change dynamically, for example, putting of payload on a conveyor belt. This leads to increased constraints on PFC performance. As discussed earlier, the digital control of the PFC stage is composed of an inner current loop that tries to follow the rectified wave at the line frequency and an outer voltage loop that tries to maintain a constant DC bus voltage at the output. The boost PFC voltage loop is designed to be very low bandwidth (10~15Hz) in order to achieve good power factor. However, this comes at the cost of compromising the dynamic response, as the voltage loops will be very slow and result in significant deviation under transient load. To improve this condition while maintaining good power factor, a non-linear voltage control loop was implemented [5]. The PI controller for the voltage loop can be written as shown in Equation 1.

$$G_v(z) = \frac{U_v}{E_v} = K_p + \frac{K_I}{1-z^{-1}} \tag{1}$$

Figure 10 illustrates the non-linear technique being used. Under steady state, a set of coefficients, K1, is used for the voltage loop having a very low bandwidth, thus good power factor. Under transients load, low bandwidth of the voltage loop can cause the output voltage to not be well regulated and overshoot. When using non-linear control, the transient condition is detected by comparing the voltage error. The coefficients for the voltage loop are switched to K2, which has a much higher bandwidth, and the voltage output is not allowed to overshoot. Once the transient condition is passed, the error reduces and the coefficients are switched back to K1.

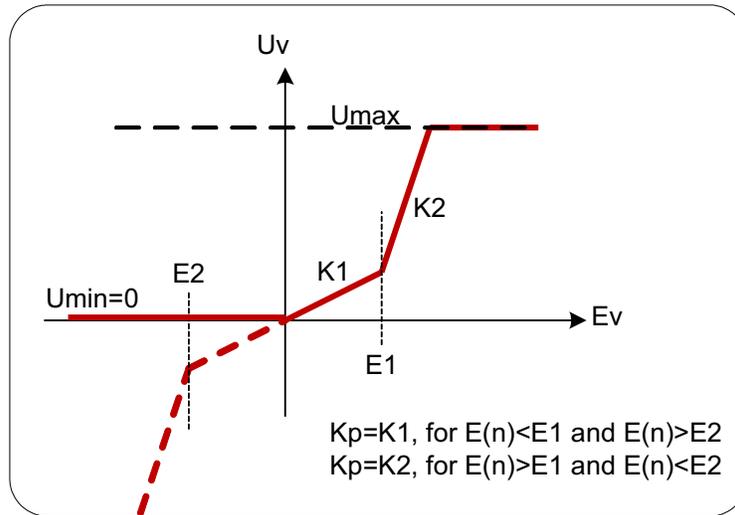


Figure 10. Non-Linear Control of PFC

Figure 13 and Figure 12 compare the results in case of load transients between linear and non-linear control of the voltage loop. Note the voltage overshoot, in case of load transients, was significantly reduced with the help of non-linear control technique. Reduction in voltage overshoot plays an important part in increasing the capacitor life time, thus increasing system life span and reliability.

- Anti Integral Windup Control

Under conditions of AC transient, the control of PFC can cause the DC bus to overshoot. One of the advantages offered using the PFC is to reduce the capacitor size needed for the motor inverter. Therefore, under transients and AC line drop, the voltage undershoot and overshoot can worsen with lower DC bus cap for the inverter stage. An anti integral windup controller was used and the overshoot and recovery in case of AC transients was significantly reduced. Figure 15 and Figure 16 illustrate the AC drop recovery response with and without anti-integral windup control. Note that the voltage overshoot and recovery time is significantly improved using the anti integral windup control for the voltage loop of the PFC.

4 Results

4.1 PFC Performance Between Linear and Non Linear Control

Figure 11 and Figure 12 compare the PFC performance at low line and 324W. In the figure, Ch3 is the input current AC current and Ch1 is the input AC voltage. The $V_{in} = 110$ Vrms, $I_{in} = 3.15$ A (rms), and the PFC is boosted to $V_{bus} = 400$ V at output load $P_{out} = 324$ W. Figure 11 uses the linear voltage loop controller, given by:

$$U(n) = U(-1) + 10.56 * E(n) - 10.5 * E(-1)$$

Figure 12 uses non-linear voltage loop controller given by:

Under Steady State:

$$U(n) = U(-1) + 0.7575 * E(n) - 0.75 * E(-1)$$

Under Transients:

$$U(n) = U(-1) + 42.24 * E(n) - 42.0 * E(-1)$$

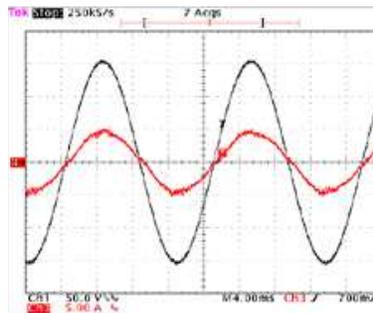


Figure 11. Linear Volt Loop Control

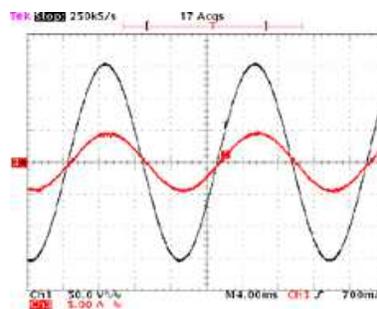


Figure 12. Non-Linear Volt Loop

4.2 DC Bus Transient Response, Low Line, Load Step

Figure 13 and Figure 14 compare the DC bus response in case of load transient between linear and non-linear control. Ch1 represents the DC bus volt transient response (AC couple, 25V/div), Ch3 represents the input current (5A/div), $V_{in} = 120$ Vrms, $V_{bus} = 400$ V, and a load step = 251W was applied to the PFC stage.

Note that from Figure 13 and Figure 14 that the total DC bus variation was reduced from 33.5 V to 26 V, an improvement of 22.4% using the non-linear voltage loop. Also note the recovery from the load transient is quicker.

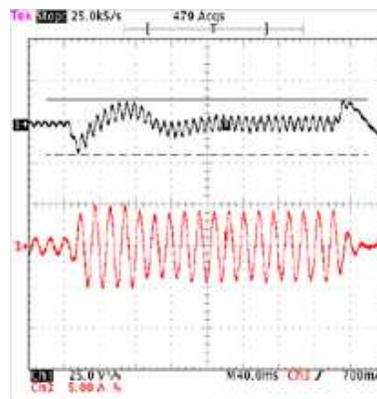


Figure 13. Linear Volt Loop Control

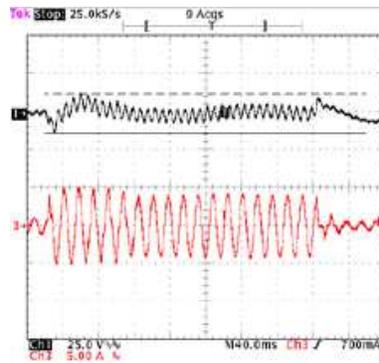


Figure 14. Non-Linear Volt Loop

4.3 AC Drop Recovery Response

Figure 15 and Figure 16 compare the response of the DC bus in case of AC drop with and without anti-integral windup control. Ch1 represents the input AC line, Ch2 the DC bus voltage and Ch3 the input current. An AC drop of 25 ms was used to compare the performance. It is observed from Figure 15 and Figure 16 that the voltage overshoot and recovery is significantly improved by using anti-integral windup control.

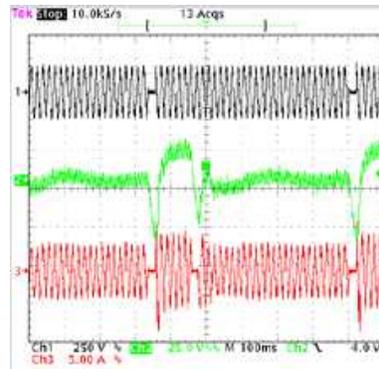


Figure 15. No Anti-Integral Windup

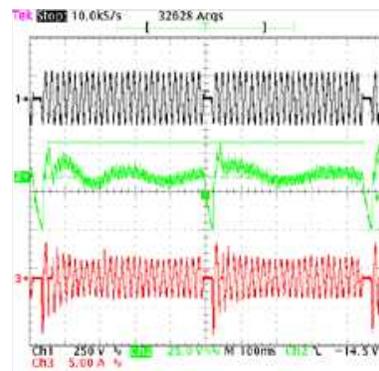


Figure 16. With Anti-Integral Windup

5 Conclusion

System integration advantages for PFC and motor control were discussed in this document and issues in integrating PFC and field oriented control on AC induction motor on a single controller were highlighted. A solution was presented using the CLA to offload the PFC algorithm, thus, freeing up bandwidth on the main controller to perform diagnostics and communications. Improvements to the PFC algorithm using non-linear control techniques and anti integral windup controller for the voltage loop were presented and results highlighted.

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