Application Report
SPRAC31–February 2019

TMS320C5505/15/35/45 schematic checklist

ABSTRACT

This application report provides recommendations and a checklist to follow while creating or reviewing schematics for the TMS320C5505/15/35/45 family of low-power fixed-point processors.

Contents

1 Introduction

1.1 Device Applicability

This application report applies to the following devices:

- C5504/C5505
- C5514/C5515
- C5532/C5533/C5534/C5535
- C5545

1.2 Links to TI Hardware Designs Based on C5505/15/35/45

1.2.1 C5505 eZdsp

- TI Tool Page: C5505 eZdsp™ USB Stick Development Tool
- Spectrum Digital Page: TMS320C5505 eZDSP USB STICK (Revision D)

1.2.2 C5515 eZdsp

- TI Tool Page: C5515 eZDSP USB Stick Development Tool
- Spectrum Digital Page: TMS320C5515 eZDSP USB STICK (Revision A)

1.2.3 C5515 EVM

- TI Tool Page: TMS320C5515 DSP Evaluation Module
- Spectrum Digital Page: EVM5515 Support Home (Revision B)

1.2.4 C5535 eZdsp

- TI Tool Page: C5535/C5545 eZdsp USB Stick Development Kit
- Spectrum Digital Page: eZdsp5535 (Revision C)

1.2.5 C5535 Audio Capacitive Touch BoosterPack

- TI Tool Page: C5000™ Audio Capacitive Touch BoosterPack

1.2.6 C5545 BoosterPack (BOOST5545ULP)

- TI Tool Page: http://www.ti.com/tool/boost5545ulp

1.3 EVM vs Data Sheet

- In case of any discrepancy between the TI EVMs and the device-specific data sheet, always follow the data sheet. Despite the designer's best efforts, the EVMs may contain errors which may still function but are not completely aligned with the data sheet specification. Therefore, the EVM designs should not be considered as reference designs to be blindly reused.

2 Complimentary Resources

- *Board and System Design Considerations for the TMS320VC5503/06/07/09A DSPs*
  - Board design recommendations for VC5503/5506/5507/5509A DSPs - still largely applicable to C5505/15/35/45 DSPs
- *OMAP5910 Decoupling/Filtering Techniques*
  - Great description of decoupling capacitor theory and methodology for calculating decoupling capacitor values

3 Recommendations Specific to C5504/05/14/15/32/33/34/35/45

3.1 Before You Begin

3.1.1 Documentation

Make sure you have the latest version of documentation, especially the data sheet and silicon errata.

TIP: On each ti.com device product folder there is a button "Alert me about changes to this product". Registration here enables proactive automatic notification of device errata.

3.1.2 Pin Out

Internal pull-up/pull-down resistors are implemented with weak transistors. As the voltage present on the I/O pin varies the relative gate voltage to this weak transistor changes which will cause the effective pullup/ pull-down resistance to change. Therefore, internal resistors do not have a linear response like external resistors. The non-linearity along with process voltage and temperature variations require internal pullup/ pull-down resistors to be specified with a wide range of resistance or current sourcing/sinking. The input current without a pull-up or pull-down turned on defines the input leakage without any current from internal pull resistors. The input current with a pull-up or pull-down turned on defines a combination of input leakage current and current required to force the internal pull resistors to the opposite voltage rail. For example, if an internal pull-up is turned on the value shown represents the total current required to pull the input to VSS.

When deciding what value of external resistor to use, you must consider the worst case combination of all internal leakage paths of all devices connected to a signal and make sure the external resistor is able to force these internal leakage paths to a potential greater than Vih min, or less than Vil max.

3.2 Unused Pins

- ❑ Do not leave inputs floating! - floating input pins consume I/O power (1 mA per floating pin is not uncommon)
  - ❑ For more information, see *C5000 DSP Based Low-Power System Design*.
- ❑ Software configurations to control unused signals
  - ❑ Pullup/Pulldown Inhibit Registers (PDINHIBR1/2/3) to enable internal pull-up/down resistors.
  - ❑ GPIOs conigured as outputs
  - ❑ Cannot apply software configurations until bootloader completes and application code runs. During boot, I/O current could be higher than after configuring for low power.
  - ❑ Some pins do not support software termination and must be terminated externally - these pins do not have "IPU" or "IPD" under the OTHER column in Terminal Functions table in the data sheet. For more information, see *C5000 DSP Based Low-Power System Design*.

3.3 Unused Power Rails

3.3.1 If USB is not Used

- ❑ Terminate USB pins to permanently disable USB
- ❑ USB_LDOO must be left floating (can be disabled in software - LDOCNTL register [7004h])
- ❑ USB_R1 signal must be connected via a 10 kΩ resistor to ground
- ❑ Short the following USB pins directly to ground:
  - ❑ USB_MXI
  - ❑ USB_VDDOSC
  - ❑ USB_VSSOSC
  - ❑ USB_VBUS
  - ❑ USB_DP
  - ❑ USB_DM
  - ❑ USB_VSSREF
  - ❑ USB_VDDA3P3
  - ❑ USB_VDDA1P3
  - ❑ USB_VDD1P3
  - ❑ USB_VDDPLL
  - ❑ USB_VSSPLL
  - ❑ USB_VSS1P3
  - ❑ USB_VSSA3P3

3.3.2 If RTC is not Used

- ❑ CVDDRTC AND LDOI MUST always be supplied even if RTC is not used
  - ❑ LDOI supplies power to the internal LDOs, the bandgap reference generator circuits, and serve as the I/O supply for some input pins
  - ❑ CVDDRTC MUST NOT be supplied by any on-chip LDO output
- ❑ If the RTC oscillator is not used, it can be disabled by connecting RTC_XI to CVDDRTC and RTC_XO to ground (or left floating). CVDDRTC must be supplied with a voltage within the recommended operating conditions.

NOTE: When RTC oscillator is disabled, the RTC registers (I/O address range 1900h – 197Fh) are not accessible.

3.3.3 If EMIF is not Used (not applicable to C5532/33/34/35 or C5545)

It is permissable to ground the DVDDEMIF supply pins if the following conditions are all met:

- ❏ At least one DVDDEMIF package ball is grounded. The others must be either floating or grounded.
- ❏ All signal pins that use DVDDEMIF as their I/O supply voltage (all of the pins listed in the *External Memory Interface Terminal Functions* table located in the *TMS320C5505 Fixed-Point Digital Signal Processor Data Manual* and the *TMS320C5515 Fixed-Point Digital Signal Processor Data Manual*), regardless of multiplexing options, are either:
  - ❏ All grounded
  - ❏ All floating (not driven by any external source)
  - ❏ Any combination of grounded or floating

3.3.4 If an On-Chip LDO Output is not Used

- ❏ If an LDO is not used, leave the LDOO output pin floating
- ❏ CVDDRTC MUST NEVER be supplied by any on-chip LDO outputs
- ❏ If DSP_LDOO is not used:
  - ❏ RESET must be asserted until power supplies and clocks are stable (internal Power on Reset logic disabled when LDO not used)
  - ❏ DSP_LDO_EN should be tied high to LDOI

3.4 Clocking

Make sure your input clock/crystal meets the data sheet requirements. For example:

- ❏ Frequency
- ❏ ESR for crystal
- ❏ Load capacitance meets both the crystal's and processor's requirements
- ❏ Crystal and caps placed physically close to processor
- ❏ Double check proper voltage level for clock (for more information, see the device-specific data sheet)
- ❏ Available clock sources to generate SYSCLK
  - ❏ CLK_SEL pin = low: RTC oscillator @ 32.768 KHz
  - ❏ CLK_SEL pin = high: CLKIN pin supplied by 11.2896, 12, or 12.288 MHz clock (for bootloader)
  - ❏ On-chip PLL and clock dividers available to modify SYSCLK frequency
- ❏ Do not need RTC oscillator if...
  - ❏ Do not need RTC clock
  - ❏ Not sourcing SYSCLK from RTC oscillator
  - ❏ Do not need RTC-only mode
  - ❏ See If RTC is not used
- ❏ Do not use CLKOUT as MCLK for any device such as a CODEC
  - ❏ CLKOUT for debugging purposes only
  - ❏ CLKOUT contains clock jitter, not glitch-free
- ❏ Avoid using SYSCLK as the clock source for peripheral clocks that require low-jitter and high precision
  - ❏ For example, I2S ports should be slaved and clocked by an audio quality clock generator for high audio quality
  - ❏ PLL jitter depends on the PLLIN and PLLOUT frequencies - 200ps cycle-cycle is a reasonable estimate at PLLOUT (before dividers)

3.5 OSC Internal Oscillator Clock Source

Figure 1 shows the recommended crystal circuit. It is recommended that pre-production printed circuit board (PCB) designs include the two optional resistors: Rbias and Rs. They may be required for proper oscillator operation when combined with production crystal circuit components

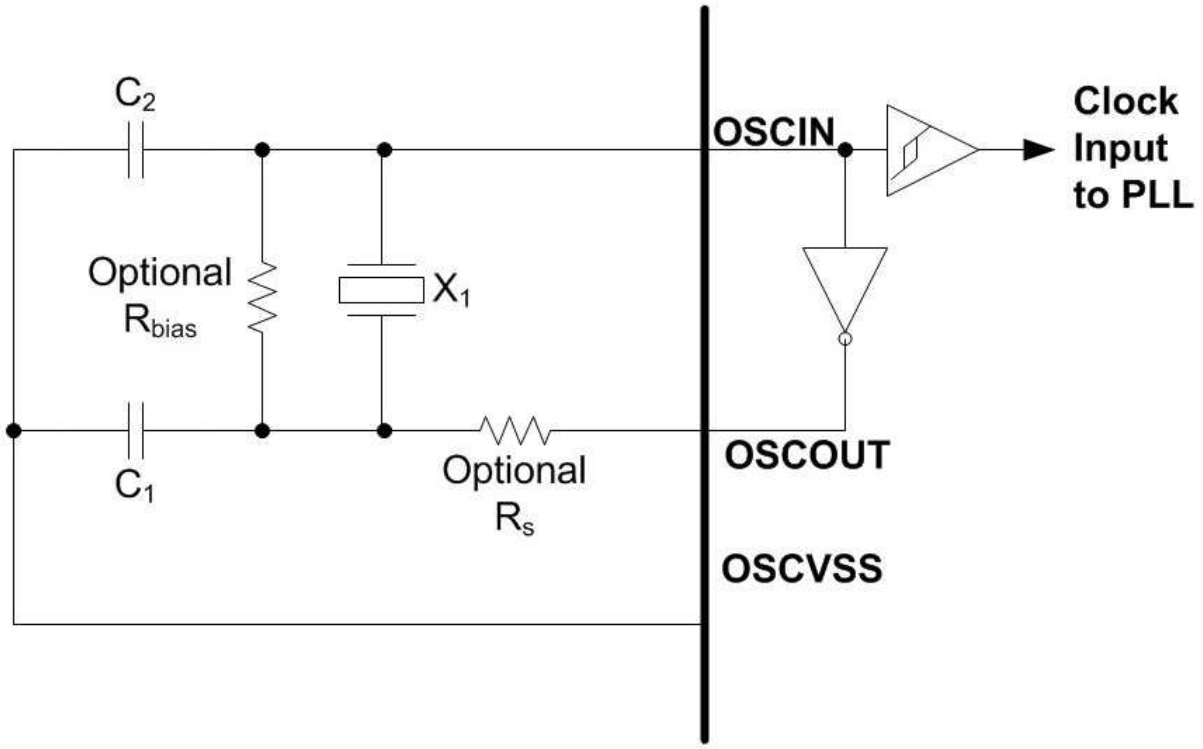

Figure 1. OSC Crystal Circuit Schematics

In general, adding Rbais and Rs resistors improves circuit performance by reducing the long start-up time, crystal overdrive and voltage and temperature related issues. Specifically, they provide the following functionality:

Rs helps reduce the drive level on the crystal and decreases the slew rate, which adds additional phase shift Recommended value: 50 Ω Rbais (the feedback resistor) is used to bias the input of the inverting amplifier and improve the loop gain Recommended value: 1M Ω. However, in most cases Rbias is not required and Rs is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on pre-production PCBs.

For the calculation of Rs and RBais values, see the Crystek Application notes. Oscillator components (Crystal, C1, C2, optional Rbias and Rd) must be located close to the device package. Parasitic capacitance to the printed circuit board (PCB) ground and other signals should be minimized to reduce noise coupled into the oscillator.

3.6 Power

For more information, see *C5000 DSP Based Low-Power System Design*

3.6.1 CVDDRTC Must be Always Supplied - [0.998 V - 1.43 V]

- ❏ CVDDRTC MUST NOT be supplied by any on-chip LDO outputs
- ❏ CVDDRTC voltage can be different to CVDD (core supply)
- ❏ CVDDRTC can be supplied through a resistor divider or through diode(s) with forward voltage drop to take 1.8 V or 3.3 V to a voltage within the range [0.998 - 1.43V] (inefficient but cheap)
  - ❏ Consider max and min currents into CVDDRTC supply as well as max and min CVDDRTC voltages when sizing resistors
  - ❏ Typical max CVDDRTC current = 0.02 mA @ 1.3 V
  - ❏ Resistor divider values calculated to supply CVDDRTC with approximately 1.3 V from 3.3 V for CVDDRTC current of 0 mA to 0.05 mA: Rtop = 10k, Rbot = 6.5k
  - ❏ If RTC is not used, RTC_XI must be tied to CVDDRTC

3.6.2 LDOI Must be Always Supplied

- ❏ Even during RTC-only mode (the lowest power idle mode)
- ❏ LDOI minimum supply voltage is 1.8 V Range: [1.8 - 3.6] V
  - ❏ There is no margin below 1.8V for LDOI, so consider the tolerance of the voltage supply
  - ❏ Bad supply: 1.8 V ±5% is in range [1.71 - 1.89] V - violates min voltage of 1.8 V
  - ❏ Good supply: 1.9 V ±5% is in range [1.80 - 2.00] V - satisfies min voltage of 1.8 V

3.6.3 On-Chip LDOs

- ❏ Pros: Included in DSP package (reduced board size and cost), On-chip POR voltage monitor and POWERGOOD holds RESET, ability to switch CVDD voltage by writing to LDOCNTL register
- ❏ Cons: Better conversion power efficiency available with off-chip regulators (switching), LDOO cannot supply CVDDRTC - still need external [0.998 - 1.43] supply (or voltage divider/diode)
- ❏ Before reset is released, LDOs ramp up to an untrimmed value. After reset is released, the bootloader trims the LDO outputs to their target voltage. Untrimmed voltages are screened to allow bootloader execution, but may be as low as 1 V. Take this into consideration if monitoring LDO output voltages before releasing reset. Consider asserting RESET for a fixed delay to allow for bandgap and LDOs to ramp to untrimmed values.
- ❏ If not using DSP_LDOO to supply CVDD...
  - ❏ Warning: If DSP_LDOO does not supply CVDD (DSP_LDO_EN = HIGH), then no Power-On-Reset logic to hold RESET low internally while CVDD ramps
  - ❏ RESET must be held low externally until all power supplies are up and stable
  - ❏ Consider POWERGOOD signal timing and tolerance during CVDD ramp - when RESET released, CVDD must be > 0.998 V with margin

3.6.4 Recommended PMIC

- ❏ TPS65000 (on the C5515 EVM) features 1.05 V/1.3 V selectable, 1.8 V/3.3 V selectable, plus additional 1.3 V, 1.8 V, 3.3 V supplies
- ❏ *Power Management Solutions for 16-Bit C5000™ Ultra-Low Power DSPs*

3.6.5 DVDDIO Supply ON While CVDD OFF

- ❑ Valid low power mode
- ❑ CVDD OFF so pins not driven by core
- ❑ Bus holders are automatically enabled to hold the state of many of the pins to prevent floating pin oscillation (saves power)
  - ❑ Internal Pull-ups/pull-downs become disabled
  - ❑ External pull-ups/pull-downs must be sized strongly to avoid contention between bus holder and external resistor (consumes power)
  - ❑ If resistor current exceeds bus-holder max current, then bus holder will flip state to match the pull-up/pull-down to avoid contention (saves power)

3.6.6 Power Sequencing

- ❑ This device has no specific power sequence unless used as a USB device
- ❑ USB supplies require power sequencing for reliable USB enumeration. If the USB subsystem is used, USB_VDDA1P3 and USB_VDD1P3 must be powered up first, and then the USB_VDDA3P3 and then the USB_VBUS. USB subsystem power up sequence:
  1. USB_VDDA1P3 and USB_VDD1P3
  2. USB_VDDA3P3
  3. USB_VBUS
- ❑ VBUS must not be supplied by host while C55xx is powered-off. The VBUS IO is not fail-safe. Following the above power sequencing ensures that VBUS will not reach the C55xx device when power is not applied.
- ❑ Load switch parts that can be used for usb power sequencing: TPS22915, TPS22913

3.6.7 Voltage Rails of IO Pins

- ❑ Check the device-specific data sheet for appropriate voltage input levels to latch a high or low signal level. The terminal functions tables in the data sheet specify the operating I/O supply voltage for each signal. Example DSP_LDO_EN input signal uses the LDOI supply voltage. A value of LDOI (or greater than the VIH of LDOI, 0.7 * LDOI voltage) is required to latch a high state.

3.7 Decoupling Capacitors

Voltages from traces on a printed circuit board can couple to each other in places where it is not desired, (like power supply planes). To decouple the traces, capacitors were added to absorb some of the voltage and help reduce this effect. For more information on how to correctly place decoupling caps, see the *Power-Supply Decoupling* section in the device-specific data sheet. PLL and some analog supplies benefit from filters or ferrite beads to keep the noise from causing clock jitter. The minimum recommendation is a ferrite bead with a resonance at 100 MHz along with at least one capacitor on the device side of the bead. Additional recommendation is to add one capacitor just before the bead to form a Pi filter. The filter needs to be as close as possible to the device pin, with the device side capacitor being the most important thing to be close to the device pin. PLL pins close together can be combined on the same supply. PLL pins farther away from each other may need their own filtered supply.

- ❑ Have you verified that your pin labels correspond to the correct pin numbers?
- ❑ Have you verified that the power pins are connected to the correct supply rails?
- ❑ Pullups/Pulldowns:
  - ❑ Decoupling capacitors should be no more than 1.25 cm maximum distance from the device power pins to be effective
  - ❑ Recommended decoupling capacitance for the DSP core supplies should be 1 μF in parallel with 0.01-μF capacitor per supply pin
  - ❑ Consider the capacitance of PCB planes
  - ❑ Larger caps for each supply can be placed further away for bulk decoupling
  - ❑ Use high–quality low–ESL/ESR capacitors. For more information, see the *Capacitor Theory* section in *OMAP5910 Decoupling/Filtering Techniques*.

3.8 LDO Output Decoupling Capacitors

The LDO circuits implement a voltage feedback control system which has been designed to optimize gain and stability tradeoffs. As such, there are design assumptions for the amount of capacitance on the LDO outputs. For proper device operation, the following external decoupling capacitors should be used when the on-chip LDOs are enabled:

- ❏ DSP_LDOO - 5 µF to 10 µF
- ❏ USB_LDOO - 1 µF to 2 µF
- ❏ ANA_LDOO - 1 µF

3.9 Digital GND, Analog GND, Local GND

- ❏ Digital GNDs: VSS, USB_VSS1P3, USB_VSSOSC
- ❏ Analog GNDs: VSSA_PLL, USB_VSSPLL, USB_VSSA1P3, USB_VSSA3P3
- ❏ Local GNDs:
  - ❏ Must not connect local GND to the board ground unless otherwise stated (USB not used, see If USB is not used)
  - ❏ VSSRTC - Local ground for RTC oscillator (must not be connected to the board ground)
  - ❏ USB_VSSREF - Local ground for USB_R1 through resistor (must not be connected to the board ground). For more information, see Section 3.11.

3.9.1 Recommended USB Supplies

Table 1. Recommended USB Supplies

Pin Name	Digital or Analog	Board Recommendation
USB_VDDOSC	Digital	Ferrite Bead, Caps to Digital GND
USB_VSSOSC	Digital	If XTAL: Local GND, If clock: Digital GND
USB_VDDA3P3	Analog	Ferrite Bead, Caps to Analog GND
USB_VSSA3P3	Analog	Analog GND
USB_VDDA1P3	Analog	Ferrite Bead, Caps to Analog GND
USB_VSSA1P3	Analog	Analog GND
USB_VDD1P3	Digital	Ferrite Bead, Caps to Digital GND
USB_VSS1P3	Digital	Digital GND
USB_VDDPLL	Analog	Ferrite Bead, Caps to Analog GND
USB_VSSPLL	Analog	Analog GND

3.10 Reset

- ❏ If CVDD supplied by DSP_LDOO (DSP_LDO_EN = low), then internal Power-on-Reset (POR) releases reset when when the DSP_LDOO voltage is above a minimum threshold voltage provided by the bandgap
- ❏ If not using DSP_LDO (DSP_LDO_EN = high), implement an external power monitor to release reset when CVDD > 0.998 V (consider tolerances to guarantee CVDD > 0.998 V)
- ❏ Cannot combine external CVDD supply with on-chip powergood voltage monitor - reset must be asserted externally
- ❏ Always place external pull-up resistor on RESET - 100K
- ❏ Nice to have push-button to reset device for debugging
- ❏ A useful tip is to place a 0.1 µF cap near the reset pin to help avoid ESD-induced resets.

3.11 USB

- ❑ Plan to route USB differential pair signals first, on top layer if possible
- ❑ Avoid stubs, differential pair length mismatch or impedance mismatch
- ❑ Avoid any discrete components in DP/DM trace (except USB.org approved ESD components)
- ❑ See *High-Speed Interface Layout Guidelines*
- ❑ This USB peripheral is USB 2.0 high speed - do not implement USB 1.0 circuit on DP/DM pins
  - ❑ USB 1.0 circuit has series resistors and capacitors to GND on the DP and DM lines
  - ❑ USB 2.0 circuit has no components (except USB.org high-speed approved ESD components)
  - ❑ Implementing a USB 1.0 circuit on USB 2.0 will impact high-speed performance
- ❑ For USB power sequence requirements, see Section 3.6.6
- ❑ Caution: If USBVDD_OSC is ON while CVDD is OFF, the USB oscillator is enabled and consumes power
  - ❑ Having I/O power supplied while CORE power is off is an allowable power configuration, see Section 3.6.5
  - ❑ Register settings are lost when CVDD is OFF - USBOSCDIS in the USBSCR register loses its state
  - ❑ Prevent power consumption by turning USBVDD_OSC OFF before CVDD is OFF
- ❑ USB_R1 - the USB_R1 resistor (reference current output) may need to be tweaked to pass USB compliance - perform the USB eye mask test on the board and adjust the resistor value until the eye is passing with margin. 8k - 10k is the range for most boards.

3.12 I2C

- ❑ I2C pull-up resistors on SDA and SCL need to be sized to meet the rise time specified in the I2C spec:
  - ❑ t_rise < 1000 ns for Standard Mode (SCL up to 100 kHz)
  - ❑ t_rise < 300 ns for Fast Mode (SCL up to 400 kHz)
- ❑ Pull-up resistors typically in the range [3k - 10k] Ω
- ❑ When more devices are on the I2C bus, stronger resistors are required to meet the rise times
- ❑ Make sure all devices on a given I2C bus have unique addresses (often this is configurable through a pin to enable multiple of the same device)

3.13 I2S

- ❑ It is recommended to use I2S as a slave to an external master that drives the bit clock and frame sync. The frame sync timings are marginal when I2S generates the BCLK and FS signals
- ❑ When I2S is configured as a slave, frame synch needs to be delayed to meet data sheet timing requirements. Implement an RC delay on the I2S_FS trace and size R and C to satisfy the timing requirements. For more information, see the device-specific data sheet.
- ❑ To ensure synchronization among multiple I2S busses, it is recommended to use one external master to drive clocks to multiple slaves (including the C55xx).

3.14 RTC

- ❑ This simple peripheral is frequently hooked up incorrectly. Make sure it's connected as follows:
  - ❑ TX ---> RX
  - ❑ RX <--- TX
- ❑ CVDDRTC must be supplied externally (MUST NOT be supplied by any on-chip LDO)
- ❑ DVDDRTC may be grounded if RTC is not used, see Section 3.3.2
- ❑ For robust software that uses WAKEUP pin to exit RTC-only mode, see the *C5000 DSP-Based Low-Power System Design*.

3.15 SAR ADC

- ❑ SAR ADC has better absolute accuracy when accurate external voltage reference (1.3 V) used instead of internal refs from Bandgap (0.8 V or 1.0 V)
  - ❑ Set REFAVDDSEL bit in SARPINCTRL register to 1: Reference Voltage set to Analog Voltage (VDDA_ANA supply)
  - ❑ Design GPAIN inputs so they are in the range of VDDA_ANA voltage (0 V - 1.3 V)
- ❑ GPAIN pin input impedance = 1MΩ
- ❑ Voltage measurements are less accurate if impedance on pin approaches the input impedance of the device

3.16 Pin Muxing

- ❑ Make pin mux decisions before starting schematics (at block diagram level)
- ❑ External Bus Selection Register (EBSR) controls 2 serial port pin muxes and 1 parallel port pin mux with software
- ❑ Software can change pin mux mode during execution, but affected peripherals must stop clocks before and reset after the change PPMODE selection (no mixing PPMODEs)
- ❑ It is recommended to set the EBSR register only once after bootloader completion. The EBSR logic is asynchronous and can cause unexpected behavior on pins being muxed (glitches, driven states, and so forth).

3.17 Signal Visibility

For debugging purposes, you may need to look at a signal on an oscilloscope. Therefore, you will want to make sure you can get access to the signals, particularly with BGA devices where it might otherwise be impossible. This can be done by bringing a via all the way through the board or other times where a pullup/pulldown is needed you can probe at the resistor. Having a GPIO brought to a test point or an LED can be useful as well.

Additionally, CLKOUT and XF pins are useful signals for debugging the PLL and bootloader.

3.18 EMIF (not applicable to C5532/33/34/35 or C5545)

- ❑ EMIF interfaces to both mSDRAM and SDRAM devices that meet the following requirements:
  - ❑ Non-mobile SDRAM can be supported under certain circumstances. The C5504/05/14/15 always use mobile SDRAM initialization but are able to support SDRAM memories that ignore the BA0 and BA1 pins for the load mode register command. During the mobile SDRAM initialization, the device issues the load mode register initialization command to two different addresses that differ in only the BA0 and BA1 address bits. These registers are the Extended Mode register and the Mode register. The extended mode register exists only in mSDRAM and not in non-mSDRAM. If a non-mobile SDRAM memory ignores bits BA0 and BA1, the second loaded register value overwrites the first, leaving the desired value in the mode register and the non-mobile SDRAM will work with the device.
  - ❑ Since the extended load mode register command always occurs before the standard load mode register command, as long as the non-mobile SDRAM ignores BA0 and BA1 during either command, the mode register will first be written to with incorrect (mobile SDRAM) data, then be overwritten with the correct (SDRAM) data.
  - ❑ MT48LC16M4A2 is an example of SDRAM that ignores BA0 and BA1 during the load mode register command
  - ❑ MT48H8M16LF is an example of mobile SDRAM that shows the extended load mode register command before the load mode register command, using BA0 and BA1 to differentiate between the two commands.
- ❑ If EMIF is not used, see Section 3.3.3.

3.19 JTAG

- ❏ For more information, see *XDS560 Emulator Technical Reference*
- ❏ JTAG configuration for low power
  - ❏ An emulator connected to the JTAG pins consumes additional power and should be disconnected for power measurements or mass production (stand-alone mode).
  - ❏ When debugging (load code from CCS):
    - ❏ Run-Free and then Disconnect from Target to avoid power consumption
- ❏ When in stand-alone mode (bootload production code):
  - ❏ If JTAG not used, ensure device does not enter test mode by adding strong (4.7k) pull ups to EMU0 & EMU1, and pull-down TRST (10K)
  - ❏ Pull-up on TDO saves power on DVDDIO rail (as much as approximately 500 µA)
    - ❏ Although only used as an output, the TDO pin uses a bidirectional I/O buffer without an internal pull-up. Pull-up externally to avoid floating input oscillation and associated power consumption.

3.20 Bootloader

The bootloader greatly influences schematics:

- ❏ SPI boot: Boots from SPI_CS0 but does not boot from SPI_CS1, SPI_CS2, or SPI_CS3
  - ❏ Checks both EBSR PPMODE 1 and PPMODE 6
  - ❏ Always have external pull-ups on SPI_CS pins
- ❏ MMC/SD boot: Boots from MMC/SD0 but does not boot MMC/SD1
- ❏ Bootloader can get stuck attempting MMC/SD0 boot if MMC0_CMD/I2S0_FS/GP[1] is not at a high level (and not toggling) during boot
  - ❏ Only an issue if booting from UART or USB, which come after MMC/SD0 in the boot sequence
  - ❏ Cause: Bootloader expects a pull-up resistor on MMC/SD0_CMD signal - if low or toggling, then bootloader gets stuck trying to access an MMC/SD card even if no card is present
  - ❏ Result: Bootloader gets stuck trying to boot MMC/SD (not present) and does not check UART or USB for boot - boot failure
  - ❏ If MMC0_CMD/I2S0_FS/GP[1] signal is used for I2S or GPIO, ensure this signal is at a high level during the bootloader execution
- ❏ NOR Boot: NOR Flash must support the Flash reset command (0x00F0 on data) and return to the read array mode afterwards, NOR Flash should support the common flash memory interface (CFI) (not applicable to C5532/33/34/35 or C5545).
- ❏ *Using the TMS320C5515/14/05/04 bootloader*
- ❏ *Using the TMS320C5545/35/34/33/32 bootloader*

4 References

- C5504 Product Page
- C5505 Product Page
- C5514 Product Page
- C5515 Product Page
- C5532 Product Page
- C5533 Product Page
- C5534 Product Page
- C5535 Product Page
- C5545 Product Page
- C5505 eZdsp™ USB Stick Development Tool
- TMS320C5505 eZDSP USB STICK (Revision D)
- C5515 eZDSP USB Stick Development Tool
- TMS320C5515 eZDSP USB STICK (Revision A)
- TMS320C5515 DSP Evaluation Module
- EVM5515 Support Home (Revision B)
- C5535/C5545 eZdsp USB Stick Development Kit
- eZdsp5535 (Revision C)
- C5000™ Audio Capacitive Touch BoosterPack
- C5545 BoosterPack
- Crystek application notes
- Texas Instruments: *Board and system design considerations for the TMS320VC5503/06/07/09A DSPs*
- Texas Instruments: *OMAP5910 decoupling/filtering techniques*
- Texas Instruments: *C5000 DSP based low-power system design*
- Texas Instruments: *Power management solutions for 16-bit C5000™ ultra-low power DSPs*
- Texas Instruments: *High-speed interface layout guidelines*
- Texas Instruments: *XDS560 emulator technical reference*
- Texas Instruments: *TMS320C5505 fixed-point digital signal processor data manual*
- Texas Instruments: *TMS320C5515 fixed-point digital signal processor data manual*
- Texas Instruments: *Using the TMS320C5515/14/05/04 bootloader*
- Texas Instruments: *Using the TMS320C5545/35/34/33/32 bootloader*

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