Application Report
SPRACH9B–October 2018–Revised January 2020

Flash Variants Supported by the mmWave Sensor

ABSTRACT

This application note describes the flash variants supported by Texas Instrument's mmWave Sensor.

Contents

List of Tables

Trademarks

1 Serial Data FLASH Supported

1.1 AWR1243/xWR1443 ES1.0 and ES2.0 Devices

The AWR1243/xWR1443 ES1.0 and ES2.0 devices work only with Spansion and Macronix devices. In particular, the flash variants tested to work with the ROM bootloader are:

- Spansion S25FL132K0XNFB010
- Macronix MX25L3233F
- Macronix MX25R1635FZNIH0 (wide voltage part variant)

1.2 xWR1642, xWR1843, IWR6843 Devices and AWR1243/xWR1443 ES3.0 Devices

There are several factors that determine if the xWR1xxx ROM bootloader can interface and work with the SFLASH on xWR1xxx devices.

1.2.1 Pre-requisite

Refer to the device data sheet for details on the timing and interfacing requirements with the SFLASH over the QSPI interface.

SFLASH device variants should support 40-MHz operation for all commands (including normal read command).

SFLASH supports the SFDP command and responds with JEDEC-compliant information regarding the capabilities and command set of the flash. The key fields interpreted are listed in Table 1.

Table 1. Key Fields

Field	Byte Offset
SFDP signature	[3-0]
JEDEC flash parameter offset in bytes	[0xE-0xC]
(1-1-4) Read support	[JEDEC flash parameter offset in bytes + 0x2] – bit6
(1-1-2) Read support	[JEDEC flash parameter offset in bytes + 0x2] – bit0
(1-1-4) Read command code	[JEDEC flash parameter offset in bytes + 0xB]
(1-1-4) Read dummy cycles	[JEDEC flash parameter offset in bytes + 0xA] – bit[4:0]
(1-1-2) Read command code	[JEDEC flash parameter offset in bytes + 0xD]
(1-1-2) Read dummy cycles	[JEDEC flash parameter offset in bytes + 0xC] – bit[4:0]

- The number of address bytes = 3 (always).
- For single data line SPI read – Read Command Code (0xB), Read Dummy cycles (8bit).

1.2.2 ROM-Assisted Download to the FLASH (Device Management Mode - SOP5)

The ROM-assisted download should work with all flash variants that allow for “Memory mapped mode” and “Page program command (0x2)” with 1 dummy byte and 24-bit addressing.

In addition to writing to the flash, the ROM bootloader also supports setting the “Quad Enable” bit for Spansion and Macronix variants (certain specific part variants only).

1.2.3 ROM-Based Load From FLASH (Functional Mode – SOP4)

The ROM bootloader performs the read from the FLASH based on the highest capability mode (quad, dual, or single) as published by the SFLASH in response to the SFDP command. The commands used are as published by the SFDP response. Thus, if the quad read is supported, the expectation is that the Quad Enable (QE) bit is already set in the FLASH. The ROM bootloader uses the quad mode to perform the read.

1.2.4 Recommendation

The flash vendors have an orderable part variant with the Quad Enable (QE) bit set. TI recommends using these variants to work with TI mmWave SOCs.

1.3 Known Issues (xWR1642 ES1.0 and IWR6843 ES1.0 Devices)

The ROM bootloader in XWR1642 pre-production devices is not compatible with SFLASH variants that support extended addressing mode. In particular, the “Number of Address length” field of the SFDP command response being non-zero is not supported. The total SFLASH addressable region in XWR1642 devices is 8 MBytes. Thus, “Number of Address length” = 0 (corresponding to 3 bytes address length) satisfies the addressable range. However, the compatibility issue is with variants that allow for 3 or 4 bytes address length.

This incompatibility will be addressed in the production version of the XWR1642 silicon.

1.4 Flash Variants

Supported flash parts for xWR1642 ES2.0, xWR1842 ES1.0, xWR1443 ES3.0, and IWR6843 ES1.0 & ES2.0 devices. The flash variants that have been tested to work on are shown in Table 2.

Table 2. Tested Flash Variants

Flash Vendor	Variant	Remarks
CYPRESS (SPANSION)	S25FL132K0XNFB01	QE bit set by ROM bootloader in SOP5 while flash programming
	S25FL064LVF01	QE bit set by ROM bootloader in SOP5 while flash programming. This flash variant supports extended addressing mode. All mmWave devices may not be compatible with the extended addressing mode. Refer to Section 1.3.
MACRONIX	MX25L3233F	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25R1635FZNIH0	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25V1635FZNQ	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25U1633FZNQ	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25V8035FM1Q	QE bit set by ROM bootloader in SOP5 while flash programming
	MX25U1633FZUI	Industrial grade 1.8-V flash
ISSI	IS25LP080D	QE bit set
WINBOND	W25Q16DVZPIG	By setting QE bit externally once

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (March 2019) to B Revision	Page
• Updated Flash Variants section.	3
• Added MX25U1633FZUI information to Tested Flash Variants table.	3

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