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ABSTRACT

The analog-to-digital converter (ADC) is a key module used to sense feedback and monitoring signals in a real-time control application. However, without careful design and evaluation of the circuits driving the ADC input, significant sample-and-hold circuit (S+H) settling errors can occur, resulting in poor performance of the ADC sensing and thus the system. This application report will identify the resources that can be used to understand ADC input settling and design appropriate ADC driving circuits as well as how to evaluate these resources in the specific context of TMS320F2837xD, TMS320F2837xS, TMS320F2838x, TMS320F2807x, TMS320F28004x, and TMS320F28002x family microcontrollers.

Project collateral and source code discussed in this application report can be downloaded from the following URL: <http://www.ti.com/lit/zip/spract6>.

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1 Introduction

When designing a system utilizing C2000 MCUs, evaluating the input circuits that are driving the ADC for proper settling is a necessary step. Inadequate settling can lead to a variety of sampling issues, most commonly signal distortion and memory-crosstalk. This application report explores the methodology presented in the seven-part video series on ADC input settling by TI precision labs: [TI Precision Labs - SAR ADC Input Driver Design](#) in the specific context of the ADCs on C2000 MCUs.

1.1 Mechanism of ADC Input Settling

To convert a sensed analog voltage to a digital conversion result, the ADC first must accurately capture the applied input voltage into its sample-and-hold circuit (S+H). As shown in [Figure 1-1](#), this entails charging the internal ADC S+H capacitor (C_h) to within some acceptable tolerance (typically 0.5 LSBs) of the applied voltage within the configured acquisition window time (also referred to as the S+H time).

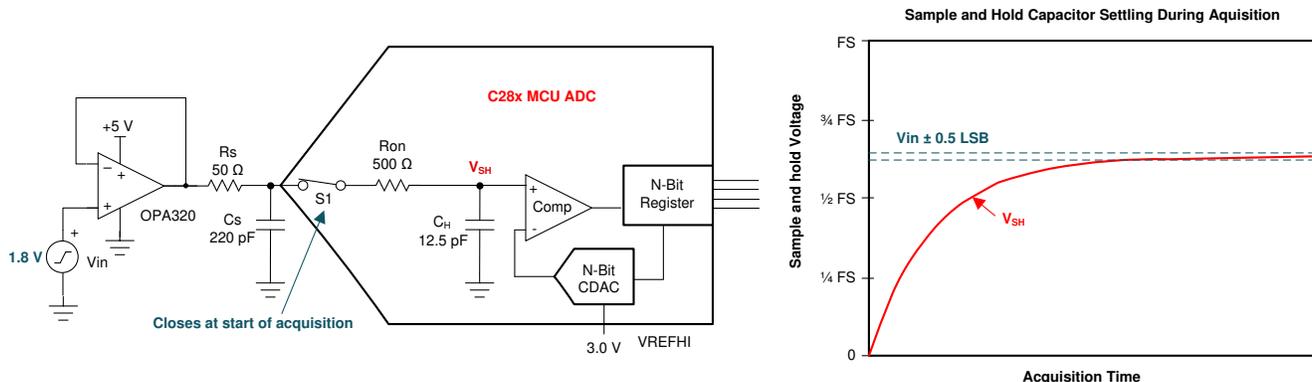


Figure 1-1. Settling of the ADC S+H Capacitor

Quickly charging C_h to the applied voltage is complicated by the finite bandwidth and settling time of the external ADC driver circuit and of the settling time of the internal ADC S+H circuit. In [Figure 1-1](#), the driver is shown as an op-amp (OPA320), which has a finite bandwidth, and the driver circuit also has intentionally placed source resistance (R_s) and intentionally placed source capacitance (C_s) which have a finite settling time determined by their RC time constant. Note that other circuit topologies are possible for driving the ADC, and these circuits may have additional components which need to be modeled to ensure appropriate settling time. These components could include unintentional parasitics such as the output impedance of a sensor or the effective source resistance of a voltage divider. [Figure 1-1](#) also shows that the ADC has an internal parasitic switch resistance (R_{on}). This, along with C_h , will provide an additional RC time constant that limits settling speed.

1.2 Symptoms of Inadequate Settling

Once a voltage has been captured into the S+H capacitor, the ADC will translate this voltage into a digital conversion result during the conversion phase. The CPU can then use this result to control or monitor the system. However, if the captured voltage does not accurately represent the applied voltage due to settling error, the final conversion result will have errors even if the ADC conversion process is perfect.

These settling errors will manifest differently depending on whether the ADC is sampling the same channel repeatedly or scanning through multiple channels in a sequence. The settling errors will also manifest differently depending on the starting voltage on the S+H capacitor at the beginning of the acquisition phase. Some ADC architectural implementations will have a starting S+H voltage close to the previously sampled voltage while other architectures will usually start the acquisition phase with a discharged S+H capacitor.

Distortion

In the case where the ADC is repeatedly sampling the same signal, settling error typically manifests as distortion of the input signal. In architectures where the S+H voltage starts near the previously sampled voltage, slow moving portions of the input signal will settle better than fast moving portions. An architecture where sequential samples begin their settling from the voltage sampled and held in the previous conversion is illustrated in Figure 1-2.

In architectures where the S+H capacitor starts each acquisition phase discharged, higher input voltages will have worse settling, resulting in distorted scaling of the signal. An architecture where sequential samples always beginning their settling from near zero-scale is illustrated in Figure 1-3.

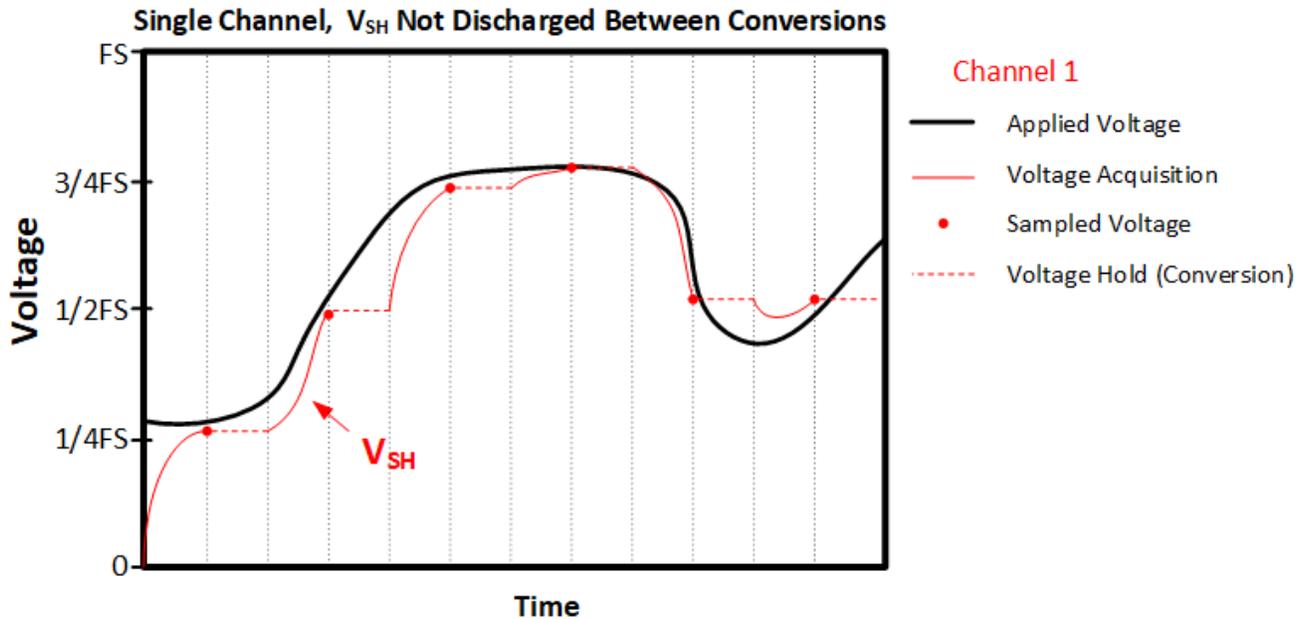


Figure 1-2. Sequence of Samples With C_H Retained Between Conversions

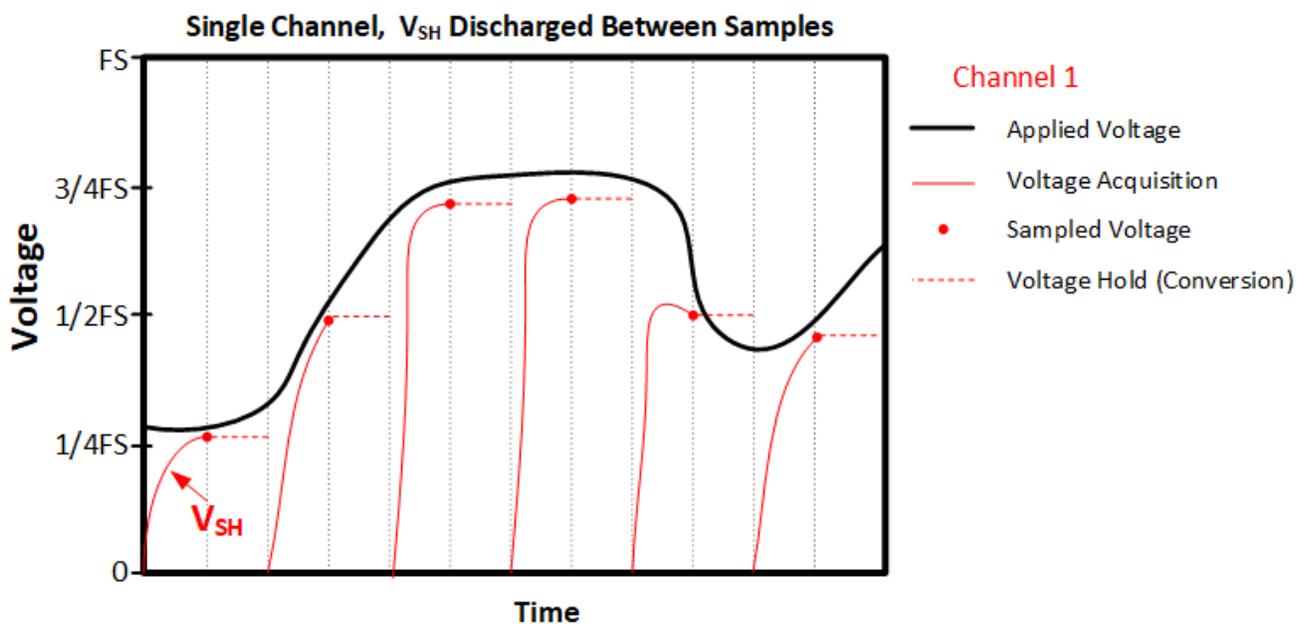


Figure 1-3. Sequence of Samples With C_H Discharged Between Conversions

Memory Cross-Talk

In many C2000 MCU applications, a typical use case is using the ADC input multiplexer to scan through multiple channels in a sequence. If a converted channel has inadequate settling, the channel may be pulled towards the voltage of the previous conversion in the sequence. This occurs because the S+H voltage starts near the previously converted voltage and then settles towards (but does not reach) the applied voltage. This tendency for the previous conversion result in a sequence of conversions to affect the current conversion is called memory cross-talk. Memory cross-talk can generally be completely mitigated via appropriate settling design.

A situation where a shared sample and hold must settle back-and-forth between two different multiplexed input signals is illustrated in [Figure 1-4](#).

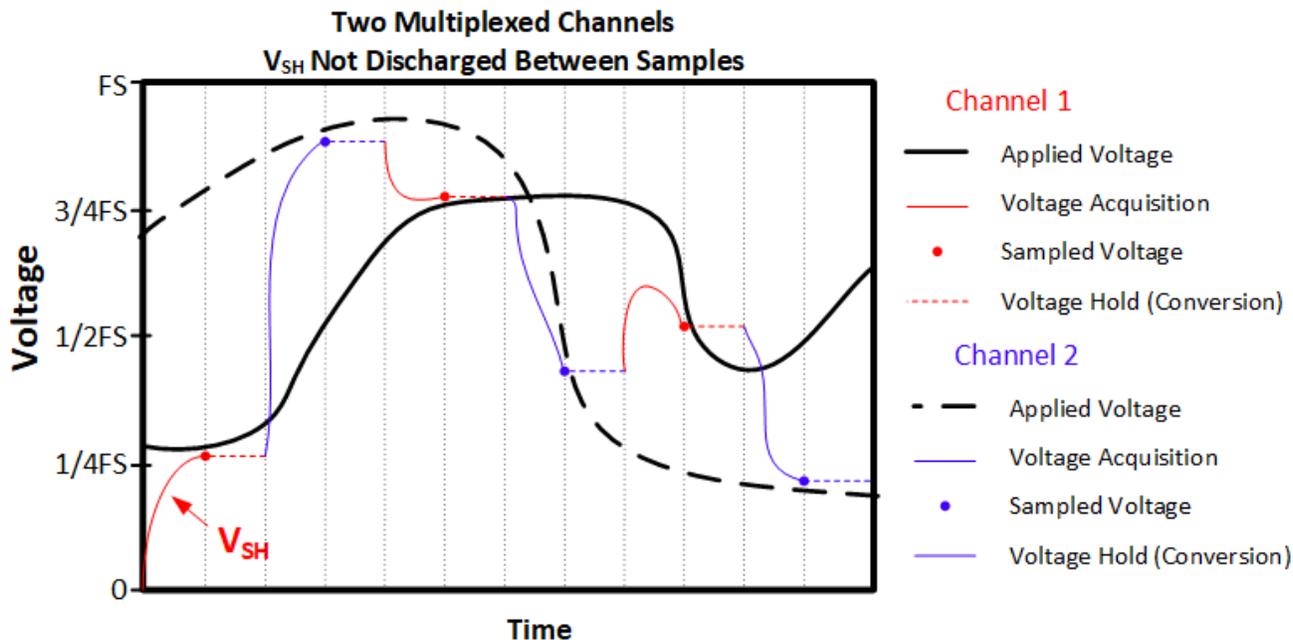


Figure 1-4. Sequence of Multiplexed Samples

Converter architectures that start with the S+H capacitor completely discharged generally do not experience significant memory cross-talk (but still experience input settling related distortion if the ADC driving circuits are not appropriate for the allocated acquisition time).

Accuracy

The errors introduced by inadequate input settling generally can not be calibrated out or reduced via oversampling and averaging. Therefore, applications that are concerned with absolute sampling accuracy also need to ensure proper ADC input settling even if the sensed input signal is low-frequency or even DC.

C2000 ADC Architecture

C2000 MCU ADCs will generally start with the S+H capacitor pre-charged to a voltage close to the previous conversion result. The exception to this is for ADCs which support differential signaling, but which are operating in single-ended mode. In this case, the S+H capacitor will start discharged when the previous conversion was from an even numbered channel and the current channel is an odd numbered channel, or vice-versa. For example, the S+H capacitor will start discharged if channel A4 is being sampled after A3 (or vice-versa) but will start close to the previously converted voltage when sampling channel A4 after channel A2 or channel A1 after channel A3.

CAUTION

The above statements about the C2000 ADC architecture are only intended to help with diagnosing problems with inadequate settling. Do not rely on these properties to ensure sufficient ADC input settling. Instead, always ensure that the input can fully settle in the allocated S+H time regardless of any assumptions about the starting voltage of the S+H circuit.

1.3 Resources for ADC Input Circuit Design and Evaluation

The following tools and materials are needed for ADC driver circuit design and evaluation for input settling.

TI Precision Labs - SAR ADC Input Driver Design Series

TI precision labs has provided an excellent seven-part video series that demonstrates how to design the input drivers for a SAR ADC. This application report will show how to apply the TI precision labs simulation and analysis methods to C2000 ADCs. Review this video series before proceeding; the rest of the report will assume that you have already done this.

Link to Video Training Series: [TI Precision Labs - SAR ADC Input Driver Design](#)

Analog Engineer's Calculator

The analog engineer's calculator tool provides a variety of very useful GUI-based calculation tabs to assist with common analog circuit design tasks. The TI Precision labs methodology takes advantage of the Data Converters -> ADC SAR Drive calculator. Ensure that this calculator is downloaded and installed before proceeding.

Link to Tool Folder: [Analog Engineer's Calculator](#)

TINA-TI SPICE-Based Analog Simulation Program

TI provides the TINA-TI application to TI customers to allow easy SPICE-based simulation of circuits utilizing TI products. The TI Precision labs input settling design methodology uses TINA-TI to perform a number of simulations to refine and verify the input circuit design for proper settling. Ensure this application is downloaded and installed before proceeding.

Link to Tool Folder: [TINA-TI™](#)

2 Input Settling Design Steps

The [TI Precision Labs - SAR ADC Input Driver Design](#) methodology to design an ideal ADC input driver can be broken into the steps below. Subsequent sections will discuss how these steps can be applied to C2000 ADCs.

1. Select the ADC.
2. Find the minimum op-amp bandwidth and RC filter ranges.
3. Select an op-amp.
4. Verify the op-amp model.
5. Build the ADC input model.
6. Refine RC filter values via simulation.
7. Perform final simulations

2.1 Select the ADC

It is assumed that you have already selected a C28x based microcontroller with one or more integrated ADCs modules. The C28x product search can be used to select an MCU: [C2000 real-time control MCU - Products](#) and the C2000 peripheral guide enumerates the differences between peripherals on different devices (including the ADC): [C2000 Real-Time Control MCU Peripherals Reference Guide](#).

Once a C2000 device has been selected, you should locate the following information in the device-specific data manual before proceeding.

Data Manual Information	Location	Comments
Minimum sample window duration	"ADC Operating Conditions" table in the "ADC Electrical Data and Timing" section	Some devices support multiple resolutions modes and signaling modes; ensure that the parameter correspond to the mode you intend to use.
ADC input model	"Input Model Parameters" table in the "ADC Input Model" section	Some devices support multiple resolutions modes and signaling modes; ensure that the model correspond to the mode you intend to use.
Specific parasitic capacitance for selected ADC pin	"Per-Channel Parasitic Capacitance" table in the "ADC Input Model" section	If channel assignment is not yet known, use the value for ADCIN15
ADC timings	"ADC Timings" table in the "ADC Timing Diagrams" section	Some devices support multiple resolutions modes and signaling modes; ensure that the timings correspond to the mode you intend to use. You will also need to know your intended CPU clock (SYSCLK) and ADC clock (ADCCLK) rate. If not yet known, use the maximum ADCCLK value given in the "ADC Operating Conditions" table along with the maximum SYSCLK for the device.

2.2 Find the Minimum Op-Amp Bandwidth and RC Filter Ranges

Once you have located the detailed ADC information in the device-specific data manual, you can use the [Analog Engineer's Calculator](#) to determine the minimum required driving op-amp bandwidth as well as the potential ranges of the external source resistor and external source capacitor to put on the ADC input.

Open the Analog Engineer's Calculator application and select the calculator Data Converters -> ADC SAR Drive calculator. This will give a calculator window similar to that shown in [Figure 2-1](#).

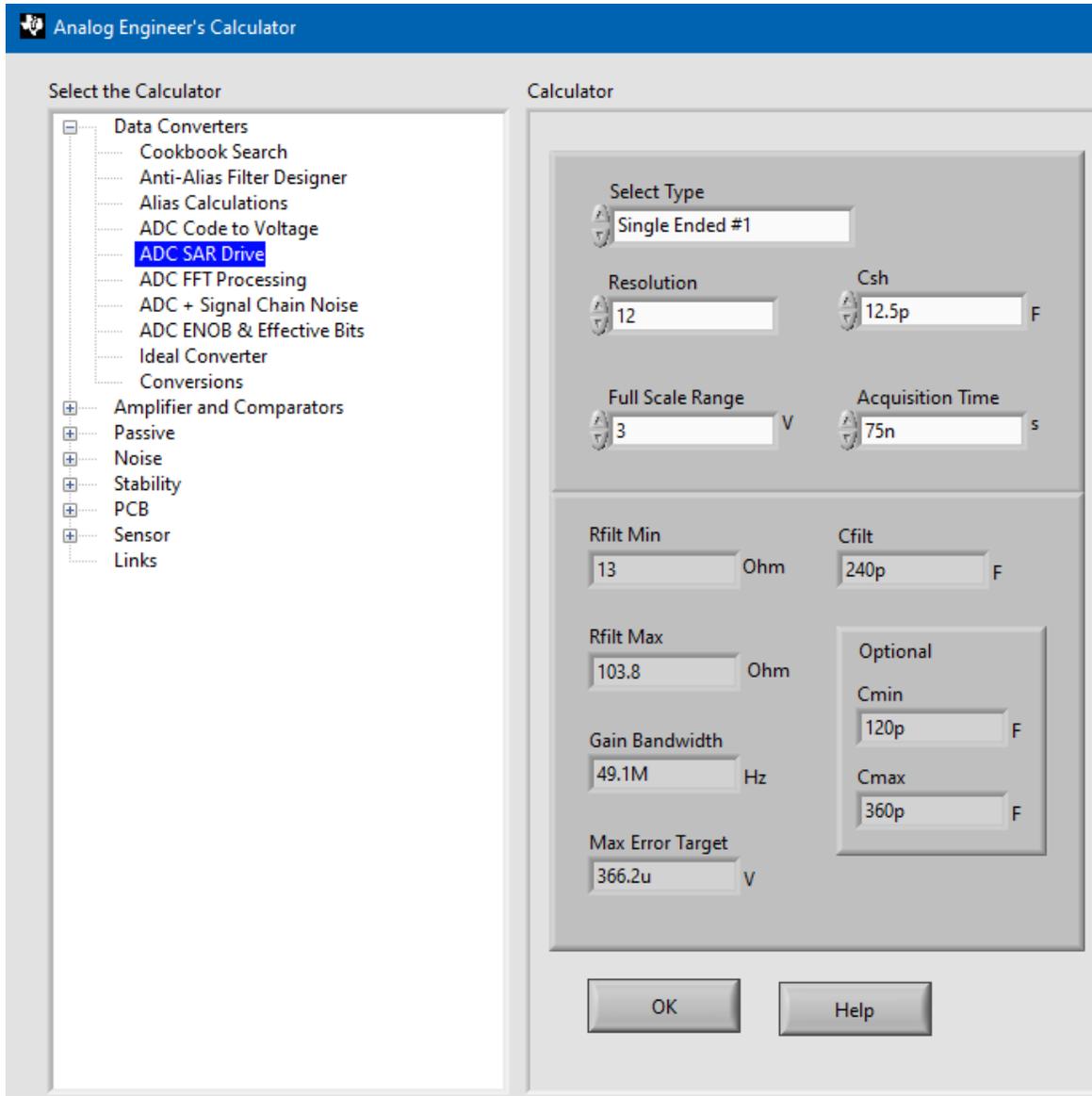


Figure 2-1. Screenshot of Analog Engineer's Calculator

Once the correct calculator is open, enter the input information:

Select Type

C2000 ADCs can be configured as either single-ended input mode or differential input mode depending on the particular device. The calculator allows several input mode types. [Table 2-1](#) maps the C2000 input modes to calculator selection types.

Table 2-1. Calculator Input Type Map

C2000 Signal Mode	Calculator Input Type Selection
Single-ended	"Single Ended #1"
Differential	"Differential"

Resolution

Enter the resolution of the ADC mode to be used in bits. For C2000 ADCs this will usually be 12-bits or 16-bits.

Usually the actual resolution of the ADC will be selected. However, in cases where an ADC channel does not need to utilize the full resolution of the ADC, a lower value can be entered to relax the input settling design requirements.

For example:

Resolution = 12 bits, $C_{sh} = 12.5$ pF, Full-scale range = 3.0 V, Acquisition duration = 100 ns

- Full resolution of 12 bits requires minimum op-amp bandwidth of 37 MHz and settling to better than 0.366 mV
- Reduced resolution of 10 bits (approximately 0.1% settling) requires a minimum op-amp bandwidth of 28 MHz and settling to better than 1.465 mV

C_{sh}

Enter the value of the ADC S+H capacitor. This can be found as the parameter " C_h " in the *Input Model Parameters* table in the device-specific data manual. Different resolutions and reference modes may have different input model parameters, so ensure that the parameter is selected that corresponds to the intended ADC use mode.

Full-Scale Range

Enter the voltage corresponding to the full-scale range of the ADC. When using external reference mode, this corresponds to the voltage supplied on the VREFHI pin of the ADC, usually 2.5 V or 3.0 V. When using internal reference mode (on supported devices), this corresponds to the voltage range of the selected reference mode (2.5 V or 3.3 V).

Acquisition Time

Enter the target ADC acquisition window time. For the lowest ADC conversion latency (corresponding to the maximum ADC sample rate), select the minimum value of the parameter "Sample window duration" in the *ADC Operating Conditions* table in the device-specific data manual.

Selecting a target S+H time larger than the ADC minimum acquisition time can ease the input settling design requirements for the input driving op-amp.

For example:

Resolution = 12- bits, $C_{sh} = 12.5$ pF, Full-scale range = 3.0 V

- Acquisition time = 75 ns requires a driving op-amp with around 50 MHz of bandwidth
- Acquisition time = 150 ns requires a driving op-amp with around 25 MHz of bandwidth
- Acquisition time = 750 ns requires a driving op-amp with around 5 MHz of bandwidth

These decisions can be made on a per-channel basis since the C2000 ADC wrapper allows per-SoC configuration of the S+H time (by using the ACQPS setting in the SoC control register).

Outputs

Once all inputs have been provided to the calculator, record the outputs for later analysis

- R_{fit} and C_{fit} output ranges will be explored via TINA-TI simulation in order to determine an optimal driver circuit
- The max error target output corresponds to 1/2 LSBs at the specified resolution. The final TINA-TI simulation will be considered successful if the settling is within this bound.
- The gain bandwidth output will be used in the next step to select an appropriate op-amp. The selected op-amp should have a unity-gain bandwidth of this value or better for best settling performance.

Math Behind the Calculator

Additional information about analytically determining the required op-amp bandwidth and ranges of R_{fit} and C_{fit} can be found in the final TI Precision Labs video in the SAR ADC Input Driver Design series: [Math Behind the R-C Component Selection](#).

2.3 Select an Op-Amp

An appropriate op-amp next needs to be selected for the ADC driver circuit. This op-amp needs to meet the minimum unity gain bandwidth reported by the Analog Engineer's calculator.

Additional instructions for selecting the op-amp are given in the TI Precision Labs video: [Selecting and Verifying the Driver Amplifier](#).

If selecting an op-amp to meet the specified requirements is proving difficult, remember that both the settling resolution and the target acquisition time can be relaxed (if the application requirements allow) to relax the driving op-amp requirements. These can both be adjusted on a per-channel basis to allow critical ADC inputs to have optimal performance while axillary ADC inputs can be allowed to have relaxed performance.

2.4 Verify the Op-Amp Model

Next, it is necessary to obtain the TINA-TI model for the op-amp selected in the previous step.

The TI Precision Labs video [Selecting and Verifying the Driver Amplifier](#) provides detailed instructions on how to obtain the TINA-TI model for the selected op-amp as well as how to verify the model against the information provided in the device-specific data manual.

2.5 Build the ADC Input Model

To simulate and refine the ADC input driver circuit in TINA-TI, it is first necessary to build a TINA-TI input model for the ADC. The TI Precision Labs video [Building the SAR ADC Input Model](#) outlines how to perform this process based on the information provided in the device-specific data manual for an ADC device. This application report is bundled with pre-generated ADC input models for TMS320F2837xD, TMS320F2837xS, TMS320F2838x, TMS320F2807x, TMS320F28004x, and TMS320F28002x family devices, so manual creation of the models is not necessary. However, the video does show how to configure your TINA-TI simulation parameters (via the slides titled "Optimizing Simulation Results").

CAUTION

The first time a settling simulation is run, do not skip the instructions to configure the simulation parameters in the [Building the SAR ADC Input Model](#) video. These instructions can be found in the "Optimizing Simulation Results" section.

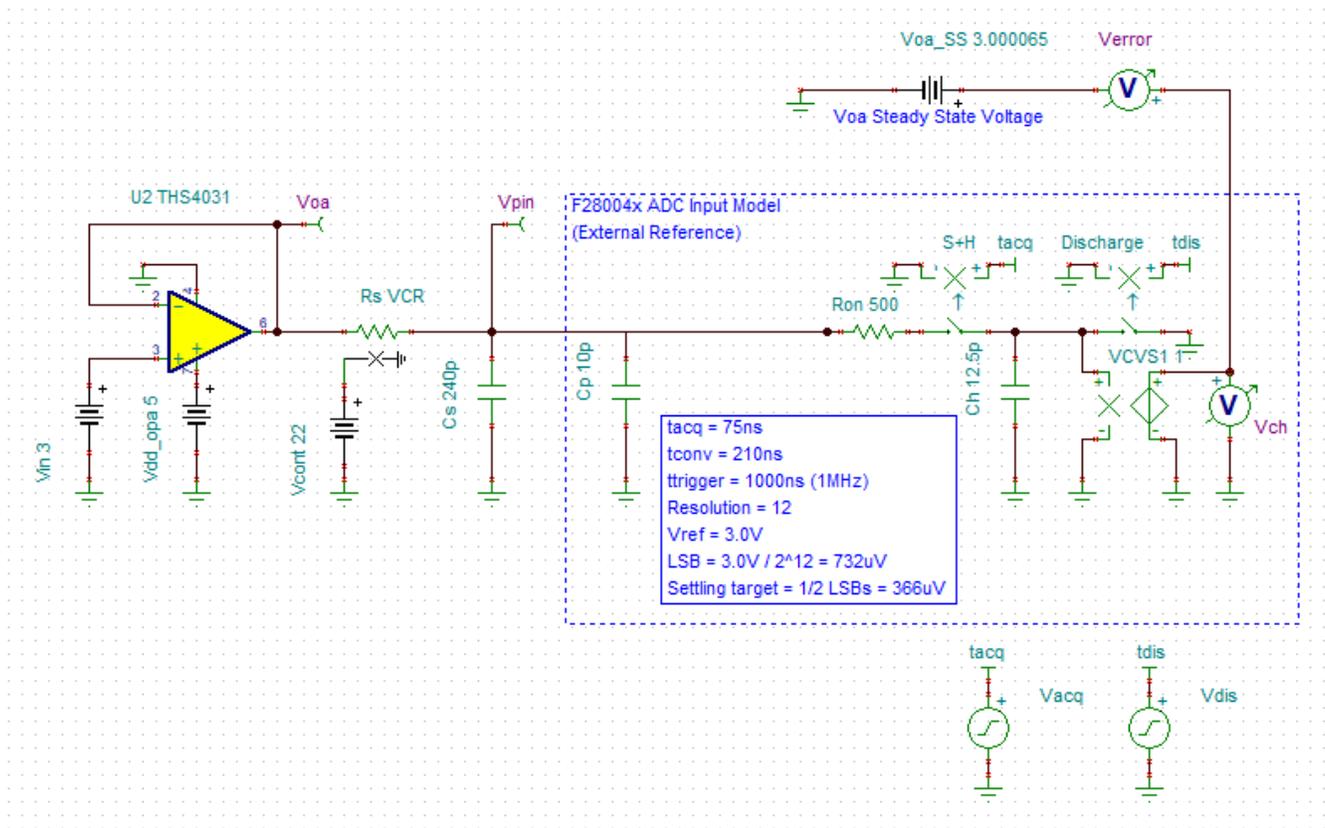


Figure 2-2. F28004x ADC Input Model

An example of one of the provided ADC input models can be seen in [Figure 2-2](#). The following sections briefly describe the primary functions of each model component.

V_{in}

V_{in} is the applied voltage that will be used to charge the S+H capacitor. While any input can be simulated, applying the full-scale input voltage will provide the worst-case DC settling conditions because the S+H capacitor always starts discharged in this model.

V_{oa} , V_{oa_ss} , and V_{error}

TINA-TI op-amp models incorporate various non-idealities, which results in the DC steady state output of the op-amp at V_{oa} not exactly matching V_{in} . The steady state output at V_{oa} can be simulated and entered into V_{oa_ss} such that V_{error} is an accurate representation of only the input settling error.

R_s , C_s , and V_{cont}

R_s and C_s are the source resistance and source capacitance. These values correspond to R_{filt} and C_{filt} in the TI Precision Labs training terminology. R_s resistance is controlled by the control voltage V_{cont} . R_s is a voltage-controlled resistor with gain of 1 (1 V = 1 Ω , 10 V = 10 Ω , and so forth) instead of a simple resistor to allow parameter sweeping when there are two R_s resistors in the differential models.

C_h , R_{on} , and C_p

Component values for the ADC input model.

C_h , the S+H capacitor, corresponds to C_{sh} in the TI Precision Labs training terminology while R_{on} , the S+H switch on resistance, corresponds to R_{sh} .

C_p is the pin-specific input capacitance. This is not modeled in the TI Precision Labs training, but can be optionally added to the simulation to improve simulation accuracy. This is particularly helpful for pins that are multiplexed with VDAC (alternate DAC voltage reference pin) that have a value of C_p , which is greater than 100 pF on most devices.

Pins that are multiplexed with the buffered DAC output on F2837x and F2807x devices have a parasitic 50k Ω pull-down resistor present on these pins. It is recommended to add this resistor to the model (not shown in [Figure 2-2](#)) to better represent behavior of these pins.

CAUTION

While the ADC input models for multiple C2000 devices are bundled with this application report, input model component values should always first be verified with the device-specific data manual before proceeding. Values for C_h and R_{on} can be obtained from the *Input Model Parameters* table in the device-specific data manual while values for C_p can be obtained from the *Per-Channel Parasitic Capacitance* table. In any cases where the device-specific data manual values disagree with the values in this document or in the provided models, the device-specific data manual values should always be considered the correct values.

S+H Switch, Discharge Switch, t_{acq} , and t_{dis}

Switch "S+H" controls when the S+H capacitor, C_h , is being charged by the driving circuit. The timings for this switch are controlled by t_{acq} . Sample t_{acq} timing configurations for a 75 ns acquisition window are shown in [Figure 2-3](#).

Switch "Discharge" controls when the S+H capacitor, C_h , is being reset by being discharged to ground. The timings for this switch are controlled by t_{dis} . Sample t_{dis} timing configurations for a 1 μ s trigger period are shown in [Figure 2-4](#).

When neither t_{acq} or t_{dis} are active, the value of the S+H capacitor is held at its final settled values.

Note that the timings are configured to emulate conversions triggered at a set 1 MHz frequency instead of back-to-back continuous conversions. This more closely emulates the typical C2000 ADC use case of being periodically triggered by the ePWM module. The triggering rate can be modified to match the actual application ePWM trigger rate by modifying the period of the t_{acq} and t_{dis} timing sources. Do, however, ensure that the trigger rate is slower than the total S+H plus acquisition time for the ADC conversion. The ADC conversion time can be found in the device-specific data manual table "ADC Timings".

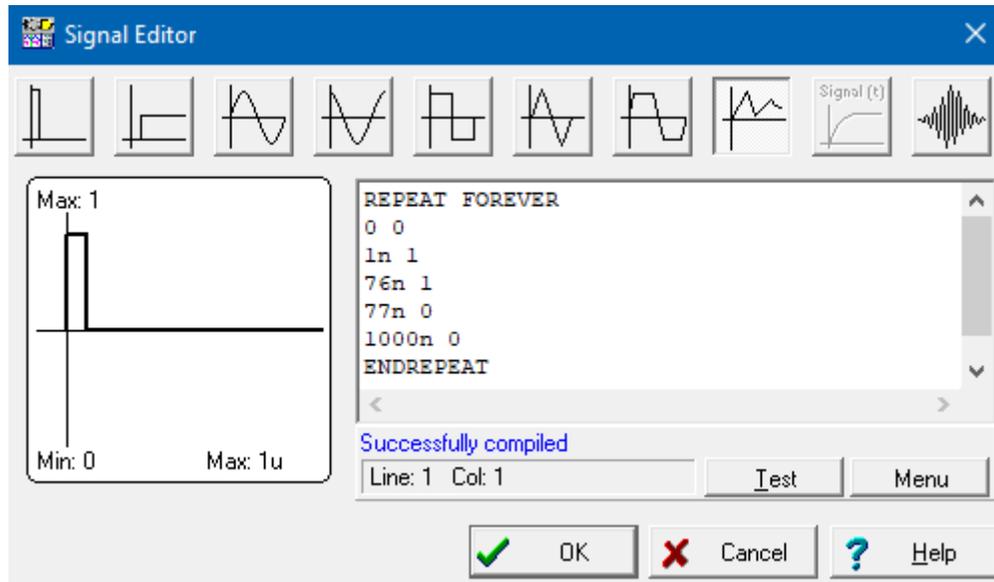


Figure 2-3. Example Timings for t_{acq} (Piecewise Linear)

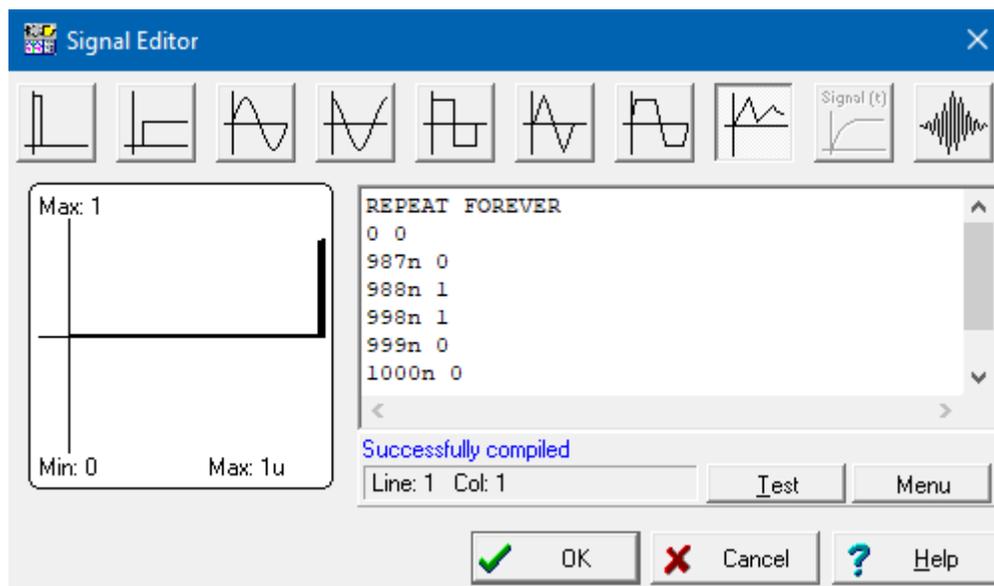


Figure 2-4. Example Timings for t_{dis} (Piecewise Linear)

2.6 Refine RC Filter Values Via Simulation

Once the ADC input model has been combined with the op-amp simulation model, simulation can be used to select the best values of R_s and C_s . In-depth instructions for performing the component refinement simulation can be found in TI Precision Labs video [Refine the Rfilt and Cfilt Values on ADC Drive](#) or by following the input circuit design example in [Section 3](#).

Once optimal values of R_s and C_s have been determined, a final simulation should be performed using the closest available standard component values. This will establish the final settling error, which can be compared to the settling error target obtained from the Analog Engineer's Calculator.

If the settling error does not meet the target, additional iteration is required that will entail evaluating a different op-amp, evaluating different R_s and C_s values, or relaxing the S+H time or settling resolution targets.

2.7 Perform Final Simulations

Additional simulations to verify the robustness of the design can also optionally be performed. These include:

- Simulate with a longer S+H duration to ensure that input is consistently settling
- Observe settling at the op-amp's output node. This node should also settled to within 1/2 LSBs (or the selected settling target) at the end of the acquisition period
- Observe settling over multiple cycles
- Perform settling simulations with an AC input

Information on performing these simulations can be found in the TI Precision Labs video [Final SAR ADC Drive Simulations](#).

2.8 Input Design Worksheet

Table 2-2 summarizes the required inputs and outputs of the input driver evaluation is provided to facilitate driving circuit evaluation.

Table 2-2. ADC Input Settling Design Worksheet

Symbol	Description	Value	Comments
V _{fs}	Full scale voltage range		In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
N	Target settling resolution (bits)		Usually the same as the resolution of the ADC Lower resolution can be targeted to relax the input design requirements
V _{errmax}	Maximum error target		$V_{fs} / 2^{N+1}$ Obtain using Analog Engineer's Calculator: ADC SAR Drive
t _{sh}	S+H time		Enter target S+H time if known Longer S+H times will result in less stringent BW requirements for the driving op-amp. Can be solved for given a pre-determined op-amp selection or a pre-determined R _S and C _S
R _{on}	ADC switch resistance		Provided in the <i>Input Model Parameters</i> table in the device-specific data manual TI precision labs training refers to this as "R _{sh} "
C _h	ADC S+H capacitance		Provided in the <i>Input Model Parameters</i> table in the device-specific data manual TI precision labs training refers to this as "C _{sh} "
C _p	ADC pin parasitic capacitance		Provided in the <i>Per-Channel Parasitic Capacitance</i> table in the device-specific data manual
C _S (range)	Range of source capacitance		Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI precision labs training refers to this as "C _{filt} "
R _S (range)	Range of source resistance		Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI precision labs training refers to this as "R _{filt} "
BW _{OPA}	ADC driver op-amp minimum bandwidth		Obtain using Analog Engineer's Calculator: ADC SAR Drive.
Op-amp	Selected Op-amp part number		Record selected op-amp here
V _{oa_ss}	Steady state op-amp output voltage		Generated from DC nodal analysis of the V _{oa} node Copy to Voa_ss before proceeding with other simulations
C _S (final)	Final source capacitance		Final selected C _S from simulation. TI precision labs training refers to this as "C _{filt} "
R _S (final)	Final source resistance		Final selected R _S from simulation. TI precision labs training refers to this as "R _{filt} "
BW _{R_SC_S}	Filter bandwidth from C _S and R _S		$1 / (2 \pi C_S R_S)$ Note For proper settling, the filter bandwidth will be necessarily higher than the ½ the sampling frequency, thus the combination of C _S and R _S generally will not function as an anti-aliasing filter.
V _{err}	Actual settling error		Ensure V _{err} < V _{errmax} Otherwise, additional iteration on selection of C _S , R _S , or the driving amplifier is needed.

3 Example Circuit Design

The following sections work through and discuss designing an example C2000 circuit for input settling.

Select the ADC

This example assumes an F280049 device in external reference mode ($V_{REFHI} = 3.0\text{ V}$) using channel A0. Triggering will occur at 1 MHz. This ADC supports 12-bit single-ended sampling only.

From the [TMS320F28004xMicrocontrollers Data Manual](#), the following key values are obtained:

- Minimum sample window duration = 75 ns
- $C_h = 12.5\text{ pF}$
- $R_{on} = 500\ \Omega$
- $C_p = 12.7\text{ pF}$
- ADC conversion time = 210 ns (t_{eoc} in the *ADC Timings* table from the [TMS320F28004xMicrocontrollers Data Manual](#)) = 21 SYSCLK cycles, SYSCLK = 100 MHz)

Find the Minimum Op-Amp Bandwidth and RC Filter Ranges

[Figure 3-1](#) shows the inputs and outputs to the Analog Engineer's Calculator for this example. From this, we obtain the following key values:

- $C_s = 240\text{ pF}$ (120 pF to 360 pF range, if needed)
- R_s range = 17 Ω to 138 Ω
- Op-amp minimum bandwidth = 37 MHz
- Settling error target (1/2 LSBs) = 366 μV

Note that, in conjunction with the op-amp selection step, it was found that slightly relaxing the S+H duration from the ADC minimum of 75 ns to 100 ns reduced the required op-amp bandwidth from 50 MHz to 37 MHz. This allowed for an op-amp selection that better met the project constraints (OPA2350) while still meeting the application requirements for sample latency.

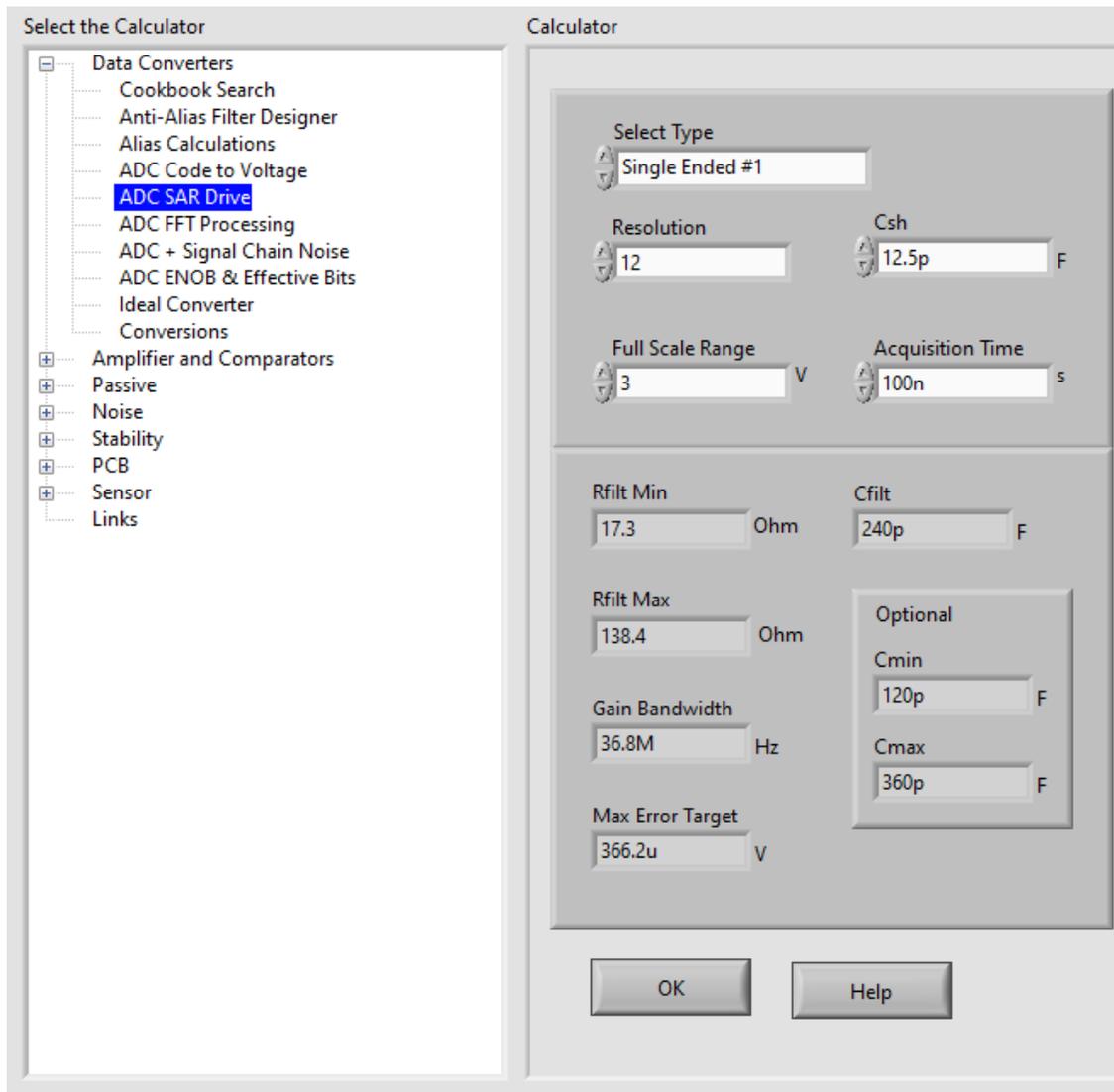


Figure 3-1. F280049 Example Analog Engineer's Calculator Output

Verify the Op-amp Model

The latest OPA2350 model was obtained from ti.com.

Build the ADC Input Model

The OPA2350 model was combined with the provided F28004x_Ext.TSC ADC input model. In addition to setting the driving amplifier to OPA2350, the following were performed on the TINA-TI file to prepare for simulation:

- Op-amp power supplies set to an appropriate voltage (5.0 V and ground)
- V_{in} set to full-scale voltage (3.0 V)
- C_s and C_p initial value set to full-scale voltage (3.0 V)
- V_{oa_ss} set to the voltage obtained from DC nodal voltage analysis (demonstrated in the next section)
- T_{acq} and T_{dis} source period set to 1000 ns (1 MHz trigger frequency)
- T_{acq} source S+H time set to 100 ns
- C_p , R_{on} , and C_h values set based on values obtained from the device-specific data manual
- C_s set to the nominal value provided by calculator
- R_s set to a value in the calculator provided range (by setting V_{cont})

The initial circuit is shown in Figure 3-2 and the timings for t_{acq} and t_{dis} are shown in Figure 3-3 and Figure 3-4.

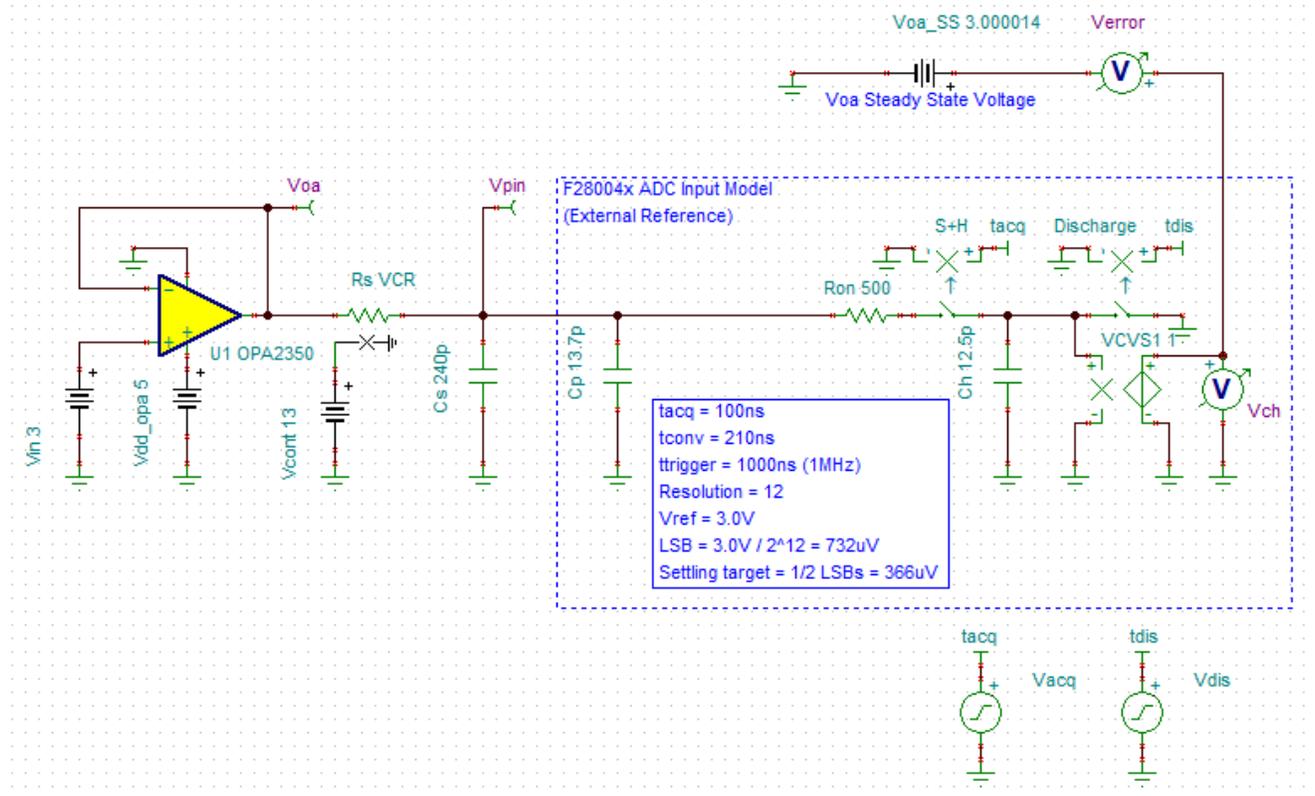


Figure 3-2. F280049 Example TINA-TI Circuit

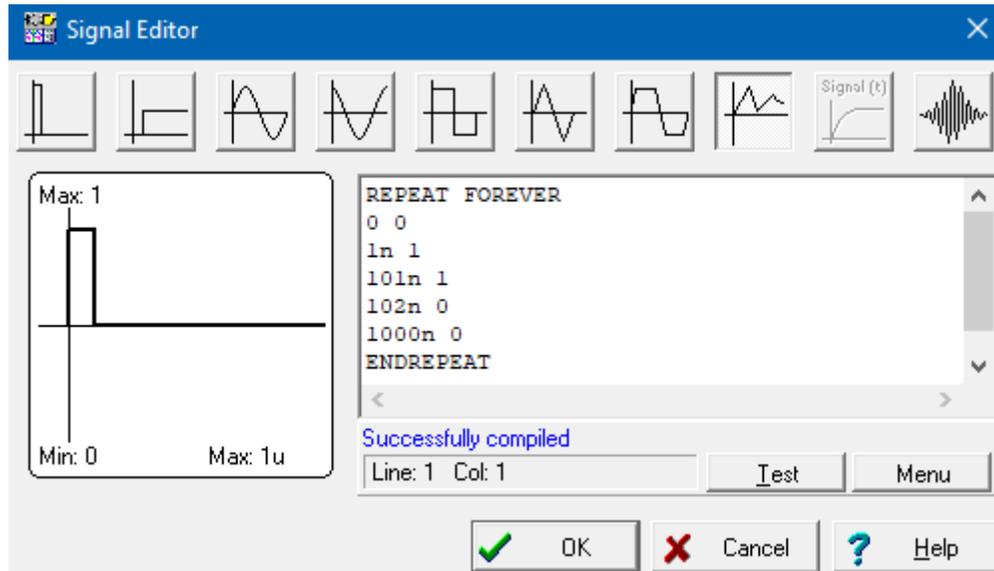


Figure 3-3. F280049 Example T_{acq} Source Timings

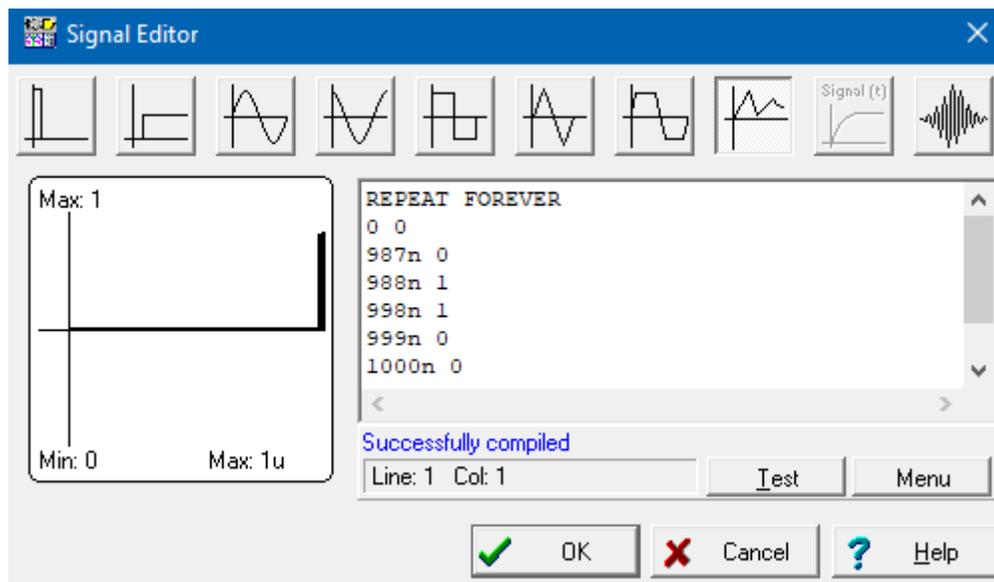


Figure 3-4. F280049 Example T_{dis} Source Timings

DC Node Analysis

To finalize the TINA-TI input model, a DC node analysis is performed to determine the steady-state output value for V_{oa} given the specific op-amp being evaluated (Analysis → DC Analysis → Calculated nodal voltages). For OPA2350 in this circuit, this gives:

- $V_{oa} = 3.000014$ V

Which is then copied to the V_{oa_ss} voltage source.

CAUTION

Ensure that the simulation parameters are configured per the "Optimizing Simulation Results" slides from the [Building the SAR ADC Input Model](#) video.

Refine RC Filter Values Via Simulation (Part 1)

Now that the circuit is setup for simulation, the first step is to run a basic transient analysis to ensure everything is functioning and to check the initial settling. The transient analysis can be run via the TINA-TI menu options: Analysis → Transient...

The settling should be captured after allowing the circuit to stabilize for a couple sampling cycles, so a time period of 2.5 μs to 5.5 μs is selected as shown in Figure 3-5. This allows capture of the full 3rd and 4th sampling cycles (each cycle is 1 μs since the trigger frequency is 1 MHz).

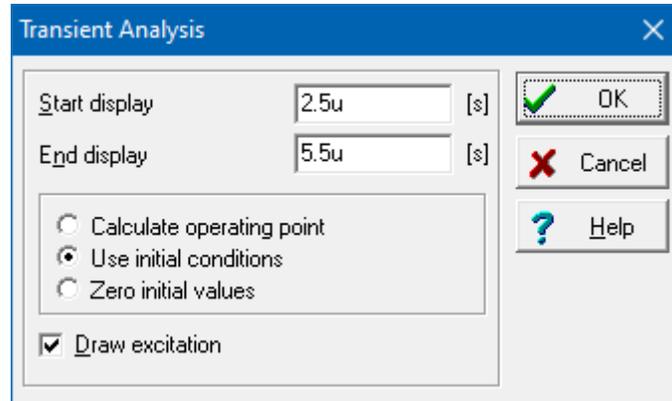


Figure 3-5. F280049 Example Transient Analysis Configuration

Figure 3-6 shows the output waveforms from the transient simulation after separating the outputs (View → Separate outputs). The error voltage scale has also been adjusted to show a range of +10 mV to -10 mV (double-click on V_{error} , then enter -10m in the "Lower limit" field and 10m in the "Upper limit" field, then click "OK").

From this output, it is clear that:

- Discharge and acquisition times are functioning as expected
- The transients on V_{oa} and V_{pin} are of reasonable magnitude (less than 100 mV, so the signal settling will be considered a small signal event)
- V_{error} is settling to about 14 μV , which is well within the error target of 366 μV

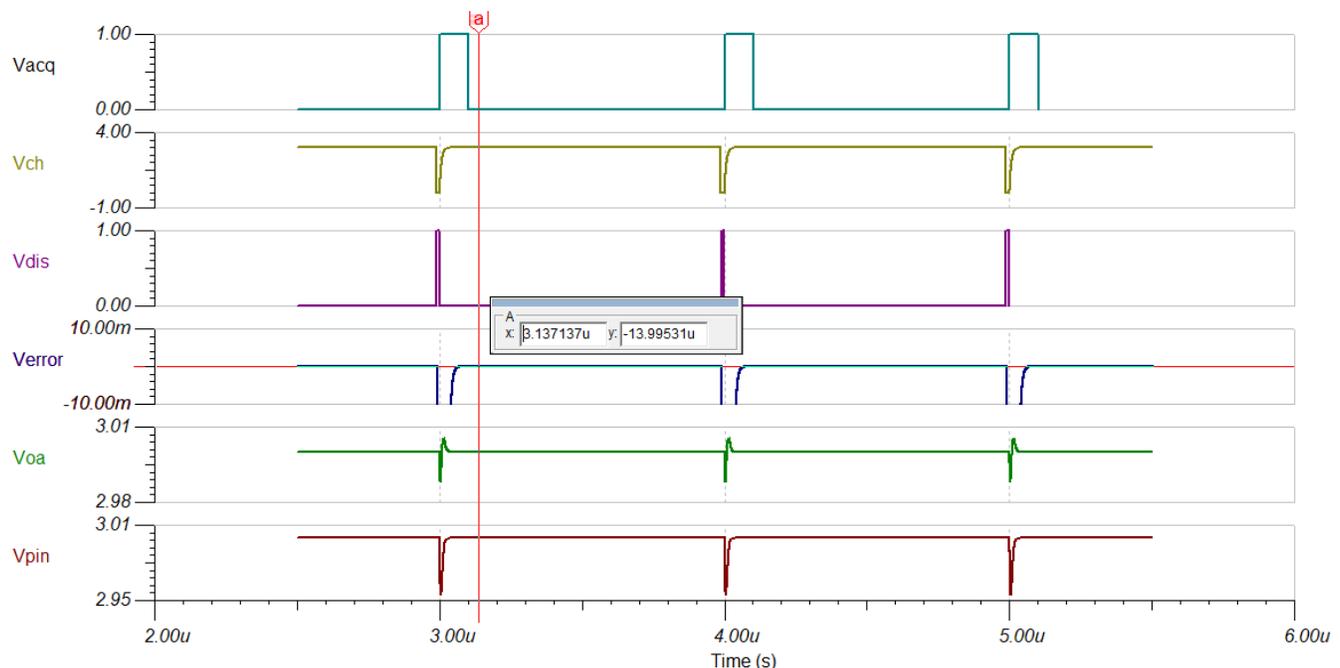


Figure 3-6. F280049 Example Initial Transient Results

Refine RC Filter Values Via Simulation (Part 2)

Now that the basic simulation has shown that the simulation is fundamentally working, sweeps can be performed to refine the R_s component selection.

To perform a sweep, click on the sweep button, then click on the V_{cont} voltage source (which controls the value of R_s).



Figure 3-7. Sweep Button

This will bring up a dialog box. Select the "..." button next to the Voltage [V] parameter and configure the sweep to select 5 points on a linear scale from 13 Ω to 138 Ω as shown in [Figure 3-8](#).

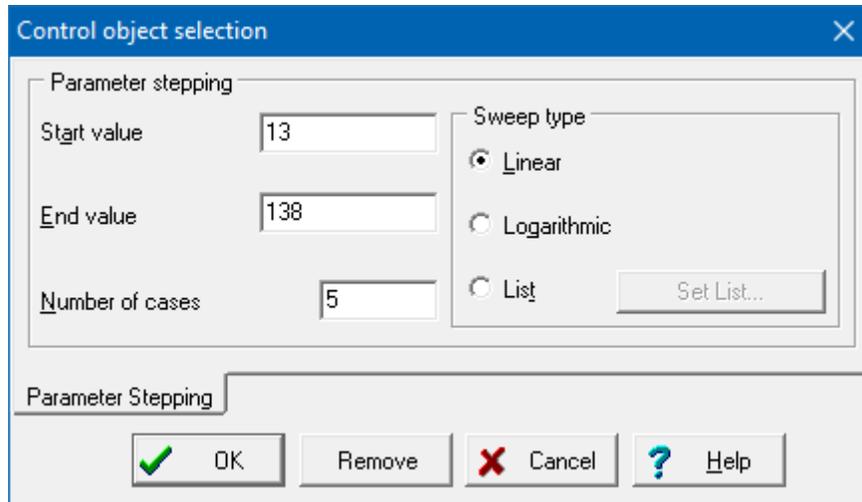


Figure 3-8. F280049 Example Sweep Control Dialog

The output of the transient simulation with a sweep of R_s is shown in Figure 3-9. Note that the outputs have again been separated, and all outputs other than V_{pin} and V_{error} have been deleted. V_{error} range has been set to -50 mV to +50 mV and the waveform has been limited to better observe the settling.

From this output, it can be concluded:

- Higher resistance values in the R_s range do not provide quick enough settling. For instance, 106 Ω only settles to 6.6 mV in the allocated S+H time while the settling target is 366 μ V
- A good range for further investigation would be 10 Ω to 50 Ω

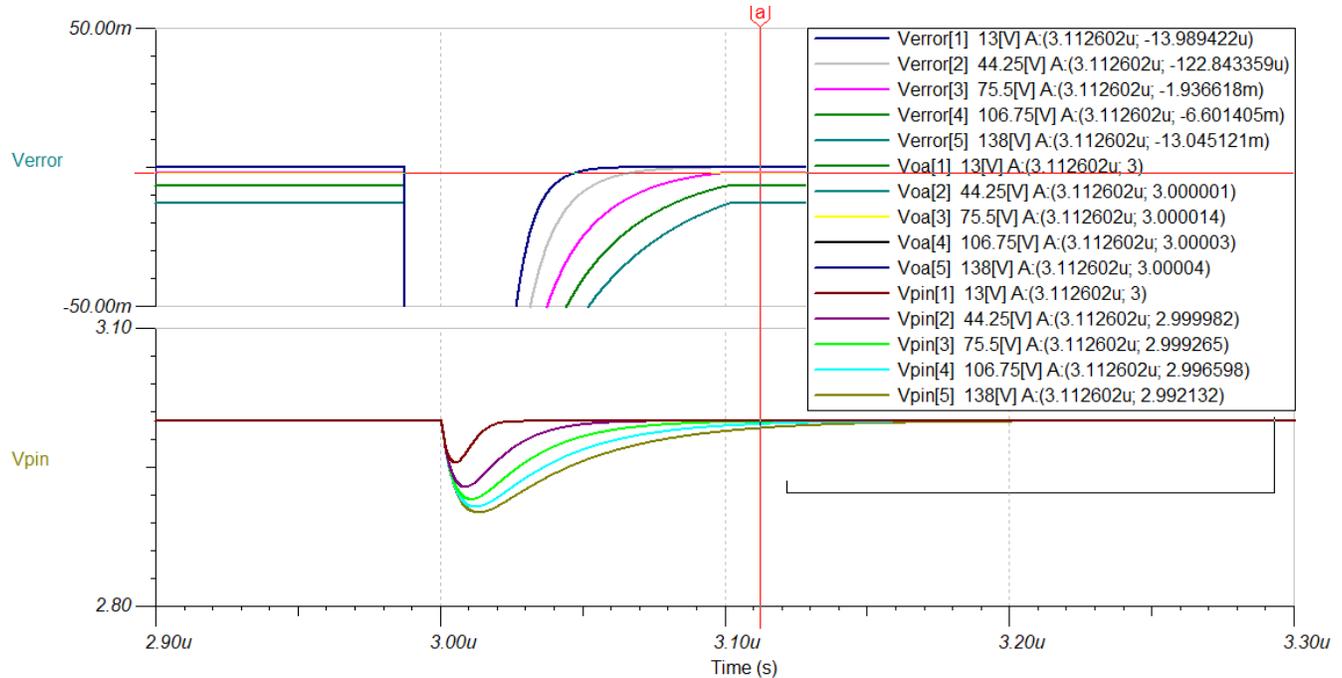


Figure 3-9. F280049 Example R_s Initial Sweep Results

Figure 3-10 shows the results of a sweep of R_s from 10 Ω to 50 Ω . From this set of waveforms, it appears that values of R_s from 10 Ω to 30 Ω all provide settling that greatly exceeds the design target. A final value of R_s was thus selected as 27 Ω .

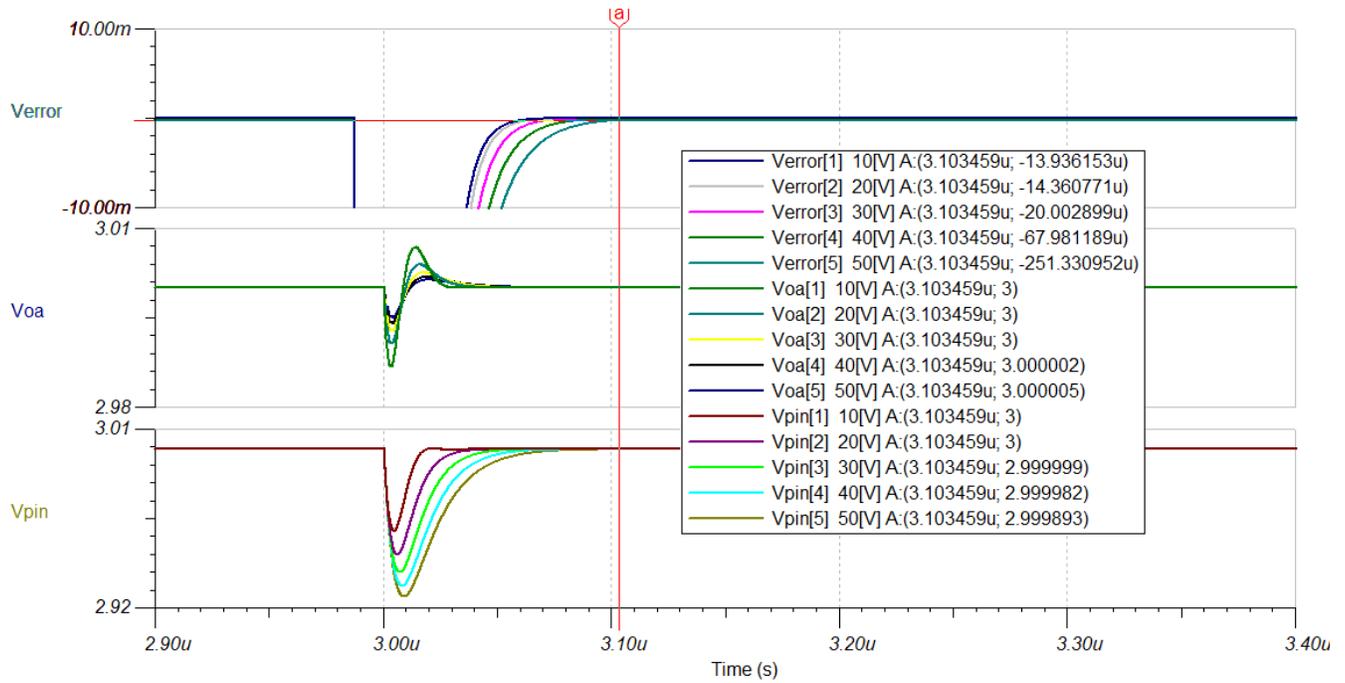


Figure 3-10. F280049 Example R_s Fine Sweep Results

Refine RC Filter Values Via Simulation (part 3)

With the final R_s and C_s values determined, a final transient simulation can be performed to validate the component selections. The results of this final simulation can be seen in Figure 3-11. From these results, it appears that the settling crosses the settling target of $366\ \mu\text{V}$ somewhere around $67\ \text{ns}$ and the final settling at $100\ \text{ns}$ is around $17\ \mu\text{V}$. The final application circuit should have excellent ADC input settling.

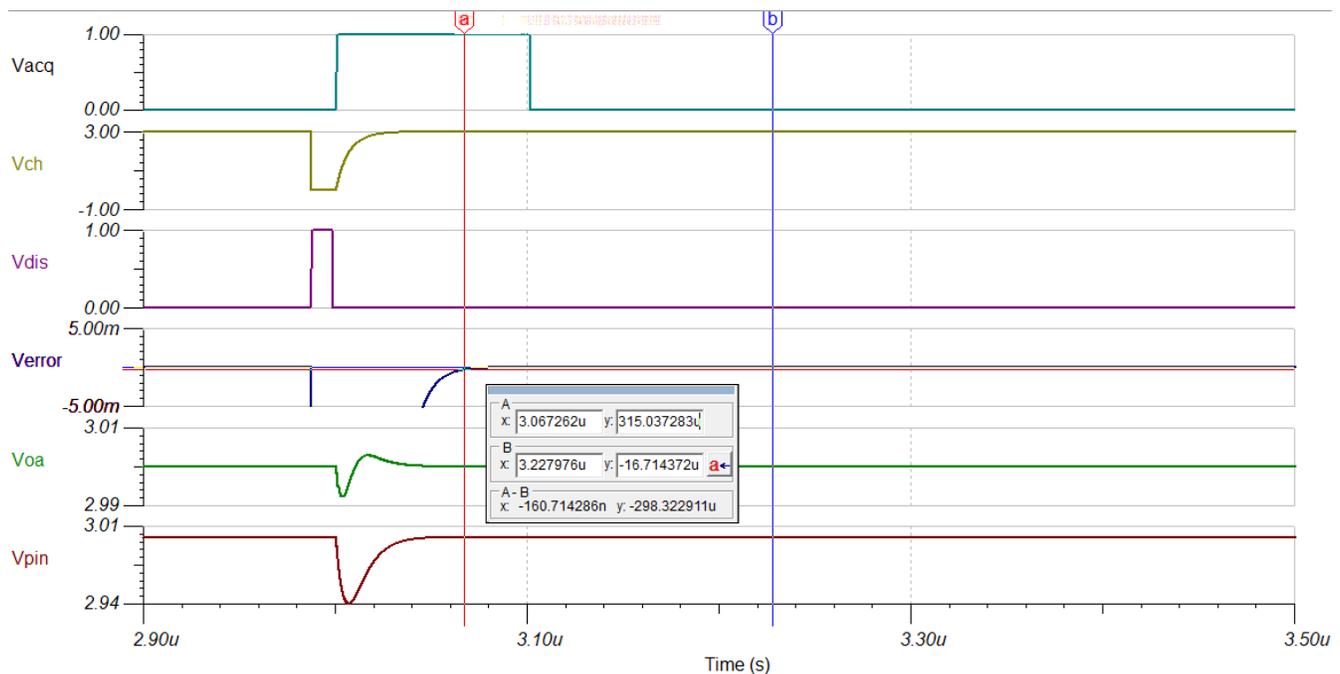


Figure 3-11. F280049 Example Final Transient Results

Further Refinement

Overall, it appears that this design has quite a bit of settling margin. If further optimization is desired, the designer could explore using an op-amp with slightly lower bandwidth. Alternately, the simulation supports using a S+H window that is shorter than $100\ \text{ns}$, if desired.

Another area refinement is to resolve a circuit with intentionally higher R_s and C_s . As designed, the low-pass filter bandwidth of the R_s and C_s circuit is about $2.5\ \text{MHz}$, so this circuit provides some rejection of high-frequency noise. By intentionally increasing R_s and C_s , the filter bandwidth can be lowered, resulting in additional noise rejection. However, note that the R_s and C_s circuit can generally not provide a true anti-aliasing filter, as this would necessarily result in a settling time constant that would be much too large to allow proper settling. If a true anti-aliasing filter is needed, this should be built as a separate filter stage before the ADC drive stage.

CAUTION

Even if the simulations indicate that the input could settle faster than the minimum acquisition window specified in the device-specific data manual, do not select an acquisition window that violates the device-specific data manual minimum acquisition window time.

Further Simulations

As indicated in Section 2.7, once the final components are selected, it is possible to perform additional simulations to further validate the design. This design was validated over multiple cycles and with increased S+H duration (not shown). No issues were identified in these additional simulations.

3.1 Completed Worksheet

Table 3-1 shows the completed worksheet for the F280049 with OPA2350 example.

Table 3-1. ADC Input Settling Design Worksheet (F280049 Example)

Symbol	Description	Value	Comments
V_{fs}	Full scale voltage range	3.0 V	In external reference mode, this is the voltage supplied to the VREFHI pin (usually 3.0 V or 2.5 V) In internal reference mode, this is the effective input range based on the selected reference mode (usually 3.3 V or 2.5 V)
N	Target settling resolution (bits)	12 bits	Usually the same as the resolution of the ADC Lower resolution can be targeted to relax the input design requirements
V_{errmax}	Maximum error target	366 μ V	$V_{fs} / 2^{N+1}$ Obtain using Analog Engineer's Calculator: ADC SAR Drive
t_{sh}	S+H time	100 ns	Enter target S+H time if known Longer S+H times will result in less stringent BW requirements for the driving op-amp. Can be solved for given a pre-determined op-amp selection or a pre-determined R_S and C_S
R_{on}	ADC switch resistance	500 Ω	Provided in the data manual table "Input Model Parameters" TI precision labs training refers to this as " R_{sh} "
C_h	ADC S+H capacitance	12.5 pF	Provided in the data manual table "Input Model Parameters" TI precision labs training refers to this as " C_{sh} "
C_p	ADC pin parasitic capacitance	12.7 pF	Provided in the data manual table "Per-Channel Parasitic Capacitance"
C_S (range)	Range of source capacitance	240 pF (120pF to 360pF)	Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI precision labs training refers to this as " C_{filt} "
R_S (range)	Range of source resistance	17 to 138 Ω	Obtain using Analog Engineer's Calculator: ADC SAR Drive. TI precision labs training refers to this as " R_{filt} "
BW_{OPA}	ADC driver op-amp minimum bandwidth	37 MHz	Obtain using Analog Engineer's Calculator: ADC SAR Drive.
Op-amp	Selected Op-amp part number	OPA2350	Record selected op-amp here
V_{oa_ss}	Steady state op-amp output voltage	3.000014 V	Generated from DC nodal analysis of the V_{oa} node Copy to V_{oa_ss} before proceeding with other simulations
C_S (final)	Final source capacitance	240 pF	Final selected C_S from simulation. TI precision labs training refers to this as " C_{filt} "
R_S (final)	Final source resistance	27 Ω	Final selected R_S from simulation. TI precision labs training refers to this as " R_{filt} "
$BW_{R_S C_S}$	Filter bandwidth from C_S and R_S	2.5 MHz	$1 / (2 \pi C_S R_S)$ Note For proper settling, the filter bandwidth will be necessarily higher than the $\frac{1}{2}$ the sampling frequency, thus the combination of C_S and R_S generally will not function as an anti-aliasing filter.
V_{err}	Actual settling error	17 μ V	Ensure $V_{err} < V_{errmax}$ Otherwise, additional iteration on selection of C_S , R_S , or the driving amplifier is needed

4 Working With Existing Circuits or Additional Constraints

The TI Precision Labs design methodology explored in this report start by assuming a S+H window is known and that the op-amp and R_s and C_s have not yet been determined. The following sections provide some guidance if one or more of these components has already been selected or otherwise needs to be constrained.

4.1 Existing Circuits

Fully determined input driving circuits can of course be simulated to check their settling using the provided ADC input models and simulation methodology.

Note that it is especially important to verify the performance over many sampling cycles for existing circuits that were not designed using the TI Precision Labs methodology. One common case where this is important is when the input was designed using a "charge-sharing" design methodology.

Brief Overview of Charge Sharing

Normally, as the size of C_s increases, the settling time will also increase. It is generally not advantageous to make C_s very large. However, if C_s becomes sufficiently large, it can fully provide all the charge needed to drive C_h to within the settling error target, regardless of the value of R_s .

The external source still needs to recharge C_s through R_s in the time between samples, otherwise each sample will slowly deplete the voltage on C_s . This results in a sample-rate limitation based on the magnitude of the R_s resistance.

For 1/2 LSBs settling, the critical value of C_s occurs at $C_s = 2^{(N+1)} \times C_h$.

Charge Sharing Example

In the example circuit in Figure 4-1, C_s has been set to approximately $2^{(N+1)} \times C_h$ and the sample trigger rate is set to 100 kHz.

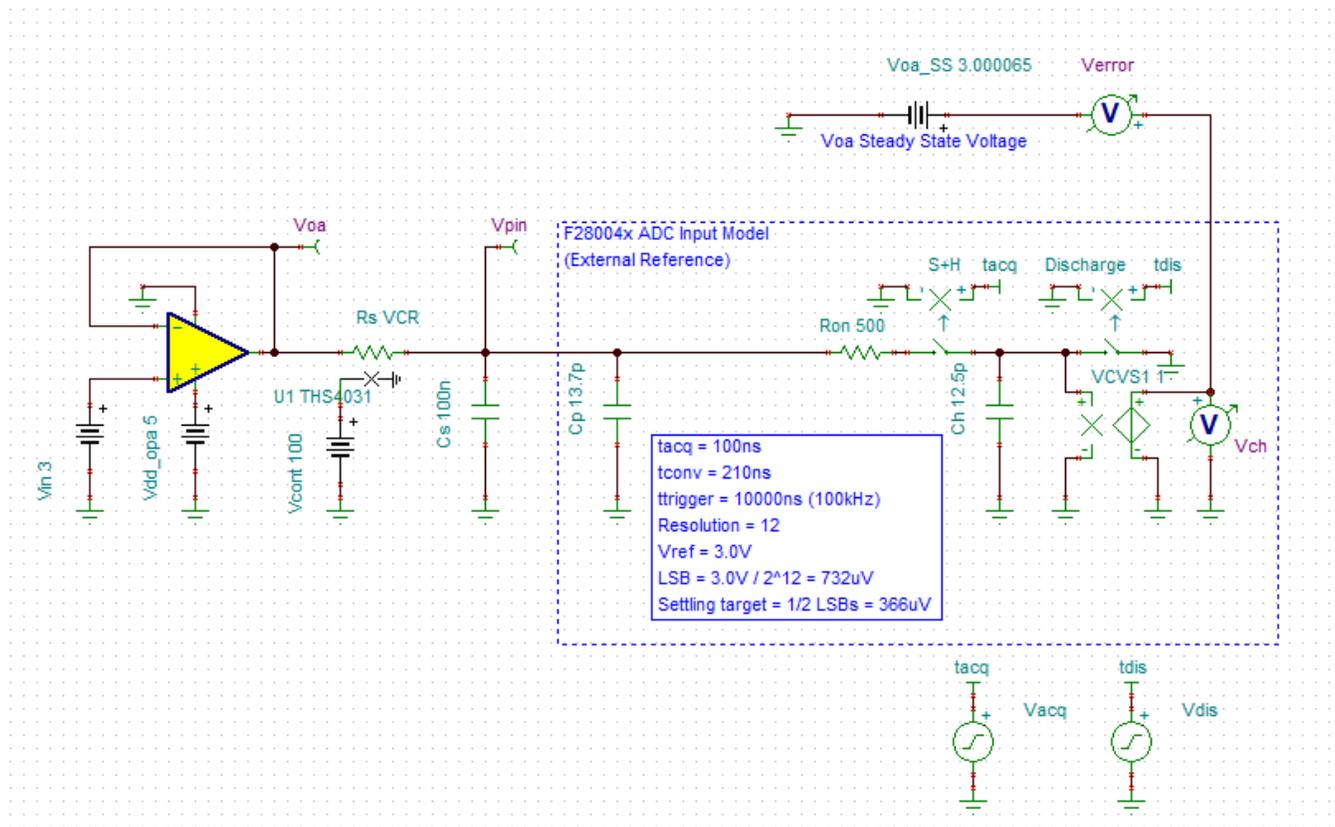


Figure 4-1. Example Circuit Utilizing Charge Sharing

Figure 4-2 shows the pin transient over many sampling cycles when R_s is $100\ \Omega$. It can be seen that the voltage on the pin (which is the voltage directly on C_s) recovers to within 1/2 LSBs in the time between conversions. This will result in good ADC input settling using a very short S+H window as long as the sample-rate remains at or below 100 ksp/s.

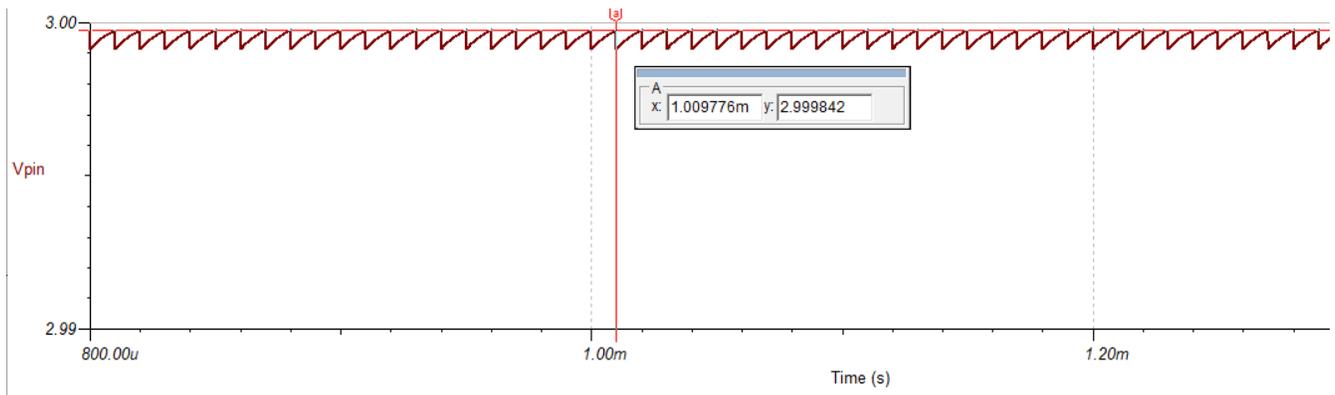


Figure 4-2. C_s Voltage With $R_s = 100\ \Omega$

Now consider the results in Figure 4-3. R_s has been set to $1\text{ k}\Omega$. In this case, the voltage on C_s is slowly depleted sample-by-sample until an equilibrium is reached. At equilibrium, the pin voltage has an error of about 3.5 mV. Even though C_h will quickly match the C_s voltage during the S+H phase, the voltage on C_s has a significant error.

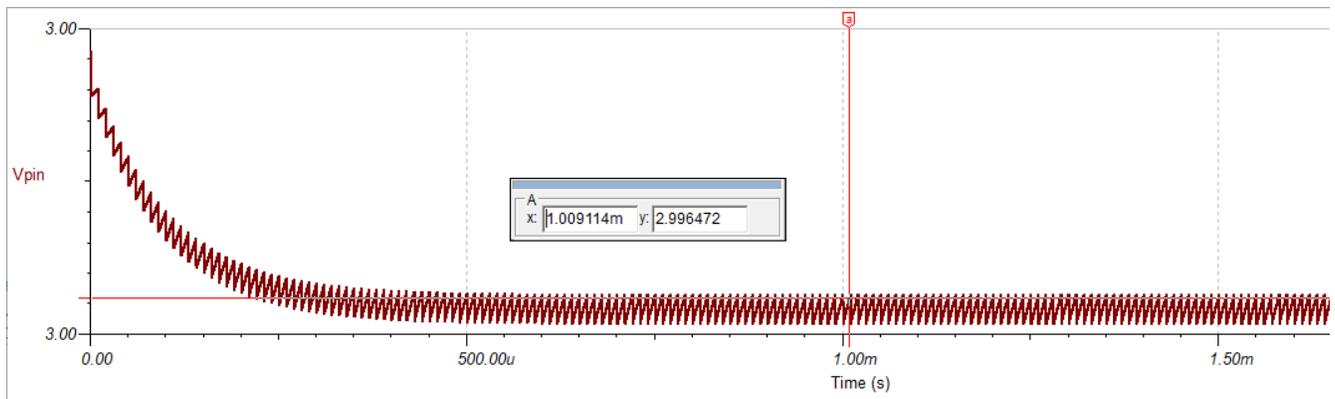


Figure 4-3. C_s Voltage With $R_s = 1\text{ k}\Omega$

To resolve this error, either R_s would need to be decreased or the sample rate would have to be reduced.

This example underscores the importance of simulating circuits with large C_s or R_s over many cycles.

4.2 Pre-Selected Op-Amp

If the op-amp has already been selected for the input driver, the easiest method for proceeding with the design is to iterate the acquisition time setting in the Analog Engineer's Calculator until the necessary bandwidth matches the bandwidth of the pre-selected op-amp. The designer can then record the C_s and R_s component ranges and proceed with the design per the existing methodology (assuming that the predicted S+H meets the application's latency or sample rate requirements).

Pre-Selected Op-Amp Example

The designer wants to use OPA2320 as the driving op-amp for an ADC input (perhaps there is a spare channel from an OPA2320 performing another function on the PCB). OPA2320 has a bandwidth of 20 MHz and the ADC in question has a C_h value of 12.5 pF. By iterating the acquisition window input of the calculator, the solution shown in [Figure 4-4](#) is found and thus a S+H window of 185 ns can be targeted.

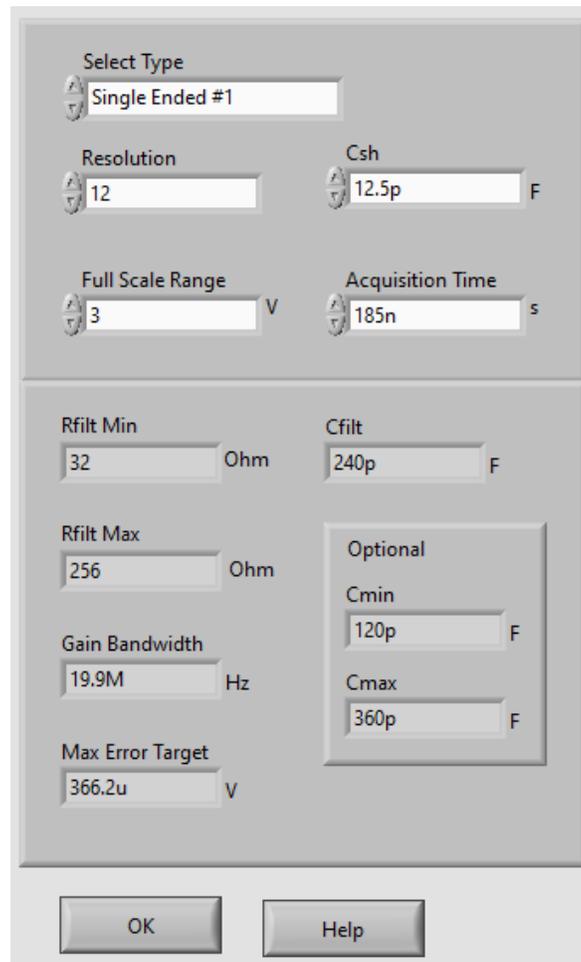


Figure 4-4. Analog Engineer's Calculator Output for OPA2320

4.3 Pre-Selected R_s and C_s Values

If both external source components have been pre-selected, a target acquisition time can be determined by simulating the circuit with an ideal source or with an op-amp with very high bandwidth. This initial target acquisition time can then be used to provide some guidance in op-amp selection, and then design refinement can proceed as normal.

Analytical Solution for ADC Acquisition Time

A quick method for estimating the ADC S+H time given selections of R_s and C_s (along with the input model parameters from the device-specific data manual) is to use the formulas shown in [Equation 1](#) and [Equation 2](#):

$$T = (R_s + R_{on})C_h + R_s (C_s + C_p)$$

$$k = \ln\left(\frac{2^N}{\text{target settling error}}\right) - \ln\left(\frac{C_s + C_p}{C_h}\right)$$

$$\text{acquisition time} = Tk \tag{1}$$

Example Analytical Solution for ADC Acquisition Time

- $n = 12$ bits
- $R_{on} = 500 \Omega$
- $C_h = 12.5$ pF
- $C_p = 12.7$ pF
- Target settling error = 1/2 LSBs
- $R_s = 180 \Omega$
- $C_s = 150$ pF

$$T = (180 \Omega + 500 \Omega)12.5 \text{ pF} + 180 \Omega(150 \text{ pF} + 12.7 \text{ pF}) = 37.8 \text{ ns}$$

$$k = \ln\left(\frac{4069 \text{ LSBs}}{0.5 \text{ LSBs}}\right) - \ln\left(\frac{(150 \text{ pF} + 12.7 \text{ pF})}{12.5 \text{ pF}}\right) = 6.4 \text{ time constants}$$

$$\text{acquisition time} = 37.8 \text{ ns} \times 6.4 = 242 \text{ ns} \quad (2)$$

5 Summary

Input settling is an important design consideration for ADC driving circuits. Without proper evaluation, distortion and memory cross-talk errors could occur, resulting in degraded sensing performance and accuracy.

By using the excellent resources provided by in the [TI Precision Labs - SAR ADC Input Driver Design](#) video series, the [Analog Engineer's Calculator](#), and the guidance in this application report, input settling can be systematically evaluated to ensure that ADC driving circuits have appropriate settling performance.

6 References

- [TI Precision Labs - SAR ADC Input Driver Design](#)
- [Analog Engineer's Calculator](#)
- [TINA-TI](#)
- [TMS320F28004xMicrocontrollers Data Manual](#)

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