Using Power IC for OMAP34xx to 36xx Family

ABSTRACT

The OMAP36xx family MPU can operate at up to 1 GHz. These new use cases increase 36xx current requirement. This document describes how to use the power IC with an OMAP36xx at 1 GHz.

This application note is applicable for TPS65921 and TPS65950 devices.

Contents

List of Tables

1 Introduction

The new OMAP36xx family MPU running at 1 GHz needs more current from VDD1 power supply domain. The rest of the supply tree remains unchanged.

2 Description of Changes

2.1 Application Schematic With OMAP34xx

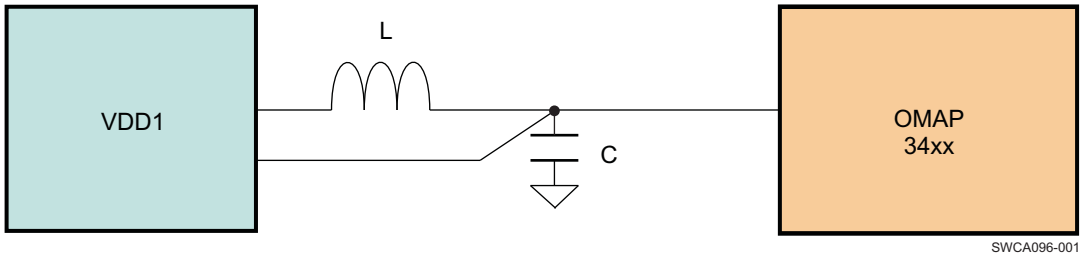

Figure 1. VDD1 External Components Connectivity for OMAP34xx

Table 1. VDD1 Components List for 34xx

Component	Min	Typical	Max	Unit
L	0.7	1	1.3	µH
C	5	10	15	µF

2.2 Application Schematic With OMAP36xx Running at 1 GHz

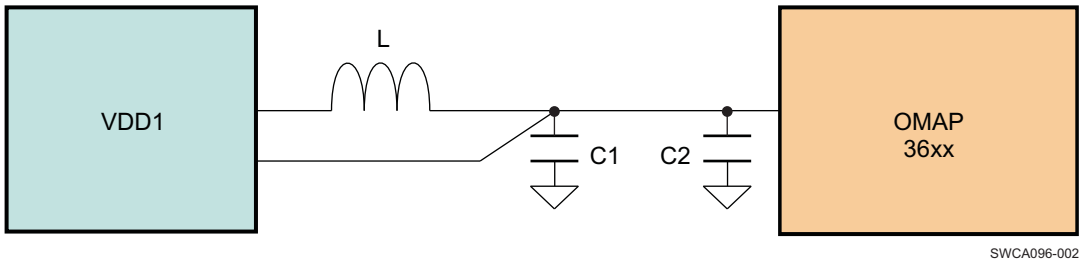

Figure 2. VDD1 External Components Connectivity for OMAP36xx

Table 2. VDD1 Components List for OPP1G

Component	Min	Typical	Max	Unit
L	0.7	1	1.3	µH
C1	11	22	33	µF
C2	11	22	33	µF

2.3 Change List and Points To Check

2.3.1 Inductor Saturation Current

VDD1 current increases; therefore, the inductor saturation increases up to a minimum of 2.1 A. This value must be at the inductor maximum temperature.

NOTE: Inductor DC resistance must be chosen carefully. A resistance which is too high affects DC-DC efficiency.

2.3.2 Voltage Drop from DC-DC Output Sense Point to OMAP Supply Balls

The DC-DC regulates the voltage at the point where the sense line is connected. Therefore, the voltage drop between the sense point and the OMAP™ MPU balls must be carefully minimized.

2.3.3 Load Transient Improvement

It is possible to improve the load transient. To achieve this, capacitor C1 should be increased to 22 µF and a capacitor of the same value as C2 can be added close to the OMAP balls. C1 is still located at the sense point.

2.3.4 Power Distribution Network

For simplicity, only tank capacitors are drawn. Some low-value capacitors must be placed along the VDD1 trace to ensure a flat frequency response of the power distribution network (PDN).

2.4 Software Compatibility

The programming model is identical between current devices and devices with enhanced current capability. No software update is necessary.

3 Power IC Impact

3.1 Part Number Upgrade

The part names are changed to identify which power IC to use with OMAP36xx 1 GHz.

Original device name (VDD1 @ 1.2 A)	New device name (VDD1@ 1.4 A)
TPS65950A2	TPS65950A3
TPS65921B	TPS65921B1

3.2 Specification Update

This section summarizes VDD1 electrical characteristics.

NOTE: Data manuals are the only reference for electrical parameters. Table 3 and Table 4 are for explanation only.

3.2.1 VDD1 Specification for TPS65950A2 and TPS65921B

Table 3. VDD1 DC-DC Regulator Characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.45	V
Output voltage step	Covering the 0.6 to 1.45-V range		12.5		mV
Output accuracy(1)	0.6 to < 0.8 V	–6%		6%	
	0.8 to 1.45 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency(2) in active and sleep modes	I_O = 100 mA, sleep		82%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
	600 mA < I_O < 1.1 A		75%		
Output current	Active mode			1.2	A
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			3	µA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	V_{IN} = V_{Max}		2.2		A
DC load regulation	0 < I_O <I_{MAX}			20	mV
Transient load regulation(3)	I_O = 10 mA to (I_{MAX}/2) + 10 mA, Maximum slew rate is I_{MAX}/2/100 ns	–65		50	mV
DC line regulation				10	mV
Transient line regulation	300 mV_{PP} AC input, 10-µs rise and fall time			10	mV
Startup time			0.25	1	ms
Recovery time	From sleep to on mode with constant load		<10	100	µs
Slew rate (rising or falling)(4)		4	8	16	mV/µs
Output shunt resistor (pulldown)			150		Ω
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current	1.8			A

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(2) VBAT = 3.8 V, VDD1 = 1.3 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, and ESR = 10 mΩ
(3) Output voltage must discharge the load current completely and settle to its final value within 100 µs.
(4) Load current varies proportionally with the output voltage. The slew rate is for increasing and decreasing voltages and the maximum load current is 1.1 A.

Table 3. VDD1 DC-DC Regulator Characteristics (continued)

Parameter	Comments	Min	Typ	Max	Unit
External capacitor[5]	Value	8	10	12	µF
	Equivalent series resistance (ESR) at switching frequency	0		20	mΩ

(5) Under current load condition step:
Imax/2 (550 mA) in 100 ns with a ±20% external capacitor accuracy or
Imax/3 (367 mA) in 100 ns with a ±50% external capacitor accuracy

3.2.2 VDD1 Specification for TPS65950A3 and TPS65921B1

Parameters that changed for 1.4-GHz support are in **bold**.

Table 4. VDD1 DC-DC Regulator Characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.45	V
Output voltage step	Covering the 0.6 to 1.45-V range		12.5		mV
Output accuracy[1]	0.6 to < 0.8 V	–6%		6%	
	0.8 to 1.45 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency [2] in active and sleep modes	I_O = 100 mA, sleep		82%		
	100 mA < I_O < 400 mA, active		85%		
	400 mA < I_O < 600 mA, active		80%		
	600 mA < I_O < 1.1 A, active		75%		
Output current	Active mode, output voltage 0.6–1.2 V			1.2	A
	Active mode, output voltage 1.2–1.45 V			**1.4**	**A**
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			3	µA
	Sleep, unloaded		30	50	µA
	Active, unloaded, not switching			300	µA
Short-circuit current	V_{IN} = V_{Max}		2.2		A
DC load regulation				20	mV
Transient load regulation[3]	I_O = 10 mA to 600 mA, Maximum slew rate is 600 mA/100 ns	–65		50	mV
DC line regulation				10	mV
Transient line regulation	300 mV_{PP} AC input 10-µs rise and fall time			10	mV
Startup time			0.25	1	ms
Recovery time	From sleep to on mode with constant load		<10	100	µs
Slew rate (rising or falling)[4]		4	8	16	mV/µs
Output shunt resistor (pull down)			150		Ω
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current	**2.1**			A

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process).
(2) **VBAT = 3.6 V, VDD1 = 1.2 V**, Fs = 3.2 MHz, L, C according to specification
(3) Output voltage must discharge the load current completely and settle to its final value within 100 µs.
(4) Load current varies proportionally with the output voltage. The slew rate is for increasing and decreasing voltages and the maximum load current is 1.1 A.

Table 4. VDD1 DC-DC Regulator Characteristics (continued)

Parameter	Comments	Min	Typ	Max	Unit
External capacitor	**Value (two capacitors of 22 µF in parallel are recommended)**		**44**		**µF**
	ESR at switching frequency	0		20	mΩ

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