

Dither Improves ACPR in RF Sampling DAC

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ABSTRACT

This application report presents the usage of dither feature integrated in the AFE7686 transmit chain to improve the Adjacent and alternate channels power ratio (ACPR). ACPR is a key measure of unwanted transmitter output from wireless transmitters used in digital communications systems such as LTE.

While the native ACPR performance of newer generations of RF sampling DACs have continually improved, performance in certain frequencies and signal conditions may still be limited. This report highlights such a case with test results and recommended usage.

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1 Introduction

The AFE7686 devices are a family of high-performance transceivers integrating quad-channel 14-bit DACs and analog-to-digital converters (ADC) meeting the performance requirements of wireless infrastructure applications. The DAC sampling clock is generated using the on-chip integer-N PLL. The sampling frequency is chosen such that the licensed 3GPP bands fall well within the first Nyquist to avoid roll-off from the sinc response of the DAC. A typical sampling clock frequency is 8847.36 MHz (72×122.88 MHz). The lower odd-order non-linearity (HD3, HD5, and so forth) of DAC is improved using a proprietary IMD enhancement circuit resulting in an additional image (also known as, $F_{DAC} / 2$ image) in the first Nyquist at $F_{DAC} / 2 - F_{out}$, where F_{DAC} is the DAC sampling clock frequency and F_{out} is the TX output frequency. For most 3GPP bands, proper frequency planning places the additional image outside the band of interest which gets rejected due to the bandpass response of the following stages in the transmit chain. However, as F_{out} approaches $F_{DAC} / 4$ the additional image falls close to the band of interest as shown in

the following sections. Dither can be used to recover the performance in such cases and the following sections cover its usage with test results. Typical ACPR requirements along with other transmit specifications at different frequencies are stated in the [TX Electrical Characteristics](#) table of the [AFE7686 Quad/Dual-Channel, RF Sampling Analog Front-End with 14-Bit 9GSPS DACs and 14-Bit 3GSPS ADCs](#) data sheet^[1].

1.1 What is Dither in the AFE7686?

Dither in AFE7686 is a sinusoid (tone) generated using an NCO (numerically controlled oscillator) with a configurable frequency and amplitude. This tone is summed with the incoming digital data before sending it to the DAC. Dedicated resources in AFE7686 for the generation and summation of the dither with the signal ensure that the signal path careabouts like latency, data rate and SerDes rates remain intact.

The nature and sources of distortions in a DAC are covered in SLAA832 and [2]. Dither can also improve performance for signals with high crest factor, such as those used for ACPR (E-TM1.2 of 3GPP TS 36.141) and EVM (E-TM2/E-TM2a of 3GPP TS 36.141) tests.

2 LTE Bands 65-66

3GPP Bands 65 and 66 are a set of (new) bands used exclusively for LTE where the downlink (DL) frequency is 2110 to 2200 MHz. Since the operating frequency is close to $F_{DAC} / 4$, the harmonics and $F_{DAC} / 2$ image will fall close to the bands and can be understood as follows. If $F_{out} = F_{DAC} / 4 \pm \Delta F$,

$$F_{DAC} / 2 \text{ image: } F_{DAC} / 2 - F_{out} = F_{DAC} / 4 + F_{DAC} / 4 - (F_{DAC} / 4 \pm \Delta F) = (F_{DAC} / 4 \pm \Delta F).$$

The above re-arrangement shows that as F_{out} approaches $F_{DAC} / 4$, ΔF approaches zero, that is, the additional image produced will fall close to the desired signal making it difficult to filter out. This necessitates turning off the IMD enhancement engine which adversely affects the odd-order non-linearity products.

The odd-order non-linear products (worse being HD3 and HD5) fall at $F_{DAC} \pm n \times F_{out}$, where $n = 3, 5, \dots$

$$\text{HD3: } 4 \times F_{DAC} / 4 - 3 \times F_{out} = 4 \times F_{DAC} / 4 - 3 \times F_{DAC} / 4 \pm 3 \times \Delta F = F_{DAC} / 4 \pm 3 \times \Delta F$$

$$\text{HD5: } 4 \times F_{DAC} / 4 - 5 \times F_{out} = 4 \times F_{DAC} / 4 - 5 \times F_{DAC} / 4 \pm 5 \times \Delta F = F_{DAC} / 4 \pm 5 \times \Delta F$$

Higher order non-linearity products can also fall close to the desired band for smaller values of ΔF (upper edge of band under consideration).

2.1 Test Setup

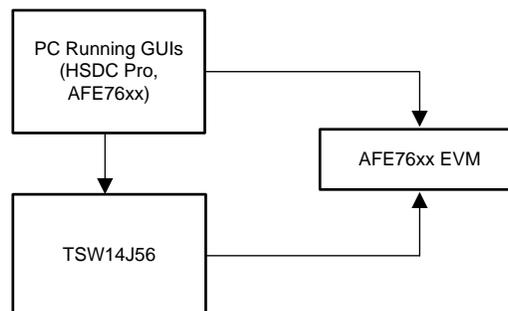
The conditions to evaluate the performance with and without dither is described in this section.

20 MHz E-TM1.1 is fed into the DAC with the output frequency (RF-NCO) centered at 2190 MHz placing the modulated output close to the upper edge of the band (small ΔF). The DAC clocked at 8847.36 MHz, is configured in 2TX_44210 mode, and is set to 18 x interpolation ratio. TSW14J56 capture card is used to feed the LTE pattern to the DAC.

Refer to the [AFE7686 Evaluation Module User's Guide](#) and [TSW14J56EVM User's Guide](#) for detailed instructions to configure AFE7686 EVM and TSW14J56 capture card. The dither feature is configured using low-level register writes to AFE7686.

[Figure 1](#) shows the test setup. The transmitter output is connected to Agilent N9030a PXA spectrum analyzer to measure ACPR.

Figure 1. Test Setup



3 AFE7686 Dither Configuration

The relevant registers to configure the dither feature are in the TX_DUC_P0 page (0x10 page address). [Table 1](#) lists a brief description of these registers. A complete description is found in the AFE7686 register set^[4].

Table 1. Registers to Configure the Dither Feature

REGISTER ADDRESS	DESCRIPTION
0x28<3>	Enables dither block
0x32<7:0>	Sets dither frequency. $\text{frequency} = P / 256 \times F_{\text{DAC}}$, where P = programmed value in decimal and F_{DAC} = DAC sampling clock frequency.
0x33<3>	Enable divide-by-2 in the summation block to prevent clipping. Not needed if input, or dither, or both are backed off.
0x33<2:0>	Selects dither backoff from full-scale. $\text{backoff} = -3 \text{ dB} \times P$, where P = programmed value in decimal.
0x3d<1>	Adds dither in summation block when asserted
0x3d<6:5>	Selects output summing function. Can be left at default setting.

The IMD enhancement feature can be controlled using register 0x29 in TX_DIG_P0 page.

An example (dither) configuration is shown in the following python script example:

```
GUI_Module=__import__('AFE7686')
GUI=GUI_Module.Device_GUI("AFE7686")
*** Dither configuration ***#
GUI.write_register("AFE7686_GLOBAL",0x10,0x55) #Page_Open
GUI.write_register("AFE7686_GLOBAL",0x28,0x0)
GUI.write_register("AFE7686_GLOBAL",0x32,0xf) #dither_freq= 172.8MHz
GUI.write_register("AFE7686_GLOBAL",0x33,0xb) #dither_amp_backoff= -9dB
GUI.write_register("AFE7686_GLOBAL",0x3d,0x22) GUI.write_register("AFE7686_GLOBAL",0x28,0x8)
GUI.write_register("AFE7686_GLOBAL",0x10,0x0) #Page_Close
*** IMD Enhancement ***#
GUI.write_register("AFE76xx_GLOBAL",0x11,1) #Page_Open
GUI.write_register("AFE76xx_GLOBAL",0x29,0xf) #off=0, on=0xf
GUI.write_register("AFE76xx_GLOBAL",0x11,0) #Page_Close
*** Turning off Dither ***#
GUI.write_register("AFE7686_GLOBAL",0x10,0x55) #Page_Open
GUI.write_register("AFE7686_GLOBAL",0x28,0x0) #0x28<3>=0
GUI.write_register("AFE7686_GLOBAL",0x3d,0x20) #0x3d<1>=0
GUI.write_register("AFE76xx_GLOBAL",0x11,0) #Page_Close
```

4 Test Results and Key Guidelines

In this section, results from the tests are discussed along with some recommendation on configuring the dither.

4.1 Test Results

TX output spectrum is shown with different dither settings to quantify the improvement.

Figure 2. TX Output With Default Condition

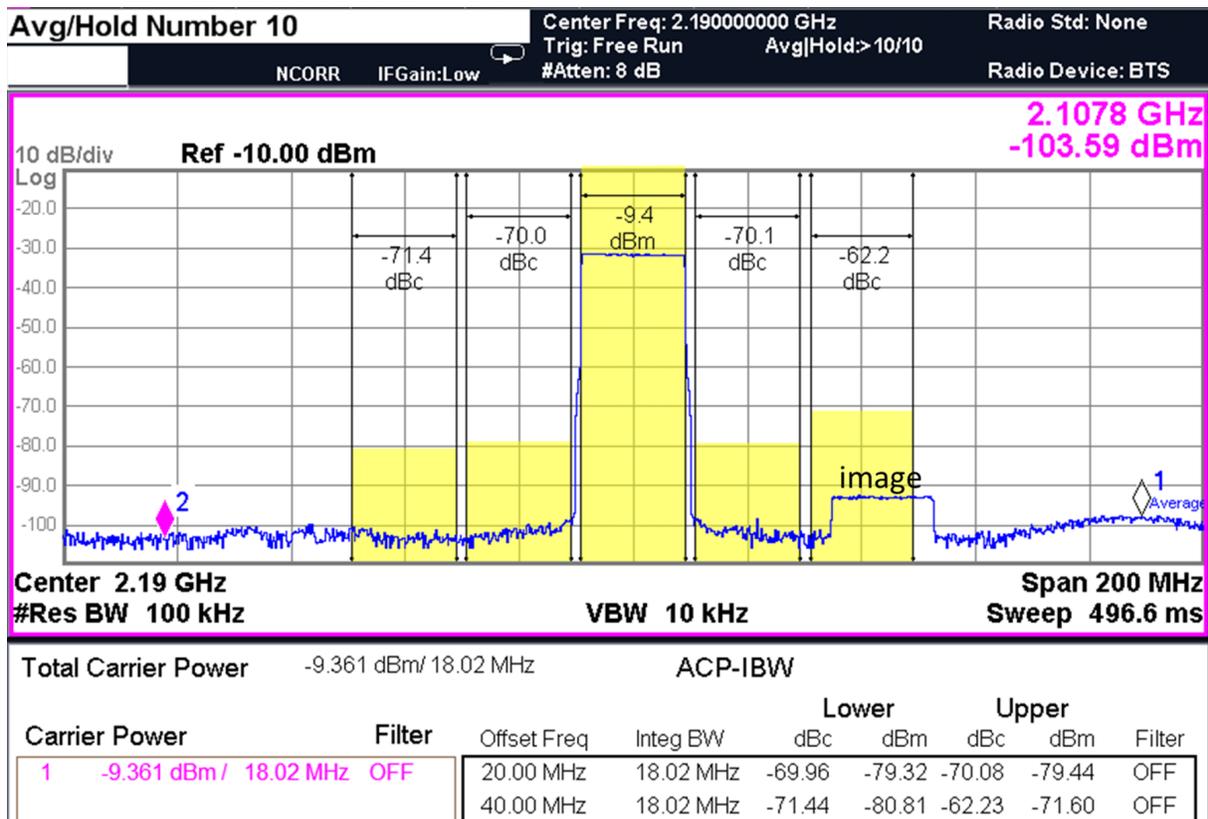
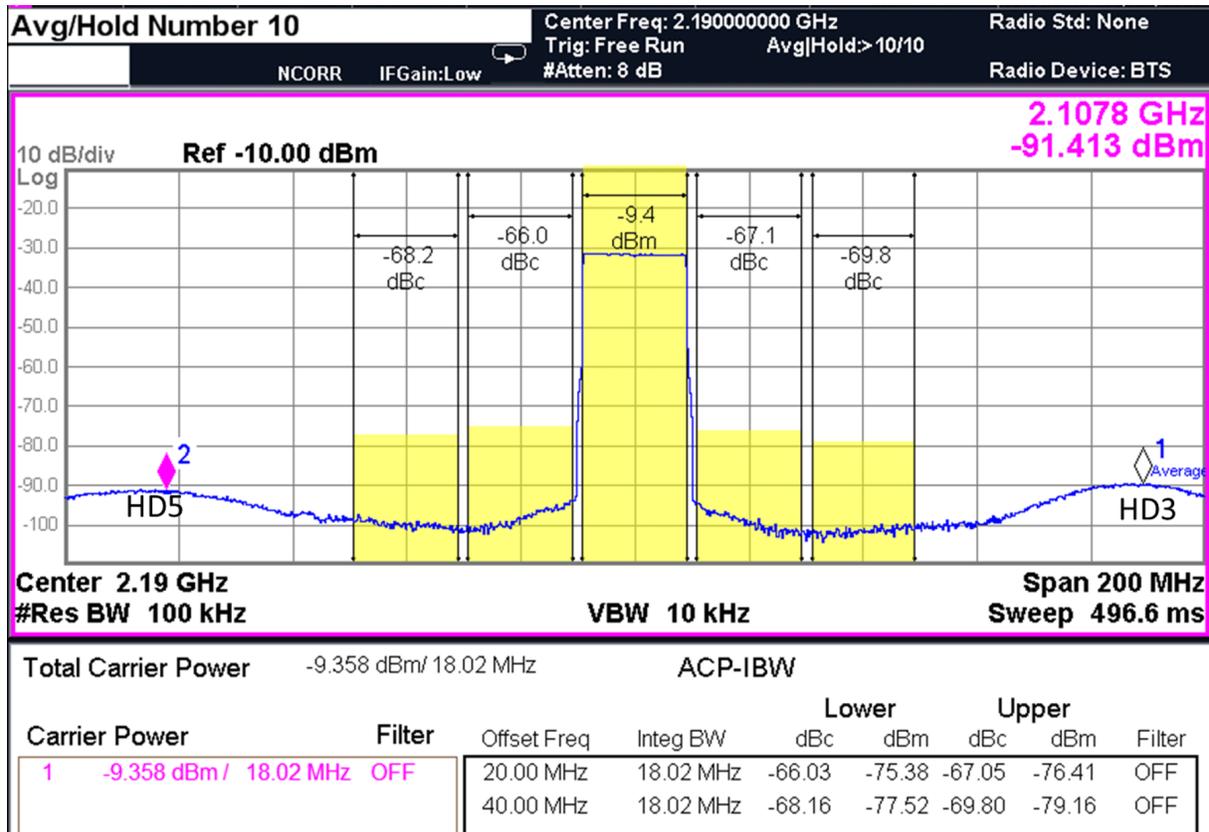


Figure 2 shows the TX output with default configuration (IMD Enhancement turned on, dither turned off). The 20-MHz LTE signal is centered around 2190 MHz. Marker 1 shows the HD3 folded-in and centered around 2277 MHz. Marker 2 shows the HD5 folded-in and centered around 2103 MHz. The $F_{DAC} / 2$ image (labeled "image") is centered around 2234 MHz and falls close to the desired signal degrading the leakage in alternate channel. HD3 and HD5 levels are low courtesy of the IMD Enhancement feature.

The image can be avoided by turning off IMD enhancement as Figure 3 shows. The HD3, HD5 and leakage degrade as shown.

Figure 3. TX Output With IMD Enhancement and Dither Turned Off



In the following sections, various combinations of dither frequency and levels are tried to find an optimal dither setting. IMD Enhancement is kept off.

Figure 4. TX Output With Dither (Level = -6 dB, freq = 207.36 M) and no Divide-by-2

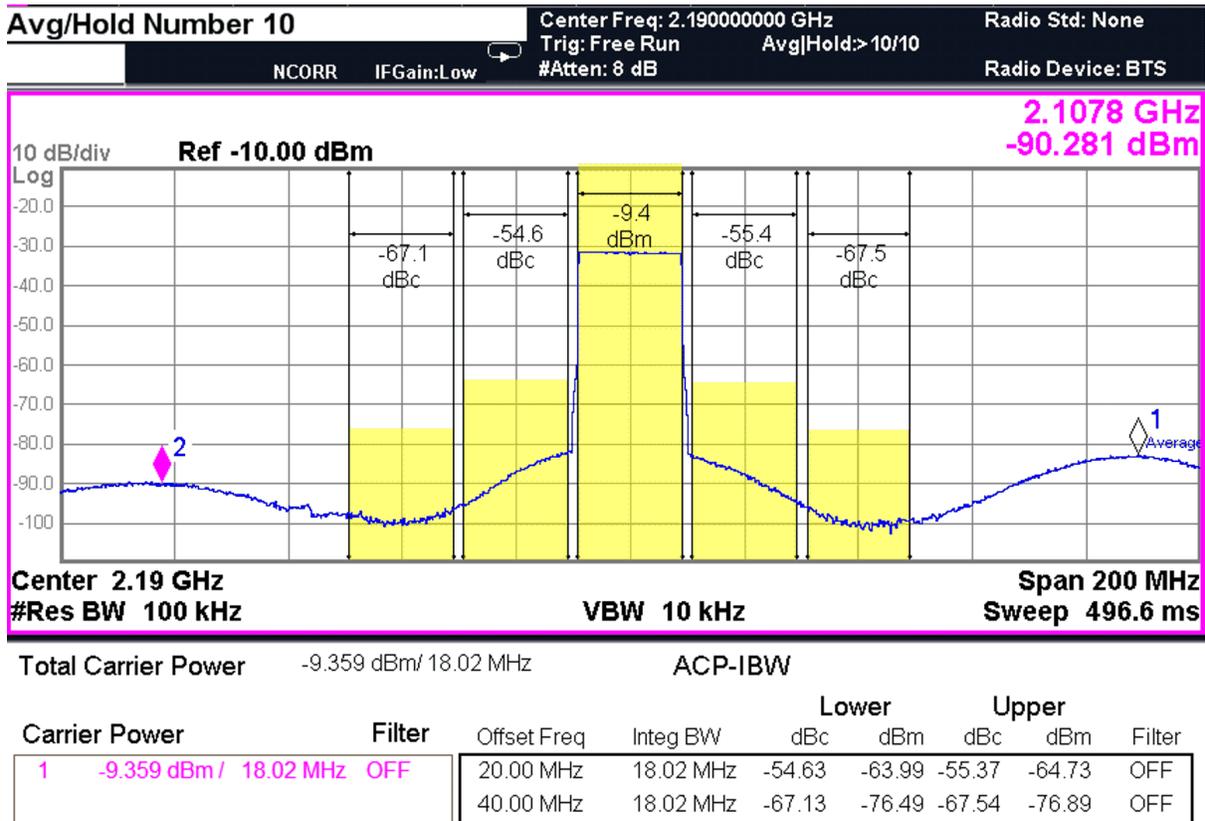


Figure 4 shows a dither setting (0x32=0x6, 0x33=0x2) with the divide-by-2 disabled with signal input at full-scale. The DAC starts to saturate (due to the full-scale input and large dither level) resulting in degraded spectrum. The fix is to enable the divide-by-2 to prevent clipping (0x33<3>=0x1).

Figure 5. TX Output With Dither (Level = -21 dB, freq = 207.36 M) and Divide-by-2

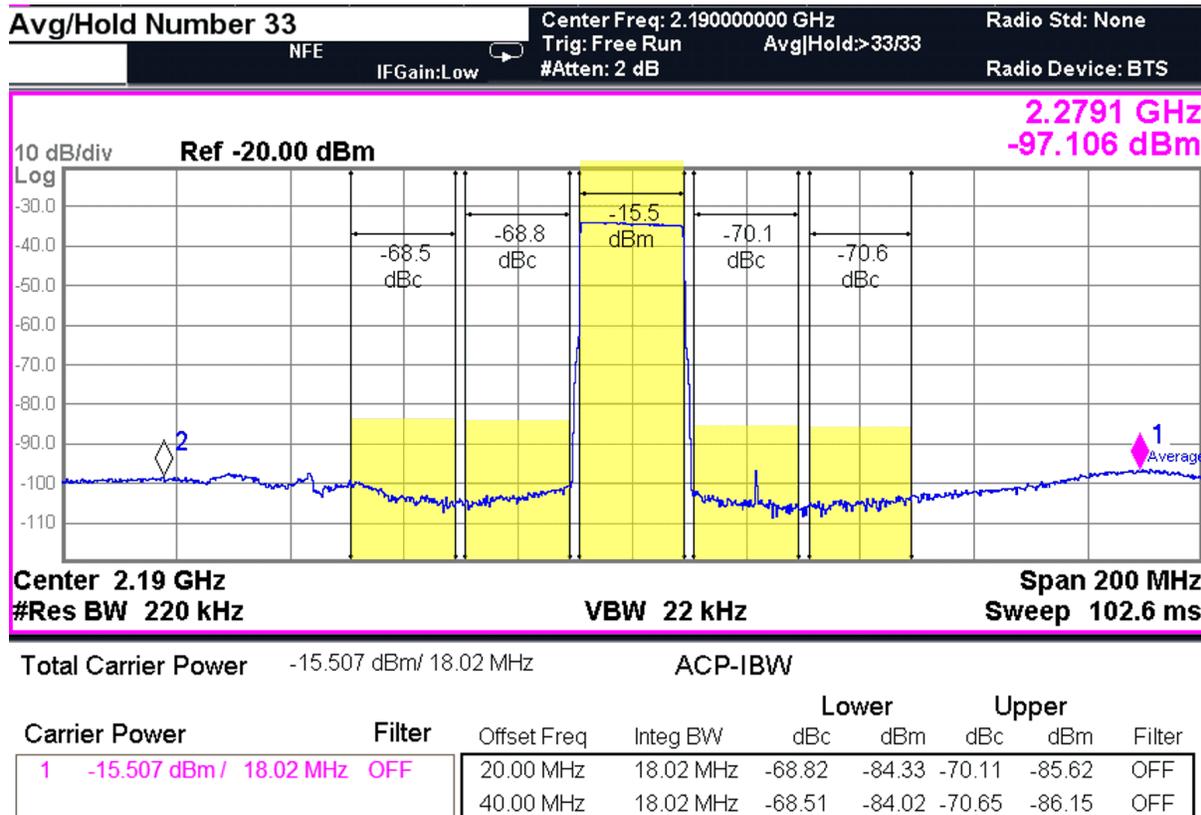
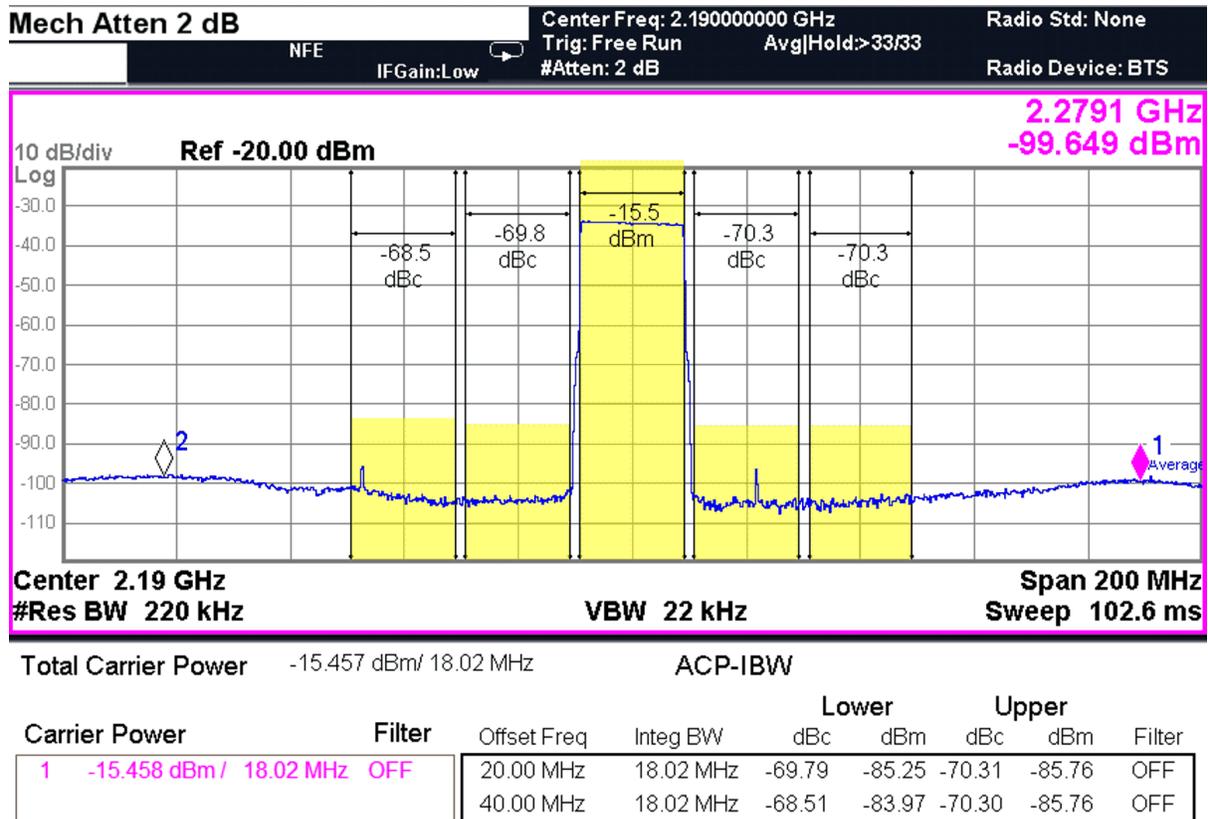


Figure 5 shows the TX output with lower dither level (-21 dB instead of -6 dB) and the divide-by-2 enabled to avoid saturation. The channel power is now 6 dB lower and leakage performance improved. The $F_{DAC} / 4$ spur in the upper adjacent channel is low enough to meet the unwanted emissions specification.

Figure 6 shows another dither setting with slightly lower HD3. The dither level and frequency is increased compared to the previous setting.

Figure 6. TX Output With Dither (Level = -9 dB, freq=518.4 M) and Divide-by-2



The ACPR improved by as much as 8 dB with the use of dither. Markers 1 and 2, respectively, show HD3 and HD5 with levels around -100 dBm.

Figure 7. TX Output Showing Dither and Signal Output

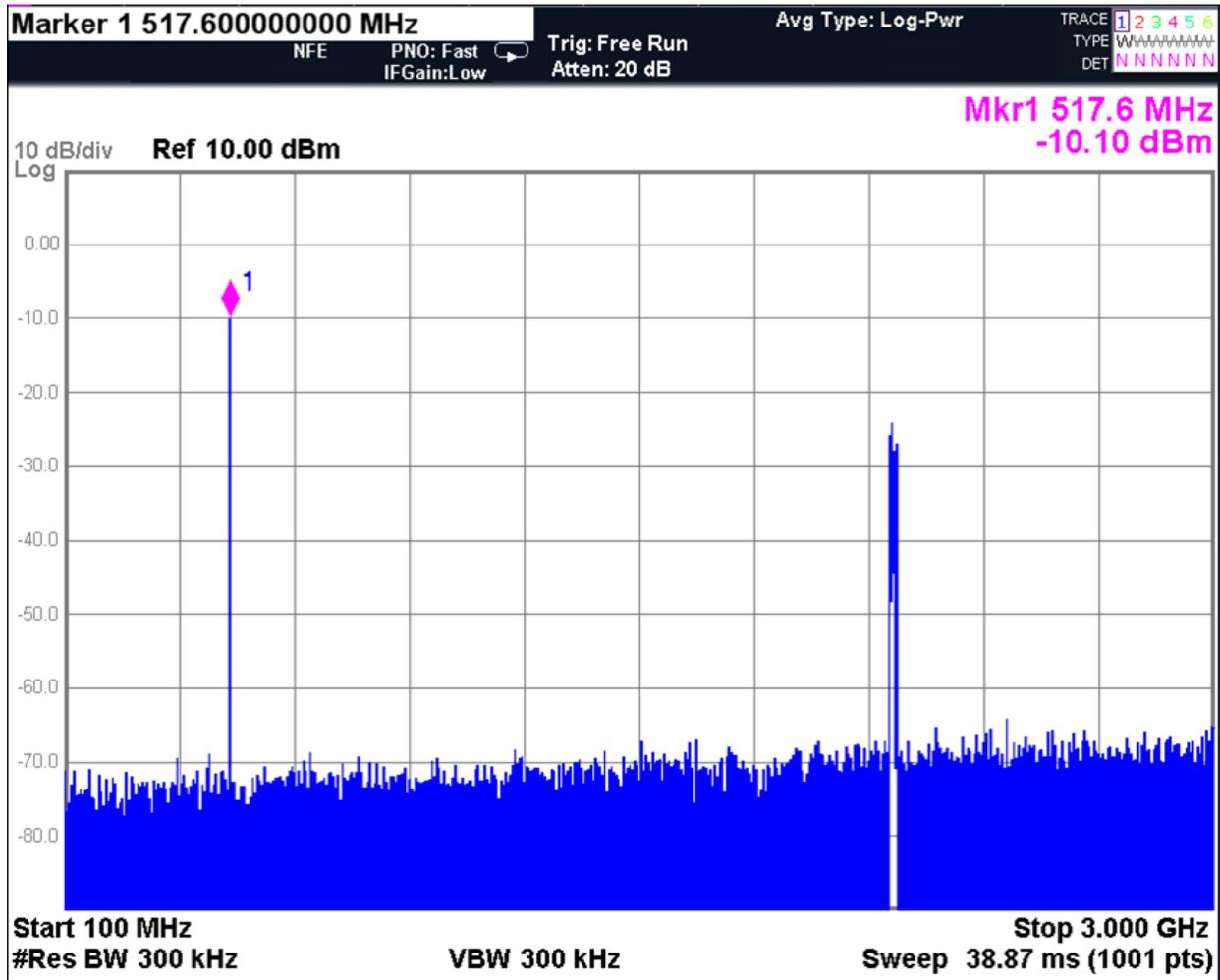


Figure 7 shows the dither at the TX output in addition to the desired signal. However, the frequency response of the signal path following the DAC will prevent this from appearing at the antenna output.

4.2 Guidelines for Dither Usage

As shown in the previous sections, the TX output quality can be significantly improved with dither. However, there is no magical setting applicable for all cases. The choice of frequency and backoff depends on the hardware and use case (channel condition, PAR, output matching, and so forth). A dither setting fine-tuned for the AFE7686EVM may not be suitable in the application board. Use the following guidelines:

- a. Choose a dither frequency such that the fundamental (and any harmonics) is rejected by the bandpass response of the succeeding blocks in the TX signal chain. This sets the upper limit on the dither frequency.
- b. The lower limit on the dither frequency should be chosen with the bandwidth of band in interest, for example, 3GPP band 65, 66 spans from 2.11 to 2.2 GHz. A small dither frequency (say 40 MHz) can have up to 3 harmonics (53x, 54x, 55x) fall in the band, even though their levels may be low.
- c. The dither level is chosen keeping the signal characteristics in mind. Dither is specially useful for signals with large PAR where the dither tone is expected to spread out the codes over a wider range than the signal will. Therefore, a reasonable dither level is required avoiding clipping or saturation at the same time. The optional divide-by-2 to scale down at the summation block can be enabled for this purpose.

5 Conclusion

In this application report, the benefits and usage of dither is highlighted. As shown in the test results, the ACPR improved by about 8 dB without degrading any other performance metric.

6 Related Documentation

1. Texas Instruments, [AFE7686 Quad/Dual-Channel, RF Sampling Analog Front-End with 14-Bit 9GSPS DACs and 14-Bit 3GSPS ADCs Data Sheet](#)
2. Keller, R. (February 2013). [Signal Chain Basics #74: Band-Limited Dither Improves SFDR in High-Speed DACs](#), Planet Analog: Signal Chain Basics #74. Retrieved from https://www.planetanalog.com/author.asp?section_id=483&doc_id=559035
3. Texas Instruments, [AFE7686 Evaluation Module User's Guide](#)
4. Texas Instruments, [AFE7686 Register Set Technical Reference Manual](#)

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