

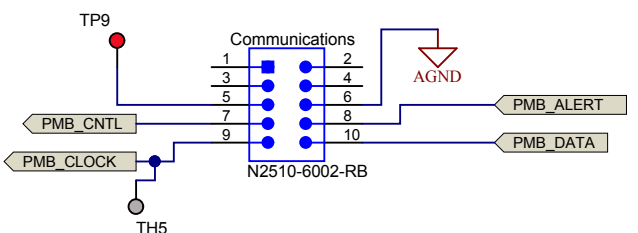
1.00V target Vout

11-13V input 12Vin nominal
470uF input caps for Test purposes only

Tested, see Test Report July 27, 2015

R13 & R43 should be omitted when using VLB10090HT-R33K-B2 inductor

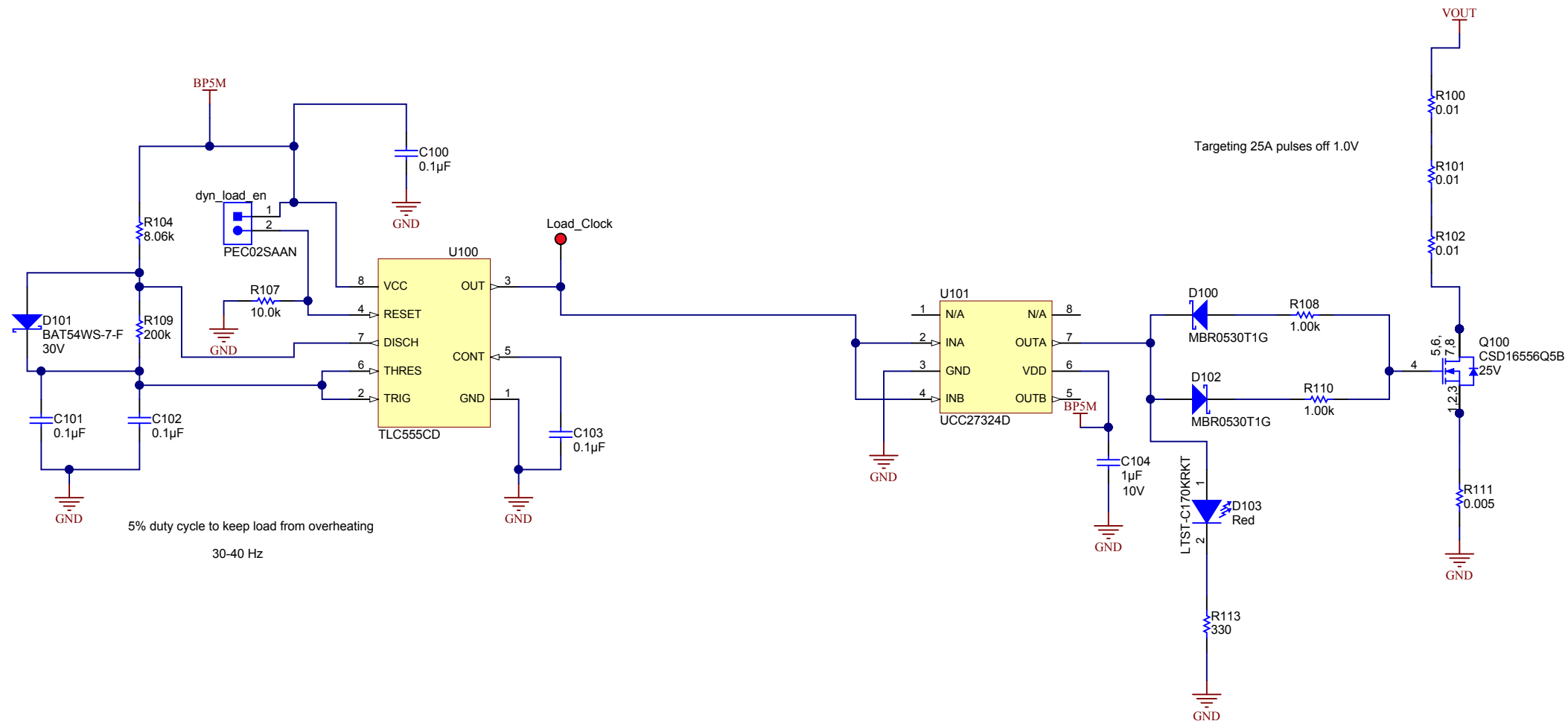
9.76M resistors are placeholders: Do not populate



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Order #:	N/AGND_ph2	Designed for:	Public Release	Mod. Date:	7/27/2015
TID #:	PMP11196	Project Title:	TPS40425&2xUCD74120	1v50a	
Number:	PMP11196	Rev:	A	Sheet Title:	
SVN Rev:	Version control disabled	Assembly Variant:	001	Sheet:	2 of 3
Drawn By:		File:	PMP11196_TPS40425&2xUCD74120.SchDoc	Size:	B
Engineer:	Josh Mandelcom	Contact:	http://www.ti.com/support		





5% duty cycle to keep load from overheating
30-40 Hz

Targeting 25A pulses off 1.0V

Tested, see Test Report July 27, 2015

PCB Number: PMP11196
PCB Rev: A

Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

DNP FID1 DNP FID2 DNP FID3

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

H9 SJ-5303 (CLEAR) H10 SJ-5303 (CLEAR) H11 SJ-5303 (CLEAR) H12 SJ-5303 (CLEAR)

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Orderable: N/A	Designed for: Public Release	Mod. Date: 7/27/2015
TID #: PMP11196	Project Title: TPS40425&2xUCD74120_1v50a	
Number: PMP11196	Rev: A	Sheet Title:
SVN Rev: Version control disabled	Assembly Variant: 001	Sheet: 3 of 3
Drawn By:	File: PMP11196_DynLoad_Hardware.SchDoc	Size: B
Engineer: Josh Mandelcom	Contact: http://www.ti.com/support	



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