

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric	FR-4	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL
 MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

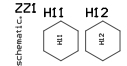
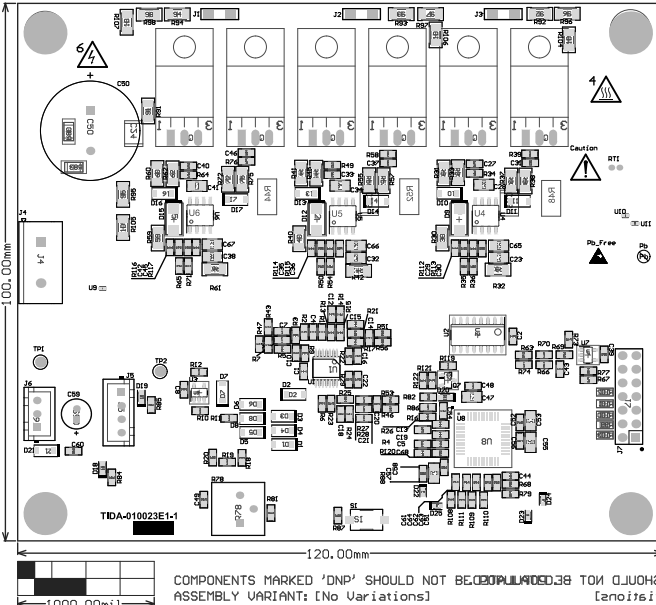
SURFACE FINISH: IMMERSION GOLD (ENG) ENEPG
 MM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

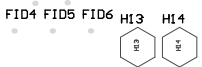
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



ZZ1 H11 H12
 ZZ1 In small label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematics.



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED OR PURCHASED FROM TI. THIS IS A DESIGN NOTE.
 ASSEMBLY VARIANT: [No Variations]

ADDITIONAL INFORMATION: PCB FILE NAME: TIDA-010023_PCB.PCBOC	BOARD #: XXXXXXXX	DATE: 01/11/2018	DESIGNED BY: SUN JING	DESIGNED FOR: TI
LAYER NAME = Top Layer	TID #: N/A	#: 011	DATE: 01/11/2018	DESIGNED BY: SUN JING
PLANT NAME: TI	DATE: 01/11/2018	#: 011	DESIGNED BY: SUN JING	DESIGNED FOR: TI

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PROJECT TITLE: Change in menu Project Project Options Parameters	LAYOUT BY: Headdid the Layout?
DESIGNED FOR: Public Release	ALTIM DESIGNER VERSION: 17.1.9.592
FILE NAME: TIDA-010023_PCB.PCBOC	SCALE: 1.00

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
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7	Bottom Overlay				

DESIGN INFORMATION

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 MN. CLEARANCE: 0.2 mm
 MN. VIA PAD SIZE: 24 MIL
 MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
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 OTHER +/- _____
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 OTHER +/- _____

DRILLING:

REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER _____

BOARD FINISH:

SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN OTHER _____
 MATTE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENERP
 MM. TIN/SILVER OR EQUIV OTHER _____

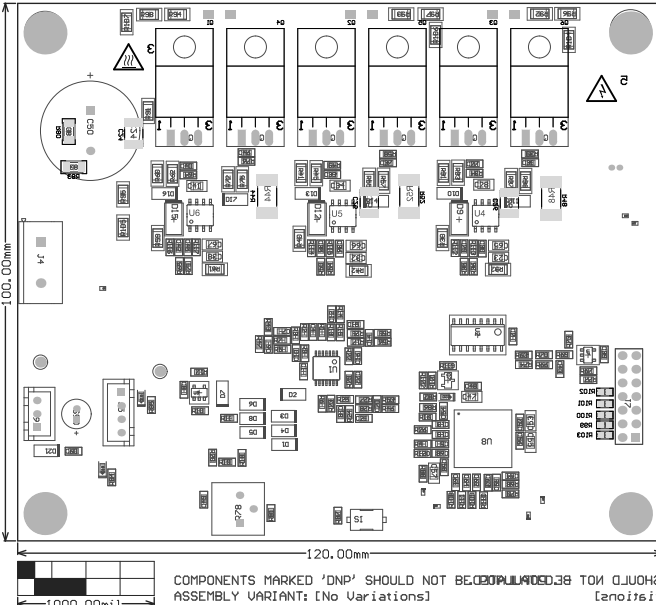
ARRAY/PANEL: CUT AND TRIM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES

BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL VIAS REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



Z21 Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematics.



ADDITIONAL INFORMATION	BOARD #:	DATE:	DESIGNED BY:	DESIGNED FOR:	FILE NAME:	ENGINEER:	LAYOUT BY:
ADDITIONAL INFORMATION	XXXXXXX	01/12/2018	XXXXXXXXXX	Public Release	TIDA-010023_PCB.PCBDOC	XXXXXXXXXX	XXXXXXXXXX
LAYER NAME =	TID #:	DATE:	DESIGNED BY:	DESIGNED FOR:	FILE NAME:	ENGINEER:	LAYOUT BY:
XXXXXXXXXX	N/A	01/12/2018	XXXXXXXXXX	Public Release	TIDA-010023_PCB.PCBDOC	XXXXXXXXXX	XXXXXXXXXX
PLT NAME =	DATE:	DESIGNED BY:	DESIGNED FOR:	FILE NAME:	ENGINEER:	LAYOUT BY:	SCALE:
XXXXXXXXXX	01/12/2018	XXXXXXXXXX	Public Release	TIDA-010023_PCB.PCBDOC	XXXXXXXXXX	XXXXXXXXXX	1:1

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SCALE: 1.00	ALTIM DESIGNER VERSION: 17.1.9.592
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